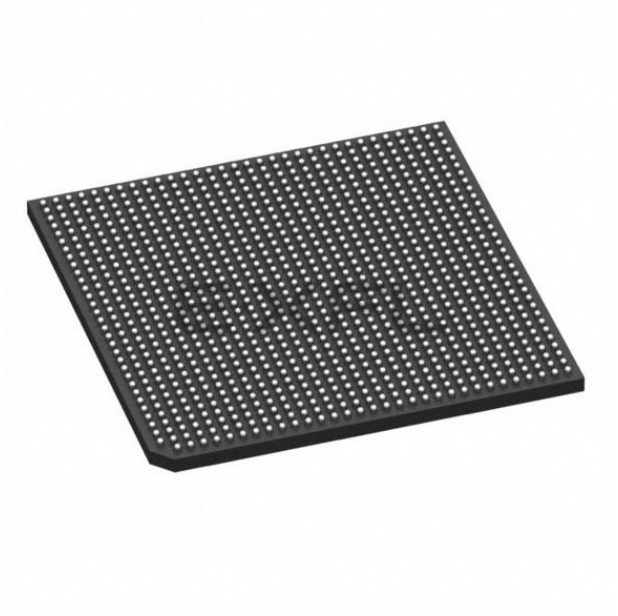

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1500kc

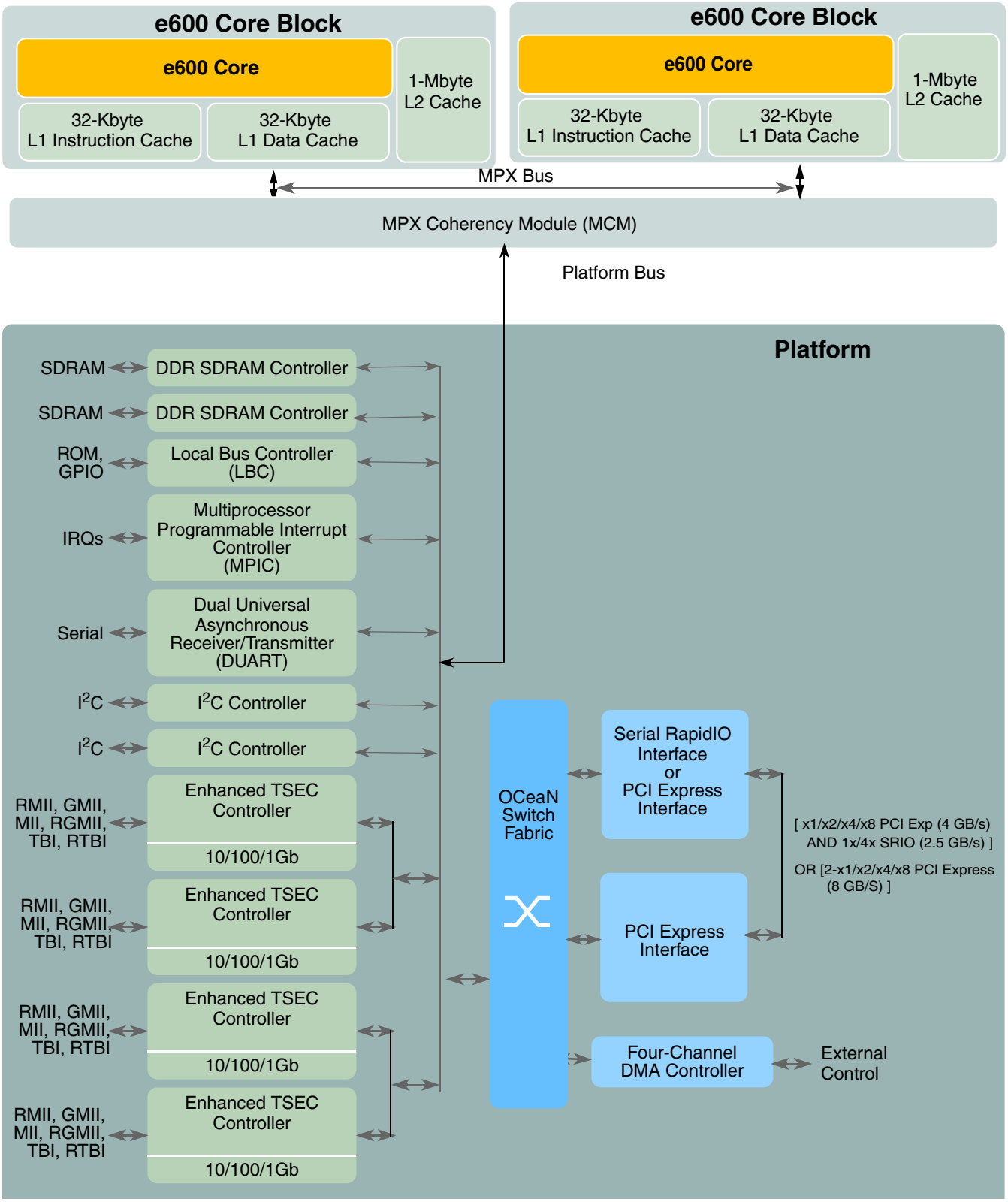

Figure 1. MPC8641 and MPC8641D

should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

Table 9. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks (EC1_GTX_CLK125 and EC2_GTX_CLK125) AC timing specifications for the MPC8641.

Table 10. EC*n*_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	—	125 ±100 ppm	—	MHz	3
EC*n*_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC*n*_GTX_CLK125 peak-to-peak jitter	t_{G125J}	—	—	250	ps	1

Figure 7 provides the AC test load for the DDR bus.

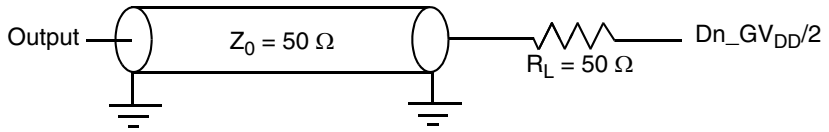

Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	1,2
Maximum baud rate	MPX clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:
1. Guaranteed by design.
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}[3]	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.

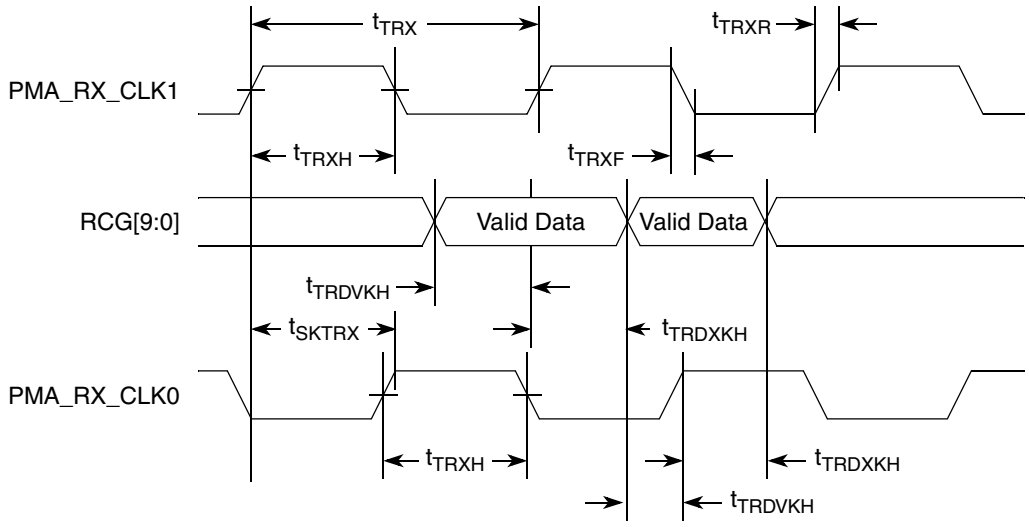

Figure 17. TBI Receive AC Timing Diagram

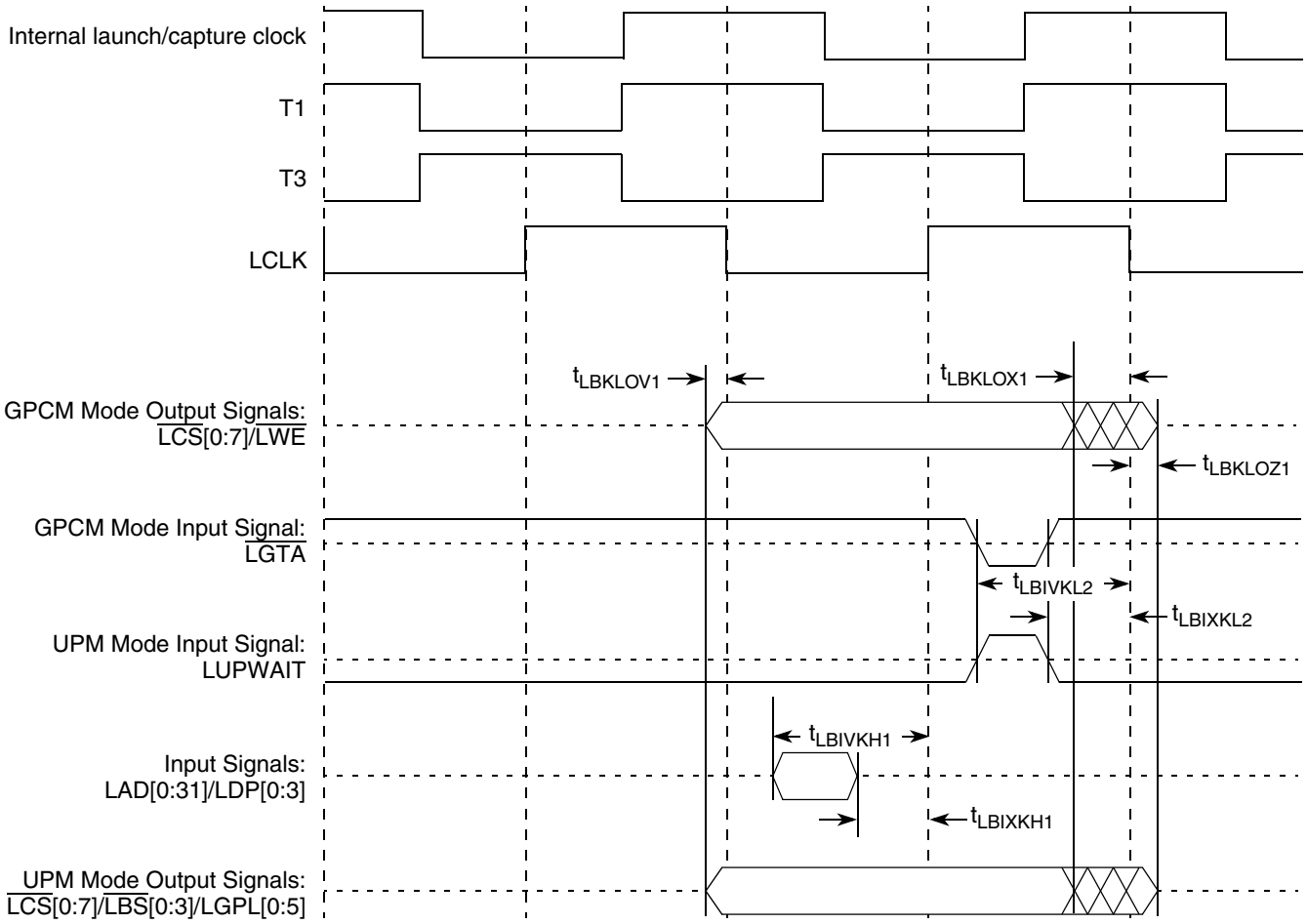

Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8641/D.

11.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

11.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 35.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5

Figure 37 shows the AC timing diagram for the I^2C bus.

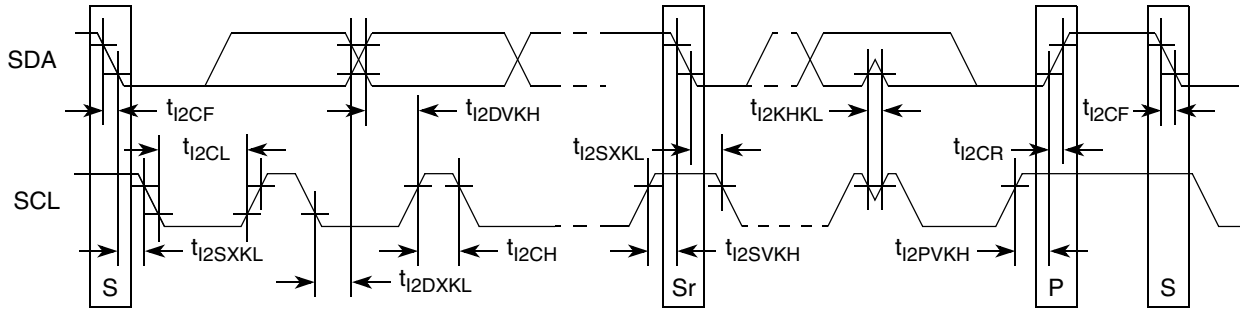

Figure 37. I^2C Bus AC Timing Diagram

13 High-Speed Serial Interfaces (HSSI)

The MPC8641D features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ for PCI Express and Serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD}_SRDS*n* are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has a 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

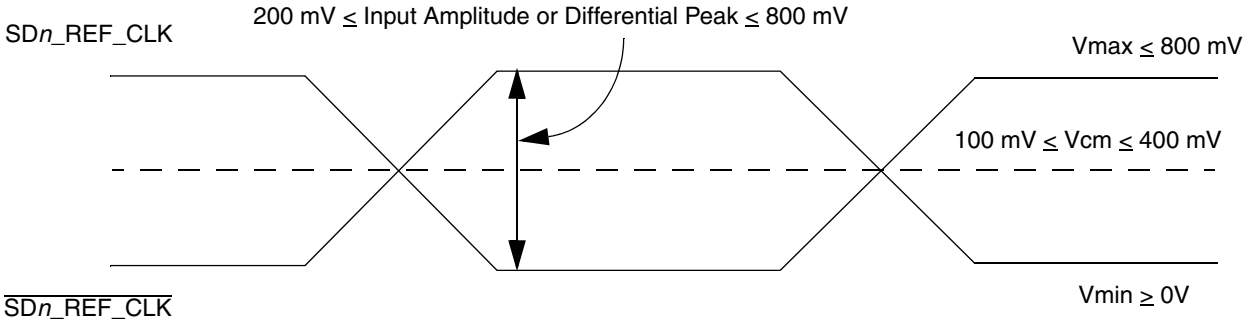

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

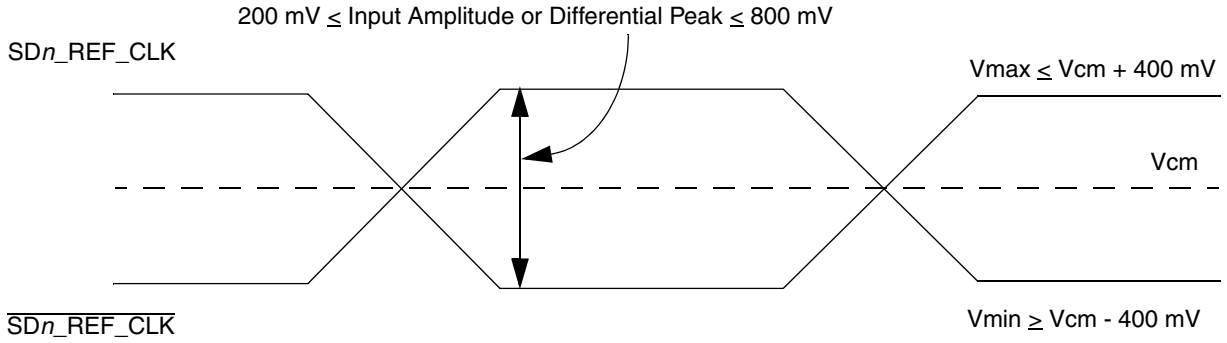

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

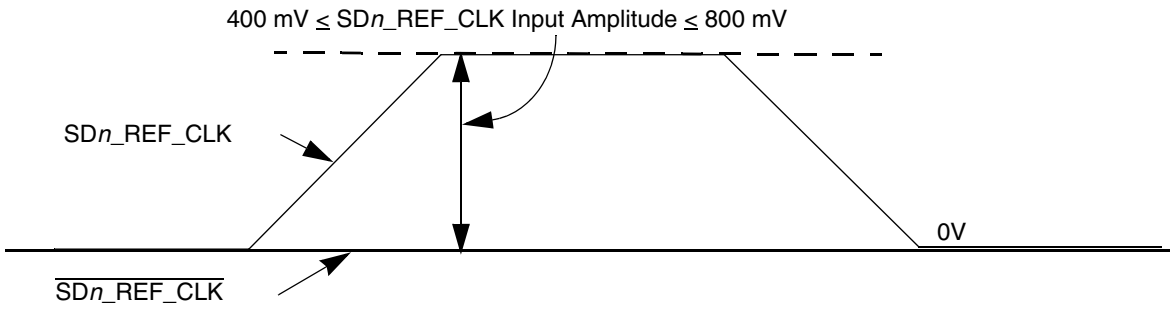

Figure 42. Single-Ended Reference Clock Input DC Requirements

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	—	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.
$T_{crosslink}$	Crosslink Random Timeout	0	—	—	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. MPC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

16 Package

This section details package parameters and dimensions.

16.1 Package Parameters for the MPC8641

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 pins. There are two package options: high-lead Flip Chip-Ceramic Ball Grid Array (FC-CBGA), and lead-free (FC-CBGA).

For all package types:

Die size	12.1 mm × 14.7 mm
Package outline	33 mm × 33 mm
Interconnects	1023
Pitch	1 mm
Total Capacitor count	43 caps; 100 nF each

For high-lead FC-CBGA (package option: HCTE[1] HX)

Maximum module height	2.97 mm
Minimum module height	2.47 mm
Solder Balls	89.5% Pb 10.5% Sn
Ball diameter (typical[2])	0.60 mm

For RoHS lead-free FC-CBGA (package option: HCTE[1] VU) and lead-free FC-CBGA (package option: HCTE[1] VJ)

Maximum module height	2.77 mm
Minimum module height	2.27 mm
Solder Balls	95.5% Sn 4.0% Ag 0.5% Cu
Ball diameter (typical[2])	0.60 mm

[1] High-coefficient of thermal expansion

[2] Typical ball diameter is before reflow

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV_{DD}	13, 18
SD1_DLL_TPD	N28	O	SV_{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV_{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)[4]				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV_{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV_{DD}	34
$\overline{\text{SD2\_TX}}$[0:3]	Y25, AA28, AB26, AC28	O	SV_{DD}	—
$\overline{\text{SD2\_TX}}$[4:7]	AE28, AG28, AJ28, AL28	O	SV_{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV_{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV_{DD}	32, 35
$\overline{\text{SD2\_RX}}$[0:3]	Y29, AA31, AB29, AC31	I	SV_{DD}	—
$\overline{\text{SD2\_RX}}$[4:7]	AH29, AJ31, AK29, AL31	I	SV_{DD}	35
SD2_REF_CLK	AE32	I	SV_{DD}	—
$\overline{\text{SD2\_REF\_CLK}}$	AE31	I	SV_{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV_{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV_{DD}	30
SD2_PLL_TPD	AF29	O	SV_{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV_{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV_{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV_{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals[5]				
EC1_GTX_CLK125	AL23	I	LV_{DD}	39
EC2_GTX_CLK125	AM23	I	TV_{DD}	39
EC_MDC	G31	O	OV_{DD}	—
EC_MDIO	G32	I/O	OV_{DD}	—
eTSEC Port 1 Signals[5]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LCS[6]/DMA_DACK[2]	E23	O	OV_{DD}	7, 10
LCS[7]/DMA_DDONE[2]	F23	O	OV_{DD}	7, 10
LWE[0:3]/ LSDDQM[0:3]/ LBS[0:3]	E21, F21, D22, E20	O	OV_{DD}	6
LBCTL	D21	O	OV_{DD}	—
LALE	E19	O	OV_{DD}	—
LGPL0/LSDA10	F20	O	OV_{DD}	25
LGPL1/LSDWE	H20	O	OV_{DD}	25
LGPL2/LOE/ LSDRAS	J20	O	OV_{DD}	—
LGPL3/LSDCAS	K20	O	OV_{DD}	6
LGPL4/LGTA/ LUPWAIT/LPBSE	L21	I/O	OV_{DD}	42
LGPL5	J19	O	OV_{DD}	6
LCKE	H19	O	OV_{DD}	—
LCLK[0:2]	G19, L19, M20	O	OV_{DD}	—
LSYNC_IN	M19	I	OV_{DD}	—
LSYNC_OUT	D20	O	OV_{DD}	—
DMA Signals[5]				
DMA_DREQ[0:1]	E31, E32	I	OV_{DD}	—
DMA_DREQ[2]/LCS[5]	B23	I	OV_{DD}	9, 10
DMA_DREQ[3]/IRQ[9]	B30	I	OV_{DD}	10
DMA_DACK[0:1]	D32, F30	O	OV_{DD}	—
DMA_DACK[2]/LCS[6]	E23	O	OV_{DD}	10
DMA_DACK[3]/IRQ[10]	C30	O	OV_{DD}	9, 10
DMA_DDONE[0:1]	F31, F32	O	OV_{DD}	—
DMA_DDONE[2]/LCS[7]	F23	O	OV_{DD}	10
DMA_DDONE[3]/IRQ[11]	D30	O	OV_{DD}	9, 10
Programmable Interrupt Controller Signals[5]				
MCP_0	F17	I	OV_{DD}	—
MCP _1	H17	I	OV_{DD}	12, *S4*
IRQ[0:8]	G28, G29, H27, J23, M23, J27, F28, J24, L23	I	OV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[9]/DMA_DREQ[3]	B30	I	OV_{DD}	10
IRQ[10]/DMA_DACK[3]	C30	I	OV_{DD}	9, 10
IRQ[11]/DMA_DDONE[3]	D30	I	OV_{DD}	9, 10
IRQ_OUT	J26	O	OV_{DD}	7, 11
DUART Signals[5]				
UART_SIN[0:1]	B32, C32	I	OV_{DD}	—
UART_SOUT[0:1]	D31, A32	O	OV_{DD}	—
UART_CTS[0:1]	A31, B31	I	OV_{DD}	—
UART_RTS[0:1]	C31, E30	O	OV_{DD}	—
I^2C Signals				
IIC1_SDA	A16	I/O	OV_{DD}	7, 11
IIC1_SCL	B17	I/O	OV_{DD}	7, 11
IIC2_SDA	A21	I/O	OV_{DD}	7, 11
IIC2_SCL	B21	I/O	OV_{DD}	7, 11
System Control Signals[5]				
HRESET	B18	I	OV_{DD}	—
HRESET_REQ	K18	O	OV_{DD}	—
SMI_0	L15	I	OV_{DD}	—
SMI_1	L16	I	OV_{DD}	12, *S4*
SRESET_0	C20	I	OV_{DD}	—
SRESET_1	C21	I	OV_{DD}	12, *S4*
CKSTP_IN	L18	I	OV_{DD}	—
CKSTP_OUT	L17	O	OV_{DD}	7, 11
READY/TRIG_OUT	J13	O	OV_{DD}	10, 25
Debug Signals[5]				
TRIG_IN	J14	I	OV_{DD}	—
TRIG_OUT/READY	J13	O	OV_{DD}	10, 25
D1_MSRCID[0:1]/ LB_SRCID[0:1]	F15, K15	O	OV_{DD}	6, 10
D1_MSRCID[2]/ LB_SRCID[2]	K14	O	OV_{DD}	10, 25
D1_MSRCID[3:4]/ LB_SRCID[3:4]	H15, G15	O	OV_{DD}	10
D2_MSRCID[0:4]	E16, C17, F16, H16, K16	O	OV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*	—	—
Reset Configuration Signals[20]				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV_{DD}	—
TSEC1_TXD[1]/ cfg_platform_freq	AC23	—	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	—	LV_{DD}	—
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	—	LV_{DD}	—
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV_{DD}	—
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV_{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	—	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	—	LV_{DD}	—
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV_{DD}	—
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	—
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	—	LV_{DD}	—
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	—	LV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

Note:

1. Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.
3. If a DDR port is not used, it is possible to leave the related power supply (Dn_GVDD, Dn_MVREF) turned off at reset. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.
4. Low Voltage Differential Signaling (LVDS) type pins.
5. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
6. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
7. Recommend a weak pull-up resistor (1–10 kΩ) be placed from this pin to its power supply.
8. Recommend a weak pull-down resistor (2–10 kΩ) be placed from this pin to ground.
9. This multiplexed pin has input status in one mode and output in another
10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
11. This pin is open drain signal.
12. Functional only on the MPC8641D.
13. These pins should be left floating.
14. These pins should be connected to SV_{DD}.
15. These pins should be pulled to ground with a strong resistor (270-Ω to 330-Ω).
16. These pins should be connected to OVDD.
17. This is a SerDes PLL/DLL digital test signal and is only for factory use.
18. This is a SerDes PLL/DLL analog test signal and is only for factory use.
19. This pin should be pulled to ground with a 100-Ω resistor.
20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
21. Should be pulled down at reset if platform frequency is at 400 MHz.
22. These pins require 4.7-kΩ pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
23. This output is actively driven during reset rather than being tri-stated during reset.
24 These JTAG pins have weak internal pull-up P-FETs that are always enabled.
25. This pin should NOT be pulled down (or driven low) during reset.
26. These are test signals for factory use only and must be pulled up (100-Ω to 1- kΩ) to OVDD for normal machine operation.
27. Dn_MDIC[0] should be connected to ground with an 18-Ω resistor +/– 1-Ω and Dn_MDIC[1] should be connected Dn_GVDD with an 18-Ω resistor +/– 1-Ω. These pins are used for automatic calibration of the DDR IOs.
28. Pin N18 is recommended as a reference point for determining the voltage of V_{DD}_PLAT and is hence considered as the V_{DD}_PLAT sensing voltage and is called SENSEVDD_PLAT.
29. Pin P18 is recommended as the ground reference point for SENSEVDD_PLAT and is called SENSEVSS_PLAT.
30. This pin should be pulled to ground with a 200-Ω resistor.
31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
32. Must be tied low if unused
33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull up/down option to allow flexibility of future designs.
34. Used as serial data output for SRIO 1x/4x link.
35. Used as serial data input for SRIO 1x/4x link.
36. This pin requires an external 4.7-kΩ pull-down resistor to pevent PHY from seeing a valid Transmit Enable before it is actively driven.

Table 65. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Memory bus clock frequency	200	300	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 66. Platform/MPX bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Platform/MPX bus clock frequency	400	500-600	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. Platform/MPX frequencies between 400 and 500 MHz are not supported.

Table 67. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	133	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCRR[CLKDIV]. See the reference manual for the MPC8641D for more information on this.

18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 68:

- SYSCLK input signal

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For

Table 75 shows the parts that are available for ordering and their operating conditions.

Table 75. Part Offerings and Operating Conditions

Part Offerings[1]	Operating Conditions
MC8641Dxx1500KX	Dual core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641Dxx1333JX	Dual core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641Dxx1250HX	Dual core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641Dxx1000GX	Dual core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641Dxx1000NX	Dual core MAX CPU speed = 1000 MHz, MAX DDR = 500 MHz Core Voltage = 0.95 volts
MC8641xx1500KX	Single core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641xx1333JX	Single core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641xx1250HX	Single core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641xx1000HX	Single core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641xx1000NX	Single core Max CPU speed = 1000 MHz, Max DDR = 500 MHz Core Voltage = 0.95 volts

[1] Note that the “xx” in the part marking represents the package option. The upper case “X” represents the revision letter. For more information see Table 74.