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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1500ke

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
PMA_RX_CLK[0:1] clock period	t _{TRX} 3	—	16.0	_	ns
PMA_RX_CLK[0:1] skew	t _{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t _{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t _{TRXR} ²	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t _{TRXF} 2	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}}

2. Guaranteed by design.

3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.



Figure 17. TBI Receive AC Timing Diagram



Ethernet Management Interface Electrical Characteristics

Table 39. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDIO to MDC hold time	t _{MDDXKH}	0	_	—	ns	_
MDC rise time	t _{MDCR}	—	_	10	ns	4
MDC fall time	t _{MDHF}	—	-	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)}

(reference)(state) for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

- 2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
- 3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
- 4. Guaranteed by design.
- 5. t_{MPXCLK} is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.



Figure 23. eTSEC AC Test Load

NOTE

Output will see a 50- Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.



Figure 24. MII Management Interface Timing Diagram



Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Мах	Unit	Notes
Output hold times: Boundary-scan data TDO	t _{JTKLDX} t _{JTKLOX}	30 30		ns	5, 6
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK} .
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.



Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 33. JTAG Clock Input Timing Diagram





Figure 37 shows the AC timing diagram for the I^2C bus.



Figure 37. I²C Bus AC Timing Diagram

13 High-Speed Serial Interfaces (HSSI)

The MPC8641D features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{SDn}_T\overline{X}$) or a receiver input (SD*n*_RX and $\overline{SDn}_R\overline{X}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):



 The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.



SDn_REF_CLK

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)











Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8641D SerDes reference clock input's DC requirement.



Figure 46. Single-Ended Connection (Reference Only)



Symbol	Parameter	Min	Nom	Max	Units	Comments
T _{TX-EYE}	Minimum TX Eye Width	0.70	_	_	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
T _{TX-EYE-MEDIAN-to-} MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median.	_	_	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
T _{TX-RISE} , T _{TX-FALL}	D+/D-TX Output Rise/Fall Time	0.125	_	_	UI	See Notes 2 and 5
V _{TX-CM-ACp}	RMS AC Peak Common Mode Output Voltage	_	_	20	mV	
V _{TX-CM-DC-ACTIVE-} IDLE-DELTA	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	_	100	mV	$eq:logical_lo$
V _{TX-CM} -DC-LINE-DELTA	Absolute Delta of DC Common Mode between D+ and D-	0	_	25	mV	$\begin{split} & V_{\text{TX-CM-DC-D+}} - V_{\text{TX-CM-DC-D-}} <= 25 \text{ mV} \\ &V_{\text{TX-CM-DC-D+}} = DC_{(\text{avg})} \text{ of } V_{\text{TX-D+}} \\ &V_{\text{TX-CM-DC-D-}} = DC_{(\text{avg})} \text{ of } V_{\text{TX-D-}} \\ &\text{See Note 2.} \end{split}$
V _{TX-IDLE} -DIFFp	Electrical Idle differential Peak Output Voltage	0	_	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \le 20 \text{ mV}$ See Note 2.
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection		_	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
V _{TX-DC-CM}	The TX DC Common Mode Voltage	0	_	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX Short Circuit Current Limit	—	_	90	mA	The total current the Transmitter can provide when shorted to its ground
T _{TX-IDLE-MIN}	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set



Symbol	Parameter	Min	Nom	Max	Units	Comments
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
L _{TX-SKEW}	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes see Figure 52). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 52) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should





Figure 52. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/-100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, "SerDes Reference Clocks."

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.



15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- -10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \le \text{Freq}(f) \le \text{Baud}$ Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.



Transmitter Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 58. Transmitter Differential Output Eye Diagram Parameters

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Characteristic	Symbol	Ra	nge	Unit	Netes	
Characteristic	Symbol	Min	Min Max		Notes	
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver	
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55 —		UI p-p	Measured at receiver	
Total Jitter Tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver	
Multiple Input Skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit Error Rate	BER	—	10 ⁻¹²	—	—	
Unit Interval	UI	800	800	ps	+/– 100 ppm	

Table 59. Receiver AC Timing Specifications—1.25 GBaud

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.







15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 59, Table 60, Table 61) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 56 with the parameters specified in Table . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100 \Omega + -5\%$ differential resistive load.



Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100Ω resistive +/- 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/- 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.



Name ¹	Package Pin Number	Pin Type	Power Supply	Notes				
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18				
SD1_DLL_TPD	N28	0	SV _{DD}	13, 17				
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18				
High Speed I/O Interface 2 (SERDES 2) ⁴								
SD2_TX[0:3]	Y24, AA27, AB25, AC27	0	SV _{DD}	—				
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	0	SV _{DD}	34				
SD2_TX[0:3]	Y25, AA28, AB26, AC28	0	SV _{DD}	—				
SD2_TX[4:7]	AE28, AG28, AJ28, AL28	0	SV _{DD}	34				
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32				
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35				
SD2_RX[0:3]	Y29, AA31, AB29, AC31	I	SV _{DD}	—				
SD2_RX[4:7]	AH29, AJ31, AK29, AL31	I	SV _{DD}	35				
SD2_REF_CLK	AE32	I	SV _{DD}	—				
SD2_REF_CLK	AE31	I	SV _{DD}	—				
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19				
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30				
SD2_PLL_TPD	AF29	0	SV _{DD}	13, 17				
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18				
SD2_DLL_TPD	AD29	0	SV _{DD}	13, 17				
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18				
	Special Connection Requi	ement pins	·					
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	_	-	13				
Reserved	H30, R32, V28, AG32	—	—	14				
Reserved	H29, R31, W28, AG31	—	—	15				
Reserved	AD24, AG26	—	—	16				
Ethernet Miscellaneous Signals ⁵								
EC1_GTX_CLK125	AL23	I	LV _{DD}	39				
EC2_GTX_CLK125	AM23	I	TV _{DD}	39				
EC_MDC	G31	0	OV _{DD}	_				
EC_MDIO	G32	I/O	OV _{DD}	_				
	eTSEC Port 1 Sign	als ⁵						

Table 63. MPC8641 Signal Reference by Functional Block (continued)



Table 63. MPC8641 Signal Reference by Functional Block (continued)

	Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
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Note:

- 1. Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
- 2. Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.
- 3. If a DDR port is not used, it is possible to leave the related power supply (Dn_GVDD, Dn_MVREF) turned off at reset. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.
- 4. Low Voltage Differential Signaling (LVDS) type pins.
- 5. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
- 6. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
- 7. Recommend a weak pull-up resistor $(1-10 \text{ k}\Omega)$ be placed from this pin to its power supply.
- 8. Recommend a weak pull-down resistor (2–10 k Ω) be placed from this pin to ground.
- 9. This multiplexed pin has input status in one mode and output in another
- 10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
- 11. This pin is open drain signal.
- 12. Functional only on the MPC8641D.
- 13. These pins should be left floating.
- 14. These pins should be connected to SV_{DD} .
- 15. These pins should be pulled to ground with a strong resistor (270- Ω to 330- Ω).
- 16. These pins should be connected to OVDD.
- 17. This is a SerDes PLL/DLL digital test signal and is only for factory use.
- 18. This is a SerDes PLL/DLL analog test signal and is only for factory use.
- 19. This pin should be pulled to ground with a 100- $\!\Omega$ resistor.
- 20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 21. Should be pulled down at reset if platform frequency is at 400 MHz.
- 22. These pins require 4.7-kΩ pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
- 23. This output is actively driven during reset rather than being tri-stated during reset.
- 24 These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 25. This pin should NOT be pulled down (or driven low) during reset.
- 26. These are test signals for factory use only and must be pulled up (100- Ω to 1- k Ω) to OVDD for normal machine operation.
- 27. Dn_MDIC[0] should be connected to ground with an 18-Ω resistor +/- 1-Ω and Dn_MDIC[1] should be connected Dn_GVDD with an 18-Ω resistor +/- 1-Ω. These pins are used for automatic calibration of the DDR IOs.
- 28. Pin N18 is recommended as a reference point for determining the voltage of V_{DD}_PLAT and is hence considered as the V_{DD}_PLAT sensing voltage and is called SENSEVDD_PLAT.
- 29. Pin P18 is recommended as the ground reference point for SENSEVDD_PLAT and is called SENSEVSS_PLAT.
- 30. This pin should be pulled to ground with a 200- Ω resistor.
- 31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
- 32. Must be tied low if unused
- 33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull up/down option to allow flexibility of future designs.
- 34. Used as serial data output for SRIO 1x/4x link.
- 35. Used as serial data input for SRIO 1x/4x link.
- 36. This pin requires an external 4.7-kΩ pull-down resistor to pevent PHY from seeing a valid Transmit Enable before it is actively driven.



Table 65. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Мах		
Memory bus clock frequency	200	300	MHz	1, 2

Notes:

1. Caution: The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.

2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 66.	Platform/MPX	bus Clocking	Specifications	

	Maximum Processor Core Frequency		Unit	Notes
Characteristic	1000, 1250, 1333, 1500MHz			
	Min	Мах		
Platform/MPX bus clock frequency	400	500-600	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.

2. Platform/MPX frequencies between 400 and 500 MHz are not supported.

Table 67. Local Bus Clocking Specifications

	Maximum Processor Core Frequency		Unit	Notes
Characteristic	1000, 1250, 1333, 1500MHz			
	Min	Мах		
Local bus clock speed (for Local Bus Controller)	25	133	MHz	1

Notes:

1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCRR[CLKDIV]. See the reference manual for the MPC8641D for more information on this.

18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 68:

• SYSCLK input signal



• Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

|--|

18.3 e600 to MPX clock PLL Ratio

Table 69 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 69.

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

Table 69. e600 Core to MPX Clock Ratio

18.4 Frequency Options



System Design Information

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
- 2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
- 3. The local bus PLL generates the clock for the local bus.
- 4. There are two internal PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.



Figure 63. MPC8641 PLL Power Supply Filter Circuit (for platform and Local Bus)



System Design Information

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n \text{ RX}}[7:0]$
- SD*n*_REF_CLK
- SDn_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = $0xE_0F08$) and SRDS2CR1[0:7] register (offset = $0xE_0F44$.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 k Ω is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/LSDWE, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 k Ω) to OVDD

LSSD_MODE, TEST_MODE[0:3]. The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100- Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200- Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-k Ω pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and SENSEV_{DD}_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for SENSEV_{SS}_Core1 and needs to be connected to ground with a weak (2-10 k Ω) pull down resistor. Likewise, AV_{DD}_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."



Table 75 shows the parts that are available for ordering and their operating conditions.

Part Offerings ¹	Operating Conditions
MC8641Dxx1500KX	Dual core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641Dxx1333JX	Dual core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641Dxx1250HX	Dual core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641Dxx1000GX	Dual core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641Dxx1000NX	Dual core MAX CPU speed = 1000 MHz, MAX DDR = 500 MHz Core Voltage = 0.95 volts
MC8641xx1500KX	Single core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641xx1333JX	Single core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641xx1250HX	Single core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641xx1000HX	Single core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641xx1000NX	Single core Max CPU speed = 1000 MHz, Max DDR = 500 MHz Core Voltage = 0.95 volts

Table 75. Part Offerings and Operating Conditions

Note that the "xx" in the part marking represents the package option. The upper case "X" represents the revision letter. For more information see Table 74.

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