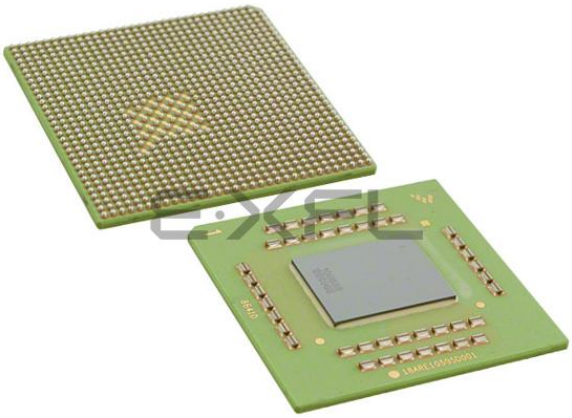

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641hx1000ge

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.50	V	—
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	40	μA	1, 2,3

Timing diagrams for FIFO appear in Figure 8 and Figure 9.

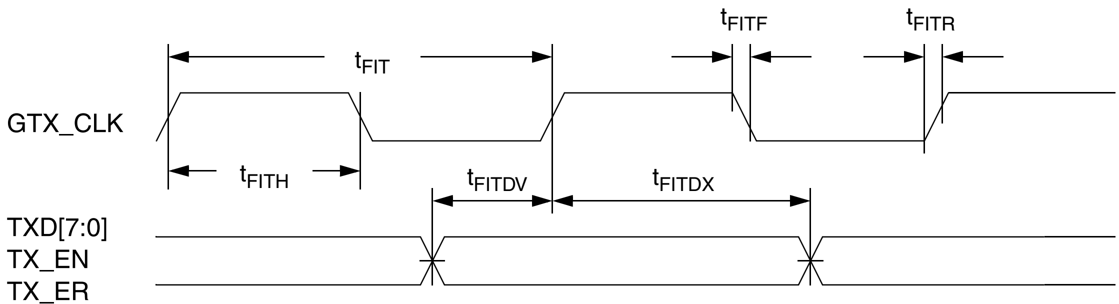

Figure 8. FIFO Transmit AC Timing Diagram

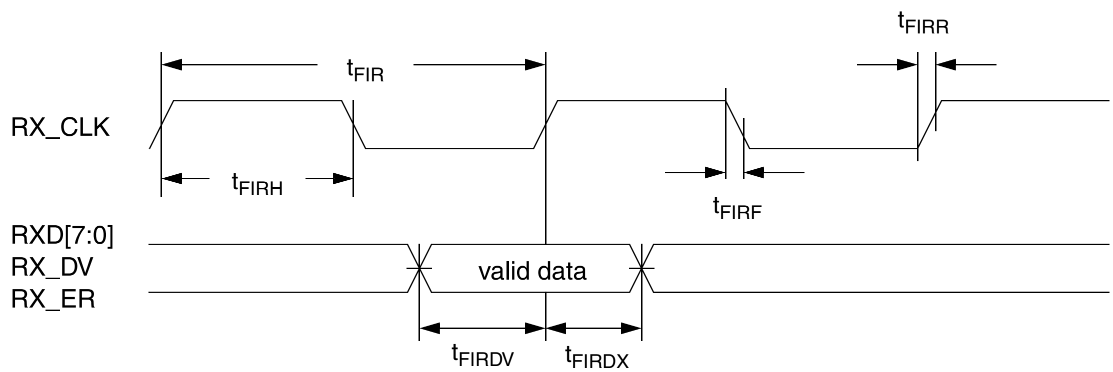

Figure 9. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 28 provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}[2]	—	—	1.0	ns

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

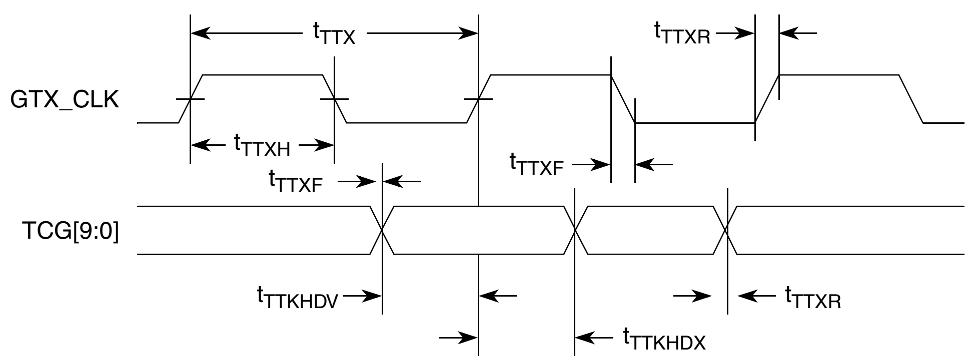

Figure 16. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}[3]	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.

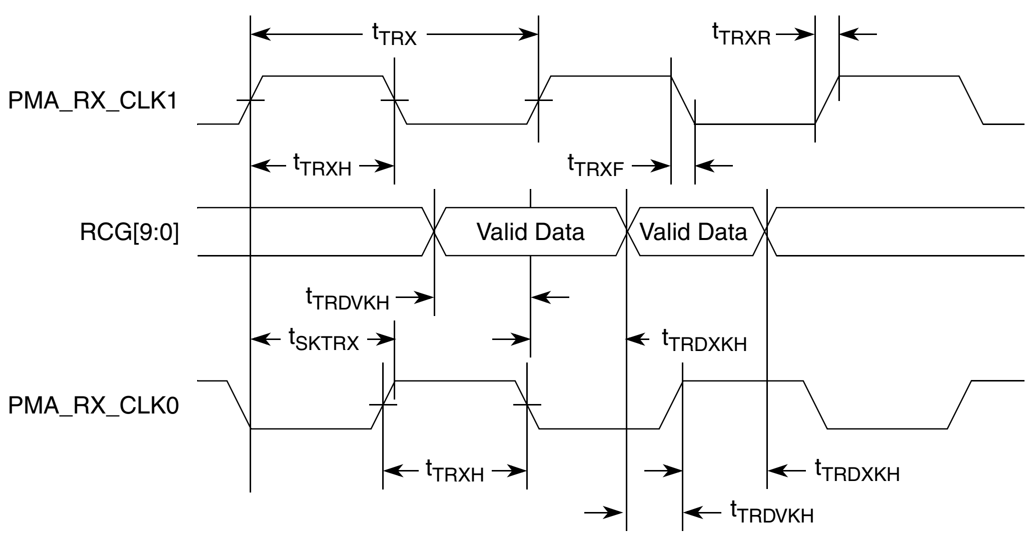

Figure 17. TBI Receive AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}/t_{RMR}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 21 provides the AC test load for eTSEC.

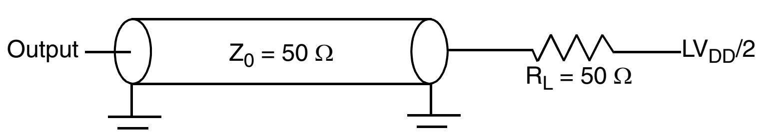

Figure 21. eTSEC AC Test Load

Figure 22 shows the RMII receive AC timing diagram.

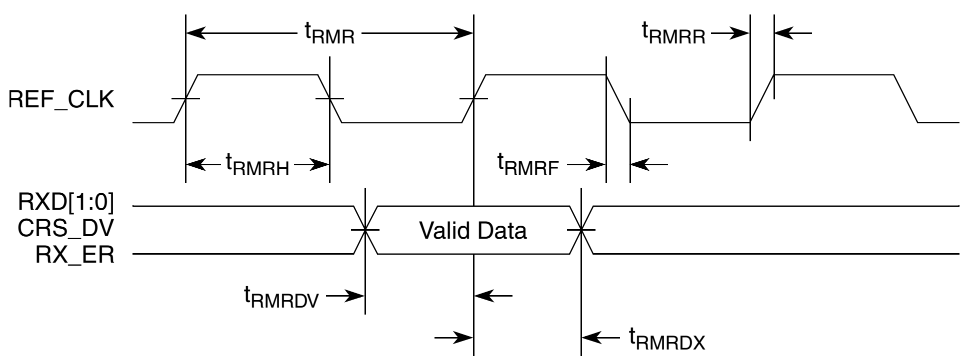

Figure 22. RMII Receive AC Timing Diagram

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

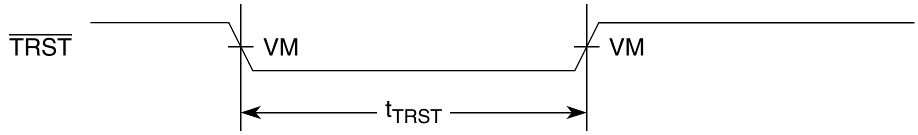

Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

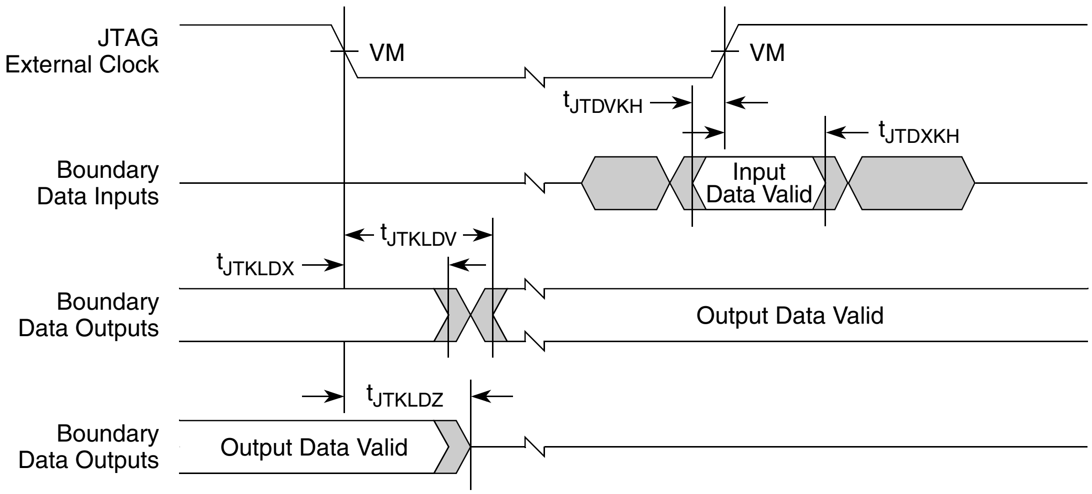

Figure 35. Boundary-Scan Timing Diagram

12 I^{2}C

This section describes the DC and AC electrical characteristics for the I^{2}C interfaces of the MPC8641.

12.1 I^{2}C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I^{2}C interfaces.

Table 45. I^{2}C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3

14.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.175	—	—	V	$V_{RX\text{-}DIFFp\text{-}p} = 2*\|V_{RX\text{-}D+} - V_{RX\text{-}D-}\|$ See Note 2.
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER} = 1 - T_{RX\text{-}EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX\text{-}CM\text{-}ACp} = \|V_{RXD+} - V_{RXD-}\|/2 - V_{RX\text{-}CM\text{-}DC}$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\|V_{RX\text{-}D+} - V_{RX\text{-}D-}\|/2$ See Note 2
$RL_{RX\text{-}DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4
$RL_{RX\text{-}CM}$	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
$Z_{RX\text{-}DC}$	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D– DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical Idle Detect Threshold	65	—	—	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*\|V_{RX\text{-}D+} - V_{RX\text{-}D-}\|$ Measured at the package pins of the Receiver

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see Figure 52). Note that the series capacitors, C_{TX}, are optional for the return loss measurement.

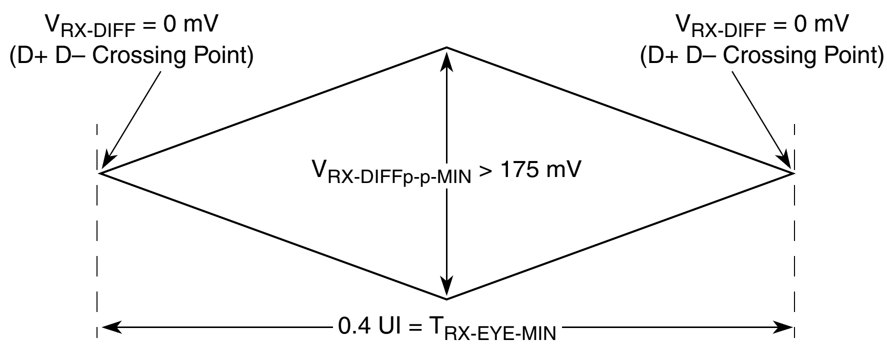

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 57. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 54 with the parameters specified in Table 58 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

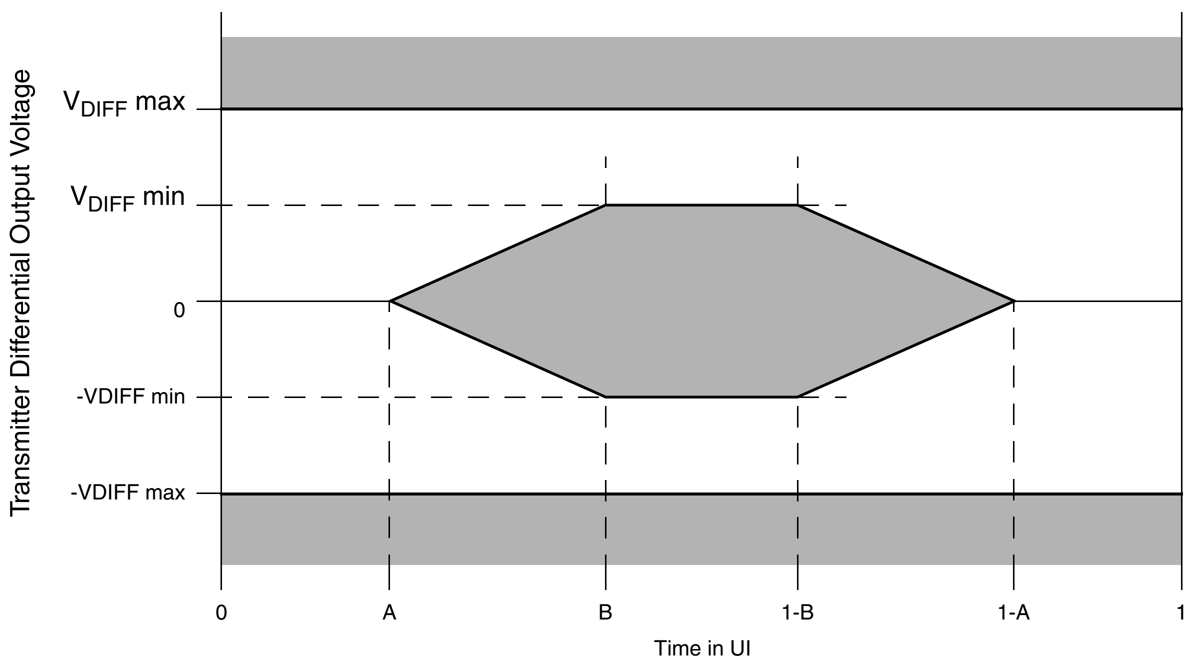

Figure 54. Transmitter Output Compliance Mask

Table 60. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 61. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

16.2 Mechanical Dimensions of the MPC8641 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the MPC8641D (dual core) and MPC8641 (single core) high-lead FC-CBGA (package option: HCTE HX) and lead-free FC-CBGA (package option: HCTE VU) are shown respectfully in Figure 57 and Figure 58.

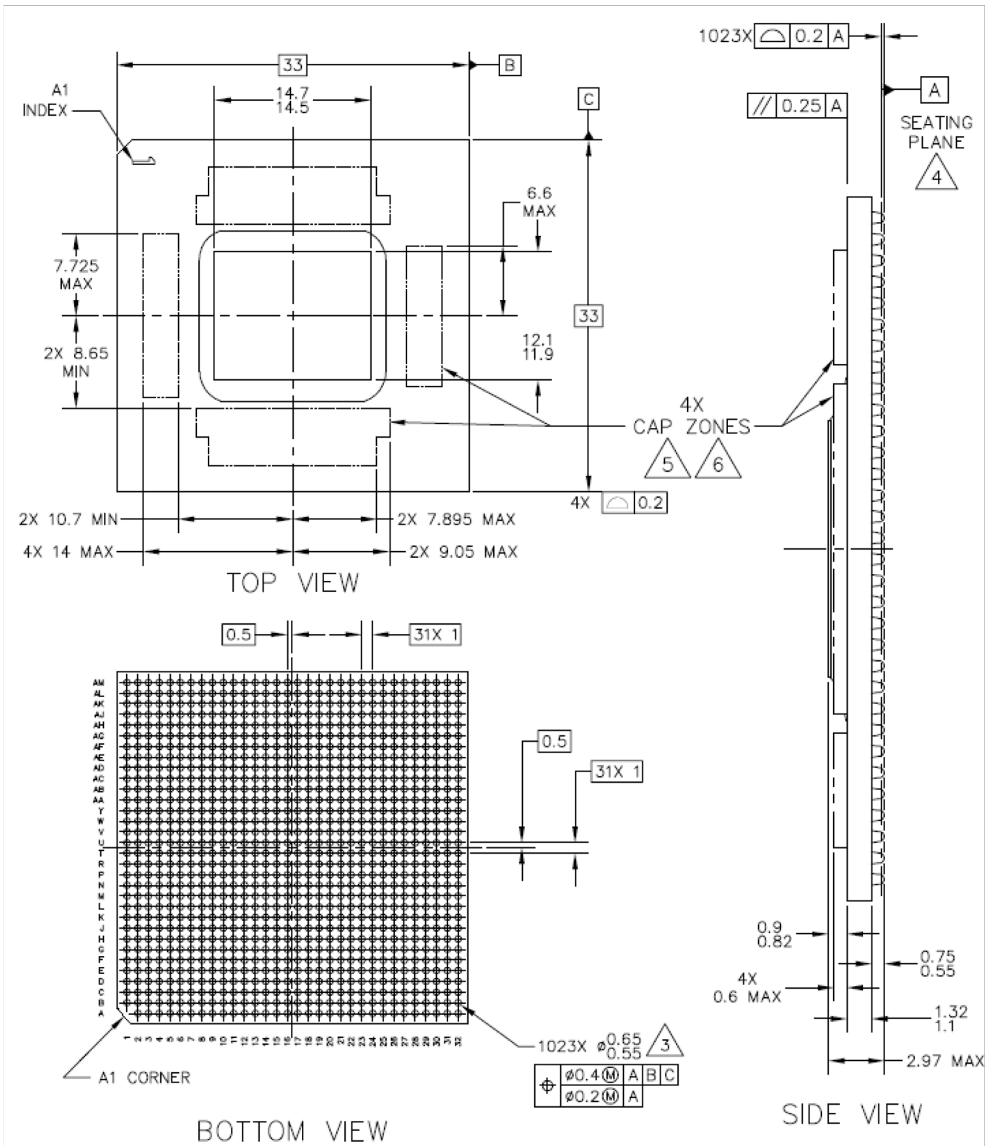

Figure 57. MPC8641D High-Head FC-CBGA Dimensions

NOTES for Figure 57

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.

17 Signal Listings

Table 63 provides the pin assignments for the signals. Notes for the signal changes on the single core device (MPC8641) are italicized and prefixed by *"S"*.

Table 63. MPC8641 Signal Reference by Functional Block

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Interface 1 Signals[2,3]				
D1_MDQ[0:63]	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17	I/O	D1_GV_{DD}	—
D1_MECC[0:7]	M8, M7, R8, T10, L11, L10, P9, R10	I/O	D1_GV_{DD}	—
D1_MDM[0:8]	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10	O	D1_GV_{DD}	—
D1_MDQS[0:8]	A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9	I/O	D1_GV_{DD}	—
$\overline{\text{D1\_MDQS}}$[0:8]	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	D1_GV_{DD}	—
D1_MBA[0:2]	AA8, AA10, T9	O	D1_GV_{DD}	—
D1_MA[0:15]	Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6	O	D1_GV_{DD}	—
$\overline{\text{D1\_MWE}}$	AB11	O	D1_GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	AB12	O	D1_GV_{DD}	—
$\overline{\text{D1\_MCAS}}$	AC10	O	D1_GV_{DD}	—
$\overline{\text{D1\_MCS}}$[0:3]	AB9, AD10, AC12, AD11	O	D1_GV_{DD}	—
D1_MCKE[0:3]	P7, M10, N8, M11	O	D1_GV_{DD}	23
D1_MCK[0:5]	W6, E13, AH11, Y7, F14, AG10	O	D1_GV_{DD}	—
$\overline{\text{D1\_MCK}}$[0:5]	Y6, E12, AH12, AA7, F13, AG11	O	D1_GV_{DD}	—
D1_MODT[0:3]	AC9, AF12, AE11, AF10	O	D1_GV_{DD}	—
D1_MDIC[0:1]	E15, G14	IO	D1_GV_{DD}	27
D1_MV_{REF}	AM18	DDR Port 1 reference voltage	D1_GV_{DD} /2	3
DDR Memory Interface 2 Signals[2,3]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*	—	—
Reset Configuration Signals[20]				
TSEC1_TXD[0] / $\overline{\text{cfg\_alt\_boot\_vec}}$	AF25	—	LV_{DD}	—
TSEC1_TXD[1]/ cfg_platform_freq	AC23	—	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	—	LV_{DD}	—
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	—	LV_{DD}	—
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV_{DD}	—
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV_{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	—	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	—	LV_{DD}	—
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV_{DD}	—
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	—
TSEC3_TXD[3]/ $\overline{\text{cfg\_core1\_lm\_offset}}$	AJ20	—	LV_{DD}	—
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	—	LV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

Note:

1. Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.
3. If a DDR port is not used, it is possible to leave the related power supply (Dn_GVDD, Dn_MVREF) turned off at reset. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.
4. Low Voltage Differential Signaling (LVDS) type pins.
5. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
6. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
7. Recommend a weak pull-up resistor (1–10 kΩ) be placed from this pin to its power supply.
8. Recommend a weak pull-down resistor (2–10 kΩ) be placed from this pin to ground.
9. This multiplexed pin has input status in one mode and output in another
10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
11. This pin is open drain signal.
12. Functional only on the MPC8641D.
13. These pins should be left floating.
14. These pins should be connected to SV_{DD}.
15. These pins should be pulled to ground with a strong resistor (270-Ω to 330-Ω).
16. These pins should be connected to OVDD.
17. This is a SerDes PLL/DLL digital test signal and is only for factory use.
18. This is a SerDes PLL/DLL analog test signal and is only for factory use.
19. This pin should be pulled to ground with a 100-Ω resistor.
20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
21. Should be pulled down at reset if platform frequency is at 400 MHz.
22. These pins require 4.7-kΩ pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
23. This output is actively driven during reset rather than being tri-stated during reset.
24 These JTAG pins have weak internal pull-up P-FETs that are always enabled.
25. This pin should NOT be pulled down (or driven low) during reset.
26. These are test signals for factory use only and must be pulled up (100-Ω to 1- kΩ.) to OVDD for normal machine operation.
27. Dn_MDIC[0] should be connected to ground with an 18-Ω resistor +/– 1-Ω and Dn_MDIC[1] should be connected Dn_GVDD with an 18-Ω resistor +/– 1-Ω. These pins are used for automatic calibration of the DDR IOs.
28. Pin N18 is recommended as a reference point for determining the voltage of V_{DD}_PLAT and is hence considered as the V_{DD}_PLAT sensing voltage and is called SENSEVDD_PLAT.
29. Pin P18 is recommended as the ground reference point for SENSEVDD_PLAT and is called SENSEVSS_PLAT.
30. This pin should be pulled to ground with a 200-Ω resistor.
31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
32. Must be tied low if unused
33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull up/down option to allow flexibility of future designs.
34. Used as serial data output for SRIO 1x/4x link.
35. Used as serial data input for SRIO 1x/4x link.
36. This pin requires an external 4.7-kΩ pull-down resistor to pevent PHY from seeing a valid Transmit Enable before it is actively driven.

example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC} = 0.1$, and a typical power consumption (P_d) of 43.4 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 43.4\ W$

For this example, a $R_{\theta sa}$value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of Table 2.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8641 thermal model is shown in Figure 62. Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See Section 3, "Power Characteristics" for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

Conductivity	Value	Unit
Die (12.4x15.3x0.86 mm)		
Silicon	Temperature dependent	
Bump and Underfill (12.4 × 15.3 × 0.07 mm) Collapsed Resistance		
k_z	5.3	W/(m • K)
Substrate (33 × 33 × 1.2 mm)		
k_x	13.5	W/(m • K)
k_y	13.5	
k_z	5.3	
C5 Solder layer (33 × 33 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	9.6	

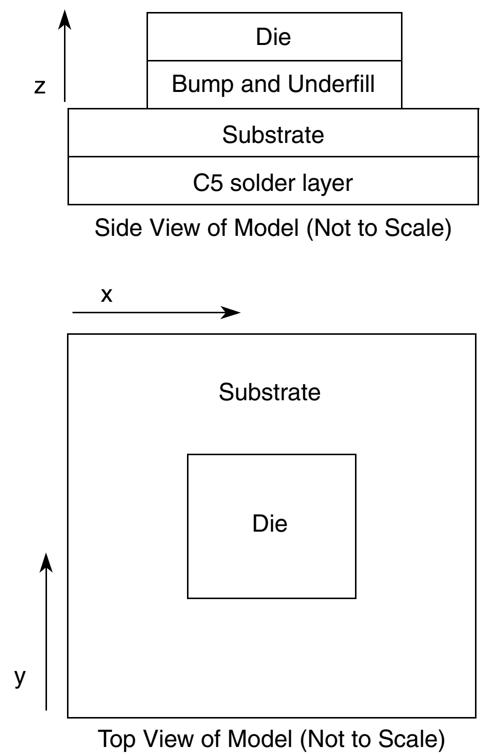

Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Local Bus - If parity is not used, tie LDP[0:3] to ground via a 4.7 kΩ resistor, tie LPBSE to OV_{DD} via a 4.7 kΩ resistor (pull-up resistor). For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

SerDes - Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 20.5.1, "Guidelines for High-Speed Interface Termination."

20.5.1 Guidelines for High-Speed Interface Termination

20.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:3] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 72 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 72. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference Clock not required)	SerDes port is enabled Partial termination may be required[1] (Reference Clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference Clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input[2] (Reference Clock is required)

Notes:

1 Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in x8 PCI Express mode, no termination is required because all pins are being used. If the port is in x1/x2/x4 PCI Express mode, termination is required on the unused pins. If the port is in x4 Serial RapidIO mode termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 68. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 67 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.