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Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641hx1333je

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T_J	0 to 105	°C	—

Notes:

- Core 1 characteristics apply only to MPC8641D
- If two separate power supplies are used for V_{DD_Core0} and V_{DD_Core1} , they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
- Caution:** Dn_MV_{IN} must meet the overshoot/undershoot requirements for Dn_GV_{DD} as shown in [Figure 2](#).
- Caution:** L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in [Figure 2](#) during regular run time.
- Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in [Figure 2](#) during regular run time.
- Timing limitations for $M,L,T,O)V_{IN}$ and Dn_MV_{REF} during regular run time is provided in [Figure 2](#)
- Applies to devices marked with a core frequency of 1333 MHz and below. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
- Applies to devices marked with a core frequency above 1333 MHz. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
- The 2.5 V \pm 125 mV range is for DDR and 1.8 V \pm 90 mV range is for DDR2.
- See [Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,”](#) for details on the recommended operating conditions per protocol.
- The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to [Section 14.4.3, “Differential Receiver \(RX\) Input Specifications.”](#)
- Applies to Part Number MC8641xxx1000NX only. $V_{DD_Coren} = 0.95$ V and $V_{DD_PLAT} = 1.05$ V devices. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for $V_{DD_Coren} = 0.95$ V.
- This voltage is the input to the filter discussed in [Section 20.2, “Power Supply Design and Sequencing,”](#) and not necessarily the voltage at the AV_{DD_Coren} pin, which may be reduced from V_{DD_Coren} by the filter.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 2.5\text{ V}$	4, 9
DDR2 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 1.8\text{ V}$	1, 5, 9
Local Bus signals	45 25	$OV_{DD} = 3.3\text{ V}$	2, 6
eTSEC/10/100 signals	45	$T/LV_{DD} = 3.3\text{ V}$	6
	30	$T/LV_{DD} = 2.5\text{ V}$	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage	45	$OV_{DD} = 3.3\text{ V}$	6
I ² C	150	$OV_{DD} = 3.3\text{ V}$	7
SRIO, PCI Express	100	$SV_{DD} = 1.1/1.05\text{ V}$	3, 8

Notes:

1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω . See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See [Section 17, "Signal Listings,"](#) for details on resistor requirements for the calibration of $SDn_IMP_CAL_TX$ and $SDn_IMP_CAL_RX$ transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at $T_j = 105^\circ\text{C}$ and at Dn_GV_{DD} (min).

2.2 Power Up/Down Sequence

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

NOTE

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is as follows:

1. All power rails other than DDR I/O (Dn_GV_{DD} , and Dn_MV_{REF}).

The maximum power dissipation for individual power supplies of the MPC8641D is shown in [Table 5](#).

Table 5. MPC8641D Individual Supply Maximum Power Dissipation ¹

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 1.1 \text{ V @ } 1500 \text{ MHz}$	21.00	
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 1.1 \text{ V @ } 1500 \text{ MHz}$	0.0125	
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 1.05 \text{ V @ } 1333 \text{ MHz}$	17.00	
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 1.05 \text{ V @ } 1333 \text{ MHz}$	0.0125	
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 0.95 \text{ V @ } 1000 \text{ MHz}$	11.50	5
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 0.95 \text{ V @ } 1000 \text{ MHz}$	0.0125	5
DDR Controller I/O voltage supply	$Dn_GV_{DD} = 2.5 \text{ V @ } 400 \text{ MHz}$	0.80	2
	$Dn_GV_{DD} = 1.8 \text{ V @ } 533 \text{ MHz}$	0.68	2
	$Dn_GV_{DD} = 1.8 \text{ V @ } 600 \text{ MHz}$	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	$L/TV_{DD} = 3.3 \text{ V}$	0.11	2, 3
non-FIFO eTsecn Voltage Supply	$L/TV_{DD} = 3.3 \text{ V}$	0.08	2
x8 SerDes transceiver Supply	$SV_{DD} = 1.1 \text{ V}$	0.70	2
x8 SerDes I/O Supply	$XV_{DD_SRDSn} = 1.1 \text{ V}$	0.66	2
SerDes PLL voltage supply Port 1 or 2	$AV_{DD_SRDS1}/AV_{DD_SRDS2} = 1.1 \text{ V}$	0.10	
Platform I/O Supply	$OV_{DD} = 3.3 \text{ V}$	0.45	4
Platform source Supply	$V_{DD_PLAT} = 1.1 \text{ V @ } 600 \text{ MHz}$	12.00	
Platform source Supply	$V_{DD_PLAT} = 1.05 \text{ Vn @ } 500 \text{ MHz}$	9.80	5
Platform source Supply	$V_{DD_PLAT} = 1.05 \text{ Vn @ } 400 \text{ MHz}$	7.70	
Platform, Local Bus PLL voltage Supply	$AV_{DD_PLAT}, AV_{DD_LB} = 1.1 \text{ V}$	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I²C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. $V_{DD_Coren} = 0.95 \text{ V}$ and $V_{DD_PLAT} = 1.05 \text{ V}$.

Table 10. EC_n_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC _n _GTX_CLK125 duty cycle	t _{G125H} /t _{G125}		—		%	1, 2
GMII, TBI		45		55		
1000Base-T for RGMII, RTBI		47		53		

Notes:

- Timing is guaranteed by design and characterization.
- EC_n_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation.
EC_n_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See [Section 8.2.6, “RGMII and RTBI AC Timing Specifications,”](#) for duty cycle for 10Base-T and 100Base-T reference clock.
- ±100 ppm tolerance on EC_n_GTX_CLK125 frequency

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527 \text{ MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg_plat_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when $Dn_GV_{DD}(typ) = 2.5\text{ V}$.

Table 15. DDR SDRAM DC Electrical Characteristics for $Dn_GV_{DD} (typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	2.375	2.625	V	1
I/O reference voltage	Dn_MV_{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$Dn_MV_{REF} - 0.04$	$Dn_MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$Dn_MV_{REF} + 0.15$	$Dn_GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$Dn_MV_{REF} - 0.15$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	16.2	—	mA	—

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF} . This rail should track variations in the DC level of Dn_MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq Dn_GV_{DD}$.

Table 16 provides the DDR capacitance when $Dn_GV_{DD} (typ) = 2.5\text{ V}$.

Table 16. DDR SDRAM Capacitance for $Dn_GV_{DD} (typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV_{REF} .

Table 17. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current ($V_{IN} = GND$)	I_{IL}	-600	—	μA	³

Notes:

- ¹ LV_{DD} supports eTSECs 1 and 2.
- ² TV_{DD} supports eTSECs 3 and 4.
- ³ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#) and [Table 2](#).

Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1,2
Output high voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.00	—	V	—
Output low voltage ($LV_{DD}/TV_{DD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	—	0.40	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	10	μA	1, 2,3
Input low current ($V_{IN} = GND$)	I_{IL}	-15	—	μA	³

Note:

- ¹ LV_{DD} supports eTSECs 1 and 2.
- ² TV_{DD} supports eTSECs 3 and 4.
- ³ Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 1](#) and [Table 2](#).

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSECn's $TSECn_TX_CLK$, while the receive clock must be applied to pin $TSECn_RX_CLK$. The eTSEC internally uses the transmit

8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	$t_{MRX}^{2,3}$	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}^3	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time (20%-80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}^2	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.
- ± 100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.

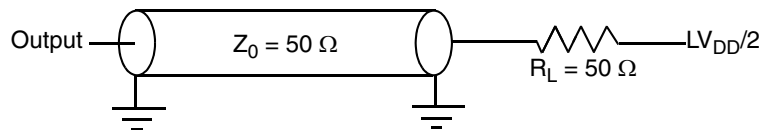


Figure 14. eTSEC AC Test Load

Figure 15 shows the MII receive AC timing diagram.

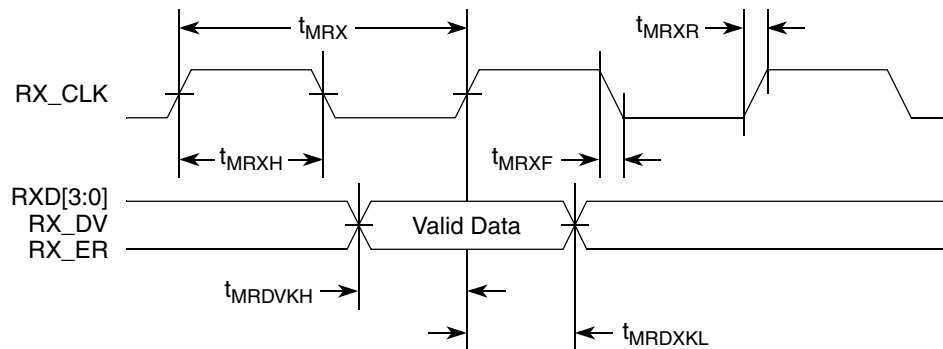


Figure 15. MII Receive AC Timing Diagram

Table 39. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. t_{MPXCLK} is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.

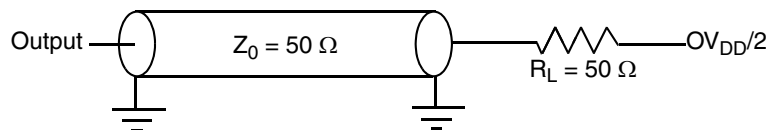


Figure 23. eTSEC AC Test Load

NOTE

Output will see a 50-Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.

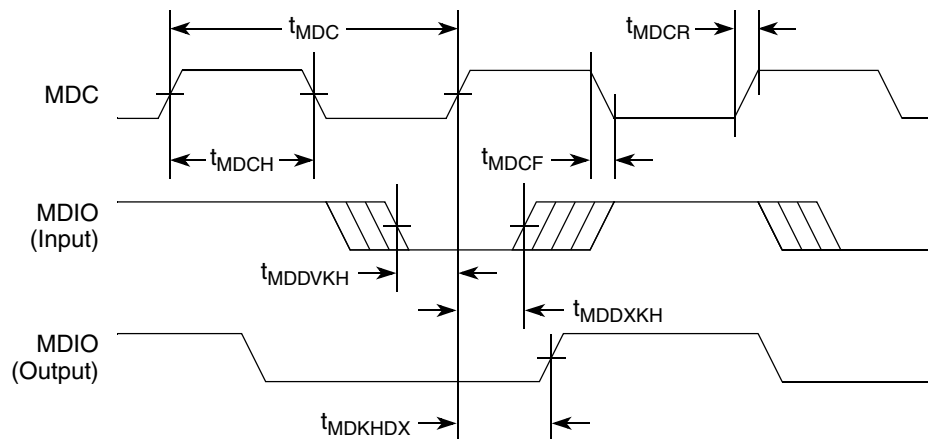


Figure 24. MII Management Interface Timing Diagram

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8641/D.

11.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = V_{DD}$)	I_{IN}	—	± 5	μA
High-level output voltage ($OV_{DD} = \min$, $I_{OH} = -100$ μA)	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage ($OV_{DD} = \min$, $I_{OL} = 100$ μA)	V_{OL}	—	0.2	V

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

11.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 35.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) ¹

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
\overline{TRST} assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	— —		4
Valid times:				ns	
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25		5

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{\text{DIFFp-p}}$) is 1000 mV p-p.

13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SDn_REF_CLK and $\overline{\text{SDn_REF_CLK}}$ for PCI Express and Serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $\text{XV}_{\text{DD_SRDSn}}$ are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
 - The SDn_REF_CLK and $\overline{\text{SDn_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SDn_REF_CLK or $\overline{\text{SDn_REF_CLK}}$) has a 50- Ω termination to SGND followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4 \text{ V}/50 = 8 \text{ mA}$) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SDn_REF_CLK and $\overline{\text{SDn_REF_CLK}}$ inputs cannot drive 50 Ω to SGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.

13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3 \text{ UI}$. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0 \text{ V}$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D– TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(IV_{TXD+} + V_{TXD-}/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$ V_{TX-CM-DC} \text{ (during L0)} - V_{TX-CM-DC} \text{ (During Electrical Idle)} \leq 100 \text{ mV}$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2 \text{ [L0]}$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2 \text{ [Electrical Idle]}$ See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25 \text{ mV}$ $V_{TX-CM-DC-D+} = DC_{(avg)} \text{ of } IV_{TXD+}$ $V_{TX-CM-DC-D-} = DC_{(avg)} \text{ of } IV_{TXD-}$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = IV_{TX-IDLE-D+} - IV_{TX-IDLE-D-} \leq 20 \text{ mV}$ See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

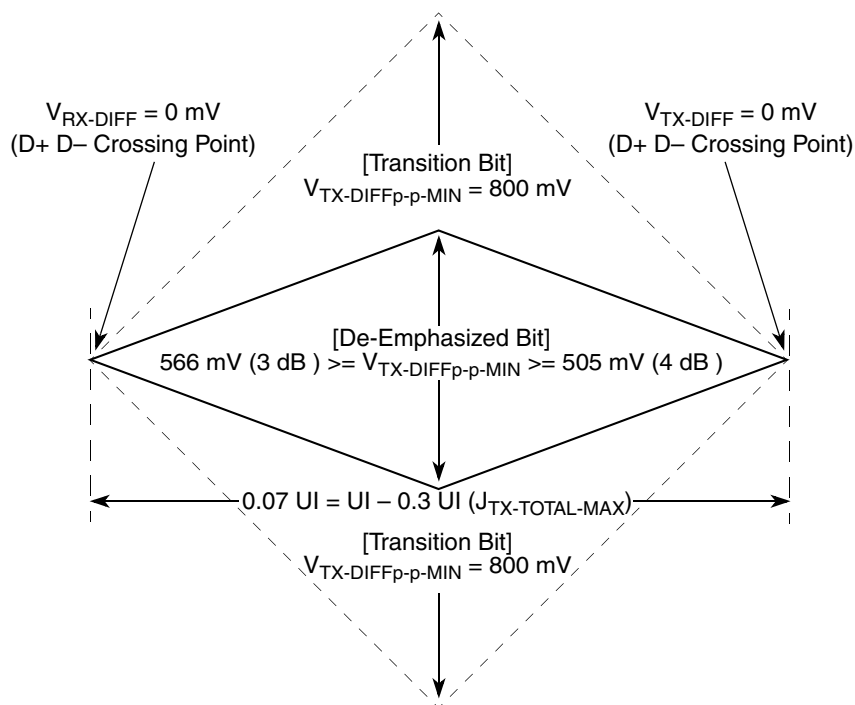


Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications

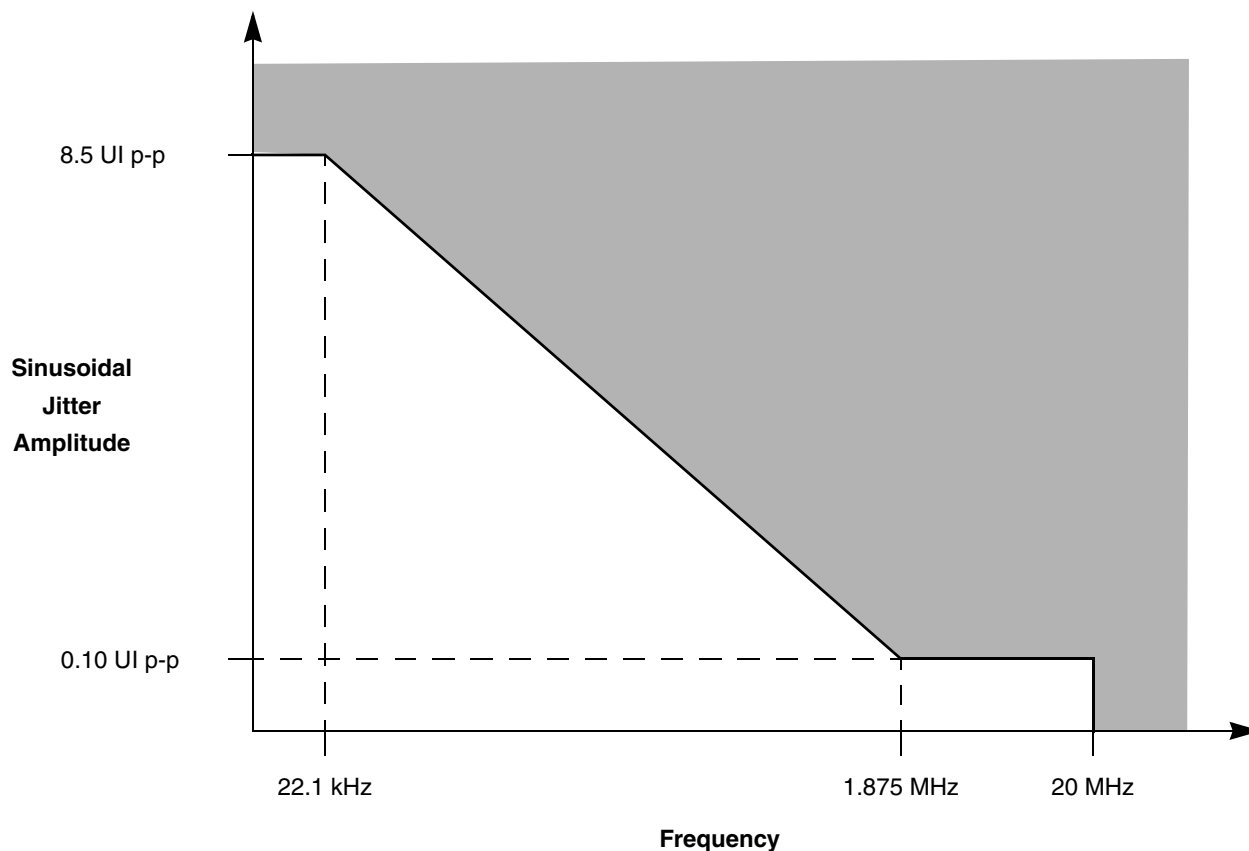


Figure 55. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification ([Table 59](#), [Table 60](#), [Table 61](#)) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in [Figure 56](#) with the parameters specified in [Table](#) . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\ \Omega \pm 5\%$ differential resistive load.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18
SD1_DLL_TPD	N28	O	SV _{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)⁴				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV _{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV _{DD}	34
$\overline{\text{SD2_TX}}[0:3]$	Y25, AA28, AB26, AC28	O	SV _{DD}	—
$\overline{\text{SD2_TX}}[4:7]$	AE28, AG28, AJ28, AL28	O	SV _{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35
$\overline{\text{SD2_RX}}[0:3]$	Y29, AA31, AB29, AC31	I	SV _{DD}	—
$\overline{\text{SD2_RX}}[4:7]$	AH29, AJ31, AK29, AL31	I	SV _{DD}	35
SD2_REF_CLK	AE32	I	SV _{DD}	—
$\overline{\text{SD2_REF_CLK}}$	AE31	I	SV _{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30
SD2_PLL_TPD	AF29	O	SV _{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV _{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals⁵				
EC1_GTX_CLK125	AL23	I	LV _{DD}	39
EC2_GTX_CLK125	AM23	I	TV _{DD}	39
EC_MDC	G31	O	OV _{DD}	—
EC_MDIO	G32	I/O	OV _{DD}	—
eTSEC Port 1 Signals⁵				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	LV _{DD}	6, 10
TSEC1_TX_EN	AB22	O	LV _{DD}	36
TSEC1_TX_ER	AH26	O	LV _{DD}	—
TSEC1_TX_CLK	AC22	I	LV _{DD}	40
TSEC1_GTX_CLK	AH25	O	LV _{DD}	41
TSEC1_CRS	AM24	I/O	LV _{DD}	37
TSEC1_COL	AM25	I	LV _{DD}	—
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV _{DD}	10
TSEC1_RX_DV	AJ24	I	LV _{DD}	—
TSEC1_RX_ER	AJ25	I	LV _{DD}	—
TSEC1_RX_CLK	AK24	I	LV _{DD}	40
eTSEC Port 2 Signals⁵				
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV _{DD}	6, 10
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV _{DD}	6, 10, 38
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV _{DD}	6, 10
TSEC2_TX_EN	AB21	O	LV _{DD}	36
TSEC2_TX_ER	AB19	O	LV _{DD}	6, 38
TSEC2_TX_CLK	AC21	I	LV _{DD}	40
TSEC2_GTX_CLK	AD20	O	LV _{DD}	41
TSEC2_CRS	AE20	I/O	LV _{DD}	37
TSEC2_COL	AE21	I	LV _{DD}	—
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV _{DD}	10
TSEC2_RX_DV	AC19	I	LV _{DD}	—
TSEC2_RX_ER	AD21	I	LV _{DD}	—
TSEC2_RX_CLK	AM22	I	LV _{DD}	40
eTSEC Port 3 Signals⁵				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV _{DD}	6
TSEC3_TXD[4]/	AM19	O	TV _{DD}	—
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV _{DD}	6

- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

Table 68. MPX:SYSCLK Ratio

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

18.3 e600 to MPX clock PLL Ratio

[Table 69](#) describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in [Table 69](#).

Table 69. e600 Core to MPX Clock Ratio

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

18.4 Frequency Options

Tyco Electronics
 Chip Coolers™
 P.O. Box 3668
 Harrisburg, PA 17105-3668
 Internet: www.chipcoolers.com
 Wakefield Engineering
 33 Bridge St.
 Pelham, NH 03076
 Internet: www.wakefield.com

800-522-6752

603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in [Table 71](#), the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

[Figure 60](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

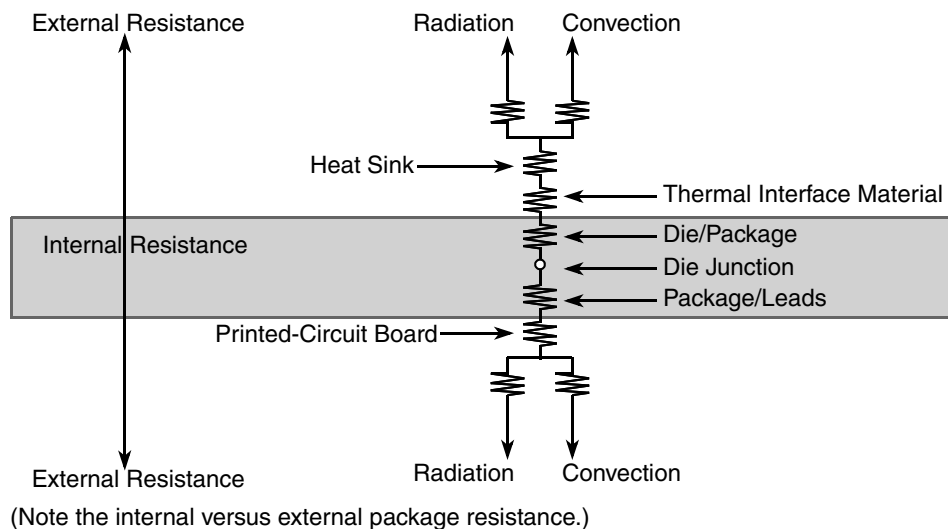


Figure 60. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

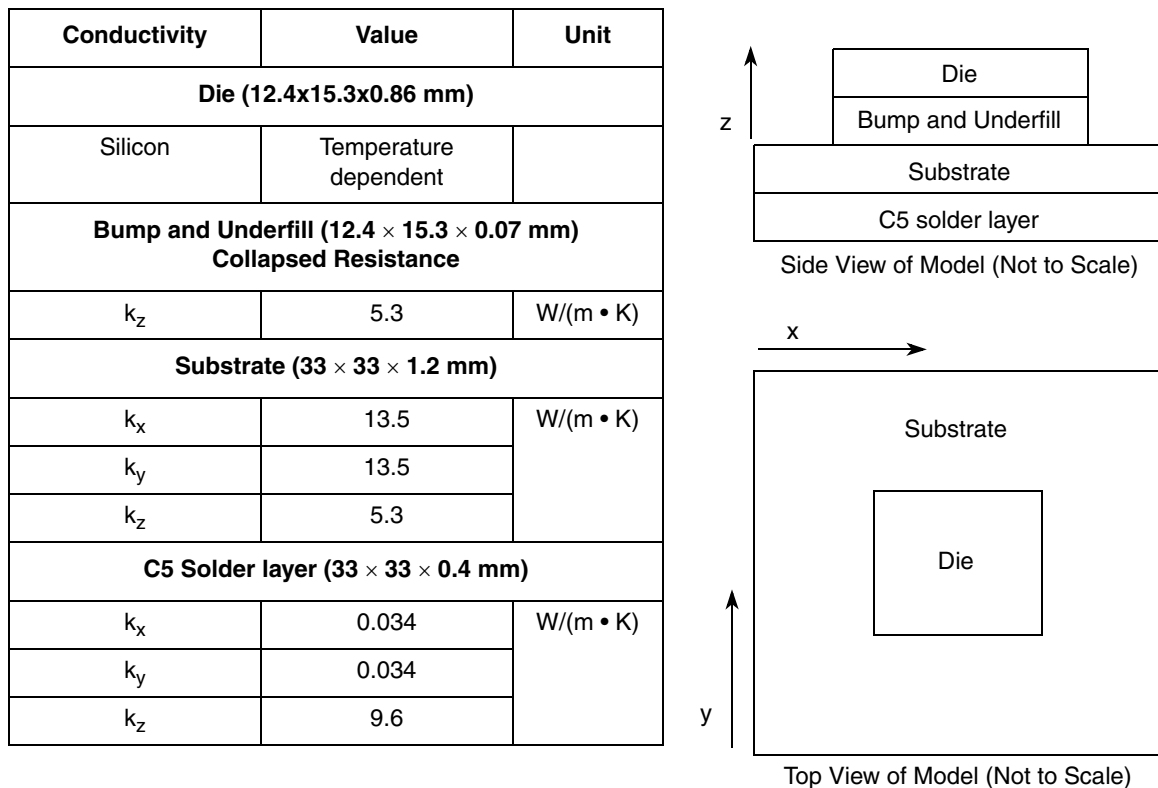


Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

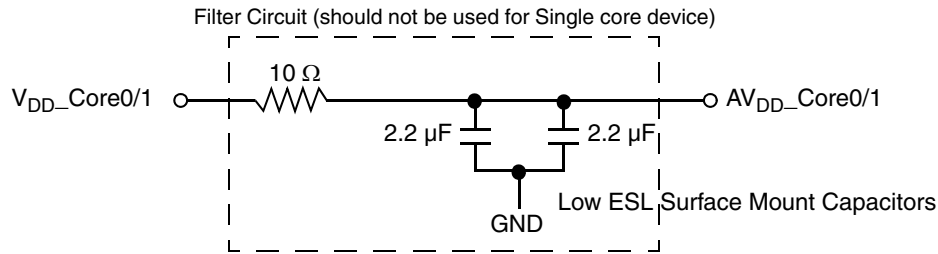
$$V_f > 0.40 \text{ V}$$

$$V_f < 0.90 \text{ V}$$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

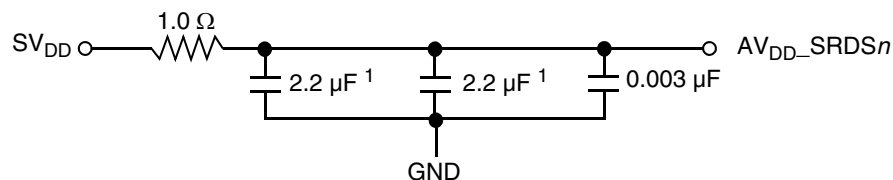
$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$



Note: For single core device the filter circuit (in the dashed box) should be removed and AV_{DD}_Core1 should be tied to ground with a weak (2-10 kΩ) pull-down resistor.

Figure 64. MPC8641 PLL Power Supply Filter Circuit (for cores)

The AV_{DD}_SRDS_n signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS_n balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS_n balls. The 0.003-μF capacitor is closest to the balls, followed by the two 2.2-μF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS_n to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 65. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS_n should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the SV_{DD} power plan.

20.2.2 PLL Power Supply Sequencing

For details on power sequencing for the AV_{DD} type and supplies refer to [Section 2.2, “Power Up/Down Sequence.”](#)

20.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system