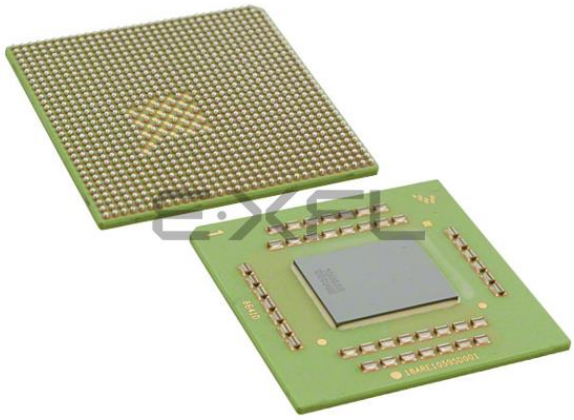

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641hx1500kb

- DDR memory controllers
  - Dual 64-bit memory controllers (72-bit with ECC)
  - Support of up to a 300-MHz clock rate and a 600-MHz DDR2 SDRAM
  - Support for DDR, DDR2 SDRAM
  - Up to 16 Gbytes per memory controller
  - Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification*, Revision 1.2
  - Both 1x and 4x LP-Serial link interfaces
  - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
  - RapidIO–compliant message unit
  - RapidIO atomic transactions to the memory controller
- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports x1, x2, x4, and x8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support of the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
  - Support a full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP off-load
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
  - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
  - RMON statistics support
  - MII management interface for control and status
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts
  - Allows processors to interrupt each other with 32b messages

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Absolute Maximum Value	Unit	Notes
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	– 0.3 to (D*n*_GV_{DD} + 0.3)	V	5
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	– 0.3 to (D*n*_GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to (LV_{DD}+ 0.3) GND to (TV_{DD}+ 0.3)	V	5
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to (OV_{DD}+ 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8641D. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be kept within 100 mV of each other during normal run time.
3. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
4. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
5. During run time (M,L,T,O)V_{IN} and D*n*_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

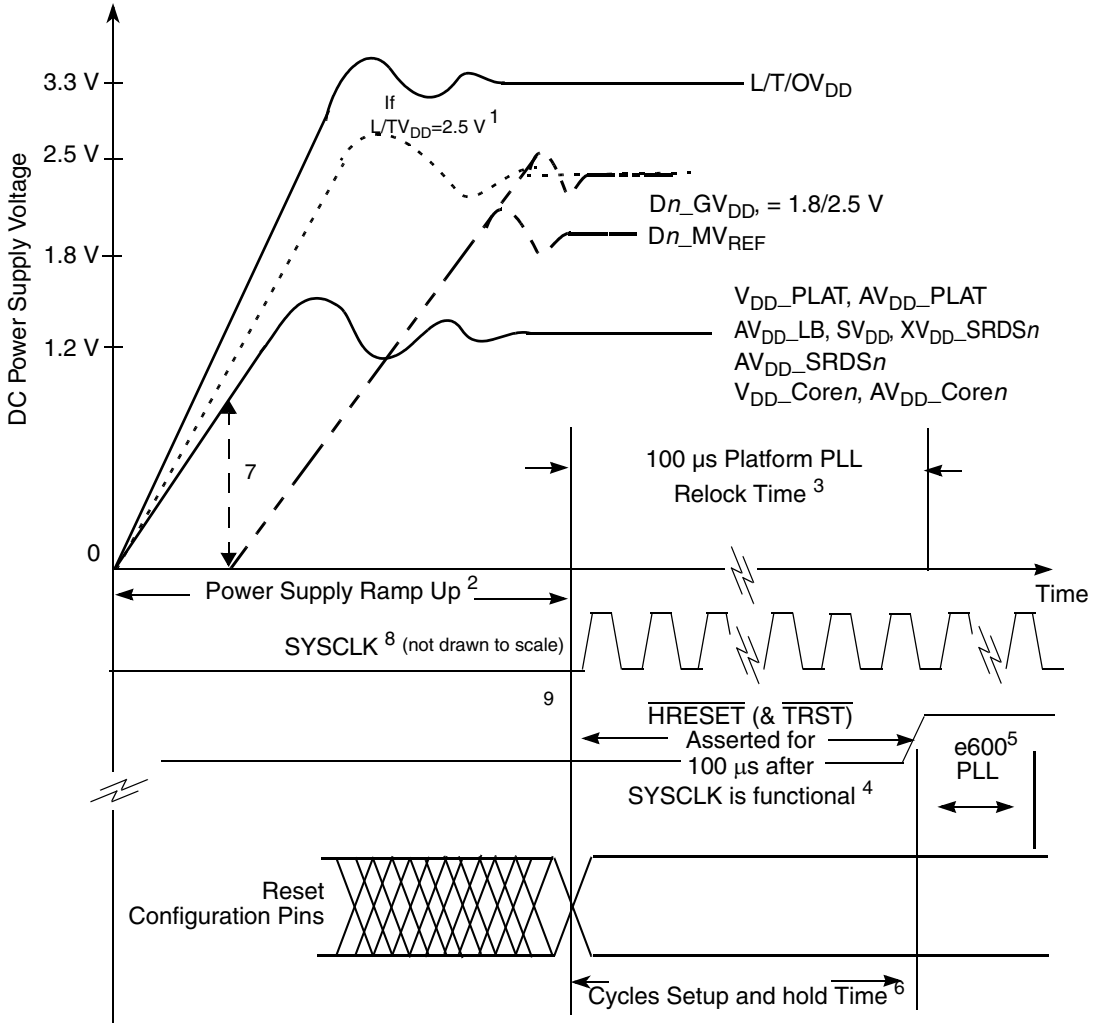
2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8641. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	1.10 ± 50 mV	V	1, 2, 8
		1.05 ± 50 mV		1, 2, 7
		0.95 ± 50 mV		1, 2, 12
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	1.10 ± 50 mV	V	8, 13
		1.05 ± 50 mV		7, 13
		0.95 ± 50 mV		12, 13
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	1.10 ± 50 mV	V	8, 11
		1.05 ± 50 mV		7, 11

Figure 3 illustrates the Power Up sequence as described above.



Notes:

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 2.
2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to Section 5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 11 for additional information on reset configuration pin setup timing requirements. In addition see Figure 68 regarding HRESET and JTAG connection details including TRST.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See Section 5, "RESET Initialization" for more information on setup and hold time of reset configuration signals.
7. V$_{DD}$_PLAT, AV$_{DD}$_PLAT must strictly reach 90% of their recommended voltage before the rail for Dn_GV$_{DD}$, and Dn_MV$_{REF}$ reaches 10% of their recommended voltage.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4],TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

Figure 3. MPC8641 Power-Up and Reset Sequence

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF}+ 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. D*n*_MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 14 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit

Table 29. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

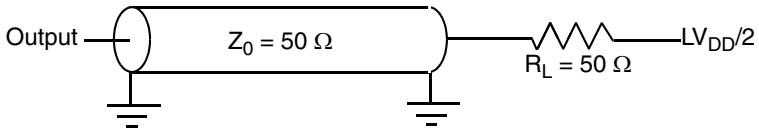


Figure 11. eTSEC AC Test Load

Figure 12 shows the GMII receive AC timing diagram.

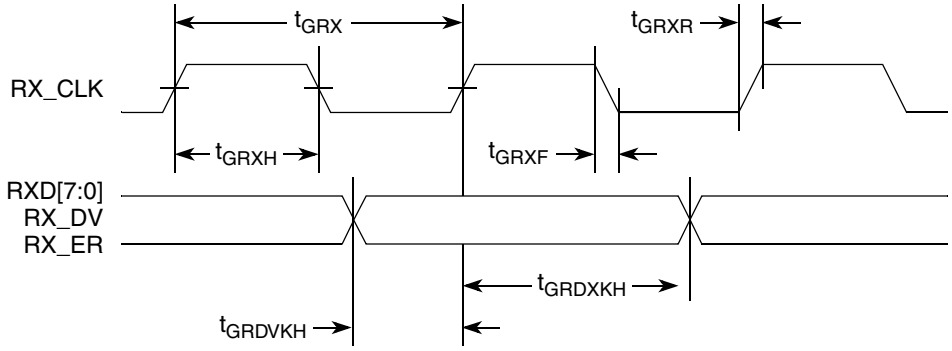


Figure 12. GMII Receive AC Timing Diagram

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock period duration [3]	t_{RGT}[5,6]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

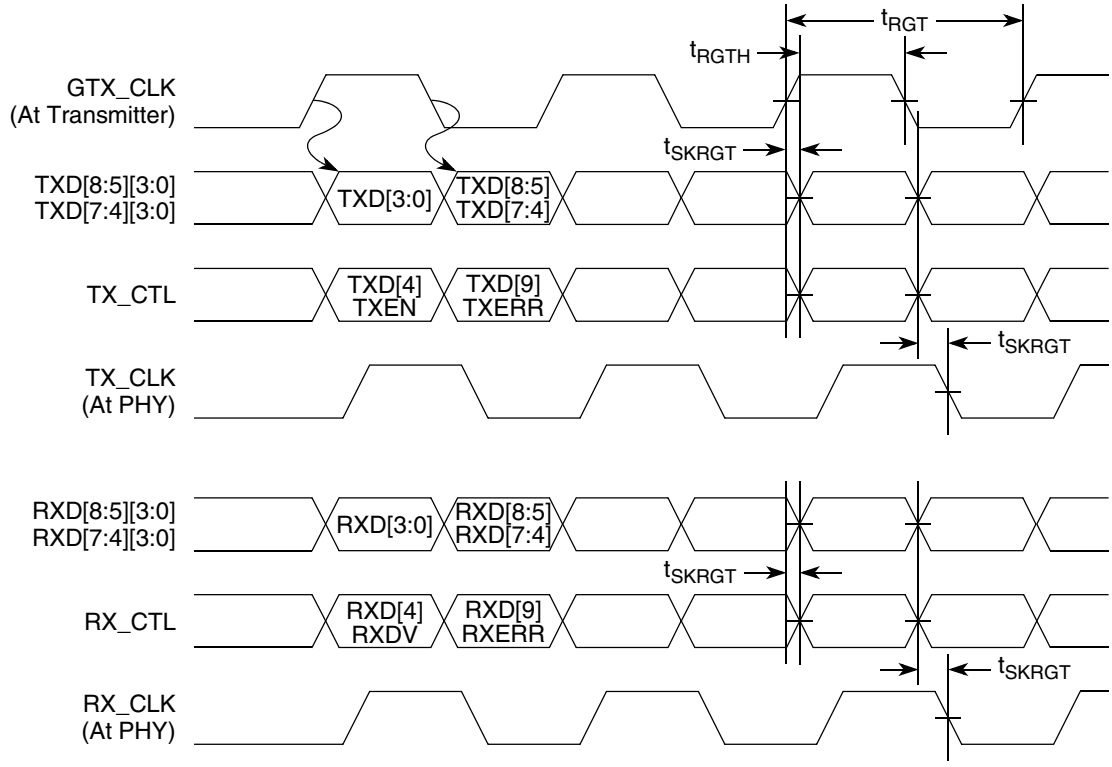


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

Table 38. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	—	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

Table 39. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	9.3	MHz	2, 4
MDC period	t_{MDC}	80	—	400	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16*t_{MPXCLK}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	10	—	$16*t_{MPXCLK}$	ns	3, 5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—

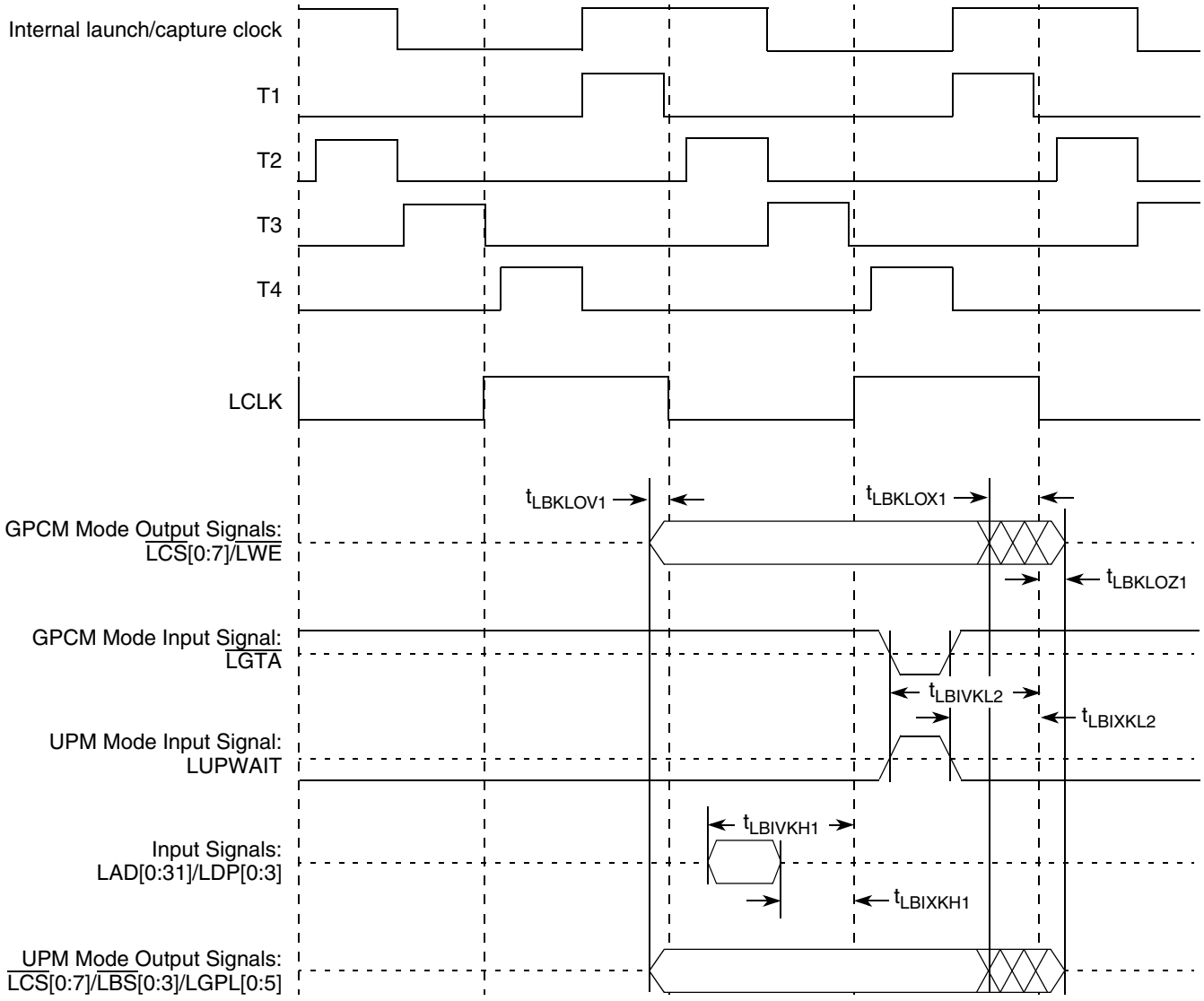


Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	—	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.
$T_{crosslink}$	Crosslink Random Timeout	0	—	—	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. MPC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

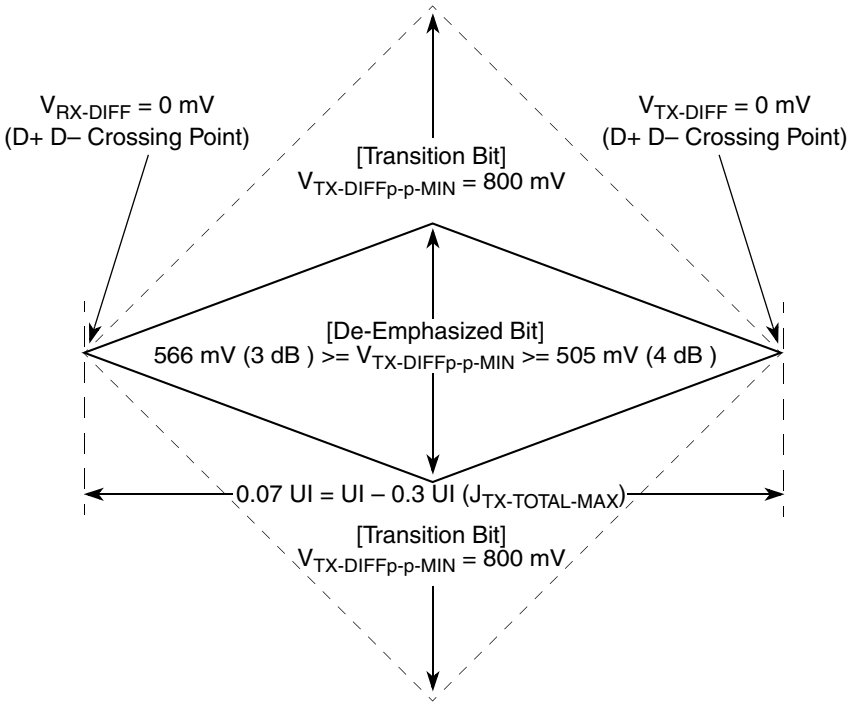


Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D2_MDQ[0:63]	A7, B7, C5, D5, C8, D8, D6, A5, C4, A3, D3, D2, A4, B4, C2, C1, E3, E1, H4, G1, D1, E4, G3, G2, J4, J2, L1, L3, H3, H1, K1, L4, AA4, AA2, AD1, AD2, Y1, AA1, AC1, AC3, AD5, AE1, AG1, AG2, AC4, AD4, AF3, AF4, AH3, AJ1, AM1, AM3, AH1, AH2, AL2, AL3, AK5, AL5, AK7, AM7, AK4, AM4, AM6, AJ7	I/O	$D2\_GV_{DD}$	—
D2_MECC[0:7]	H6, J5, M5, M4, G6, H7, M2, M1	I/O	$D2\_GV_{DD}$	—
D2_MDM[0:8]	C7, B3, F4, J1, AB1, AE2, AK1, AM5, K6	O	$D2\_GV_{DD}$	—
D2_MDQS[0:8]	B6, B1, F1, K2, AB3, AF1, AL1, AL6, L6	I/O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MDQS}}$[0:8]	A6, A2, F2, K3, AB2, AE3, AK2, AJ6, K5	I/O	$D2\_GV_{DD}$	—
D2_MBA[0:2]	W5, V5, P3	O	$D2\_GV_{DD}$	—
D2_MA[0:15]	W1, U4, U3, T1, T2, T3, T5, R2, R1, R5, V4, R4, P1, AH5, P4, N1	O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MWE}}$	Y4	O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MRAS}}$	W3	O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MCAS}}$	AB5	O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MCS}}$[0:3]	Y3, AF6, AA5, AF7	O	$D2\_GV_{DD}$	—
D2_MCKE[0:3]	N6, N5, N2, N3	O	$D2\_GV_{DD}$	23
D2_MCK[0:5]	U1, F5, AJ3, V2, E7, AG4	O	$D2\_GV_{DD}$	—
$\overline{\text{D2\_MCK}}$[0:5]	V1, G5, AJ4, W2, E6, AG5	O	$D2\_GV_{DD}$	—
D2_MODT[0:3]	AE6, AG7, AE5, AH6	O	$D2\_GV_{DD}$	—
D2_MDIC[0:1]	F8, F7	IO	$D2\_GV_{DD}$	27
$D2\_MV_{REF}$	A18	DDR Port 2 reference voltage	$D2\_GV_{DD}$ /2	3
High Speed I/O Interface 1 (SERDES 1)[4]				
SD1_TX[0:7]	L26, M24, N26, P24, R26, T24, U26, V24	O	SV_{DD}	—
$\overline{\text{SD1\_TX}}$[0:7]	L27, M25, N27, P25, R27, T25, U27, V25	O	SV_{DD}	—
SD1_RX[0:7]	J32, K30, L32, M30, T30, U32, V30, W32	I	SV_{DD}	—
$\overline{\text{SD1\_RX}}$[0:7]	J31, K29, L31, M29, T29, U31, V29, W31	I	SV_{DD}	—
SD1_REF_CLK	N32	I	SV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	N31	I	SV_{DD}	—
SD1_IMP_CAL_TX	Y26	Analog	SV_{DD}	19
SD1_IMP_CAL_RX	J28	Analog	SV_{DD}	30
SD1_PLL_TPD	U28	O	SV_{DD}	13, 17

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV_{DD}	13, 18
SD1_DLL_TPD	N28	O	SV_{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV_{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)[4]				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV_{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV_{DD}	34
$\overline{\text{SD2\_TX}}$[0:3]	Y25, AA28, AB26, AC28	O	SV_{DD}	—
$\overline{\text{SD2\_TX}}$[4:7]	AE28, AG28, AJ28, AL28	O	SV_{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV_{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV_{DD}	32, 35
$\overline{\text{SD2\_RX}}$[0:3]	Y29, AA31, AB29, AC31	I	SV_{DD}	—
$\overline{\text{SD2\_RX}}$[4:7]	AH29, AJ31, AK29, AL31	I	SV_{DD}	35
SD2_REF_CLK	AE32	I	SV_{DD}	—
$\overline{\text{SD2\_REF\_CLK}}$	AE31	I	SV_{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV_{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV_{DD}	30
SD2_PLL_TPD	AF29	O	SV_{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV_{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV_{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV_{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals[5]				
EC1_GTX_CLK125	AL23	I	LV_{DD}	39
EC2_GTX_CLK125	AM23	I	TV_{DD}	39
EC_MDC	G31	O	OV_{DD}	—
EC_MDIO	G32	I/O	OV_{DD}	—
eTSEC Port 1 Signals[5]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23,AG24, AG23, AE24, AE23, AE22, AD22	O	LV_{DD}	6, 10
TSEC1_TX_EN	AB22	O	LV_{DD}	36
TSEC1_TX_ER	AH26	O	LV_{DD}	—
TSEC1_TX_CLK	AC22	I	LV_{DD}	40
TSEC1_GTX_CLK	AH25	O	LV_{DD}	41
TSEC1_CRS	AM24	I/O	LV_{DD}	37
TSEC1_COL	AM25	I	LV_{DD}	—
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV_{DD}	10
TSEC1_RX_DV	AJ24	I	LV_{DD}	—
TSEC1_RX_ER	AJ25	I	LV_{DD}	—
TSEC1_RX_CLK	AK24	I	LV_{DD}	40
eTSEC Port 2 Signals[5]				
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV_{DD}	6, 10
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV_{DD}	6,10, 38
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV_{DD}	6, 10
TSEC2_TX_EN	AB21	O	LV_{DD}	36
TSEC2_TX_ER	AB19	O	LV_{DD}	6, 38
TSEC2_TX_CLK	AC21	I	LV_{DD}	40
TSEC2_GTX_CLK	AD20	O	LV_{DD}	41
TSEC2_CRS	AE20	I/O	LV_{DD}	37
TSEC2_COL	AE21	I	LV_{DD}	—
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV_{DD}	10
TSEC2_RX_DV	AC19	I	LV_{DD}	—
TSEC2_RX_ER	AD21	I	LV_{DD}	—
TSEC2_RX_CLK	AM22	I	LV_{DD}	40
eTSEC Port 3 Signals[5]				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV_{DD}	6
TSEC3_TXD[4]/	AM19	O	TV_{DD}	—
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV_{DD}	6

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_EN	AH19	O	TV_{DD}	36
TSEC3_TX_ER	AH17	O	TV_{DD}	—
TSEC3_TX_CLK	AH18	I	TV_{DD}	40
TSEC3_GTX_CLK	AG19	O	TV_{DD}	41
TSEC3_CRS	AE15	I/O	TV_{DD}	37
TSEC3_COL	AF15	I	TV_{DD}	—
TSEC3_RXD[0:7]	AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19	I	TV_{DD}	—
TSEC3_RX_DV	AG15	I	TV_{DD}	—
TSEC3_RX_ER	AF16	I	TV_{DD}	—
TSEC3_RX_CLK	AJ18	I	TV_{DD}	40
eTSEC Port 4 Signals[5]				
TSEC4_TXD[0:3]	AC18, AC16, AD18, AD17	O	TV_{DD}	6
TSEC4_TXD[4]	AD16	O	TV_{DD}	25
TSEC4_TXD[5:7]	AB18, AB17, AB16	O	TV_{DD}	6
TSEC4_TX_EN	AF17	O	TV_{DD}	36
TSEC4_TX_ER	AF19	O	TV_{DD}	—
TSEC4_TX_CLK	AF18	I	TV_{DD}	40
TSEC4_GTX_CLK	AG17	O	TV_{DD}	41
TSEC4_CRS	AB14	I/O	TV_{DD}	37
TSEC4_COL	AC13	I	TV_{DD}	—
TSEC4_RXD[0:7]	AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17	I	TV_{DD}	—
TSEC4_RX_DV	AC15	I	TV_{DD}	—
TSEC4_RX_ER	AF14	I	TV_{DD}	—
TSEC4_RX_CLK	AG13	I	TV_{DD}	40
Local Bus Signals[5]				
LAD[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	I/O	OV_{DD}	6
LDP[0:3]	A24, E24, C24, B24	I/O	OV_{DD}	6, 22
LA[27:31]	J21, K21, G22, F24, G21	O	OV_{DD}	6, 22
$\overline{\text{LCS}}$[0:4]	A22, C22, D23, E22, A23	O	OV_{DD}	7
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA\_DREQ}}$[2]	B23	O	OV_{DD}	7, 9, 10

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
XV_{DD}_SRDS2	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for SerDes Port 2	XV_{DD}_SRDS2 1.05/1.1 V	—
V_{DD}_Core0	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V_{DD}_Core0 0.95/1.05/1.1 V	—
V_{DD}_Core1	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V_{DD}_Core1 0.95/1.05/1.1 V	12, *S1*
V_{DD}_PLAT	M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_Core0	B20	Core 0 PLL Supply	AV_{DD}_Core0 0.95/1.05/1.1 V	—
AV_{DD}_Core1	A19	Core 1 PLL Supply	AV_{DD}_Core1 0.95/1.05/1.1 V	12, *S2*
AV_{DD}_PLAT	B19	Platform PLL supply voltage	AV_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_LB	A20	Local Bus PLL supply voltage	AV_{DD}_LB 1.05/1.1 V	—
AV_{DD}_SRDS1	P32	SerDes Port 1 PLL & DLL Power Supply	AV_{DD}_SRDS1 1.05/1.1 V	—
AV_{DD}_SRDS2	AF32	SerDes Port 2 PLL & DLL Power Supply	AV_{DD}_SRDS2 1.05/1.1 V	—
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	—	—

19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 61 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 59). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

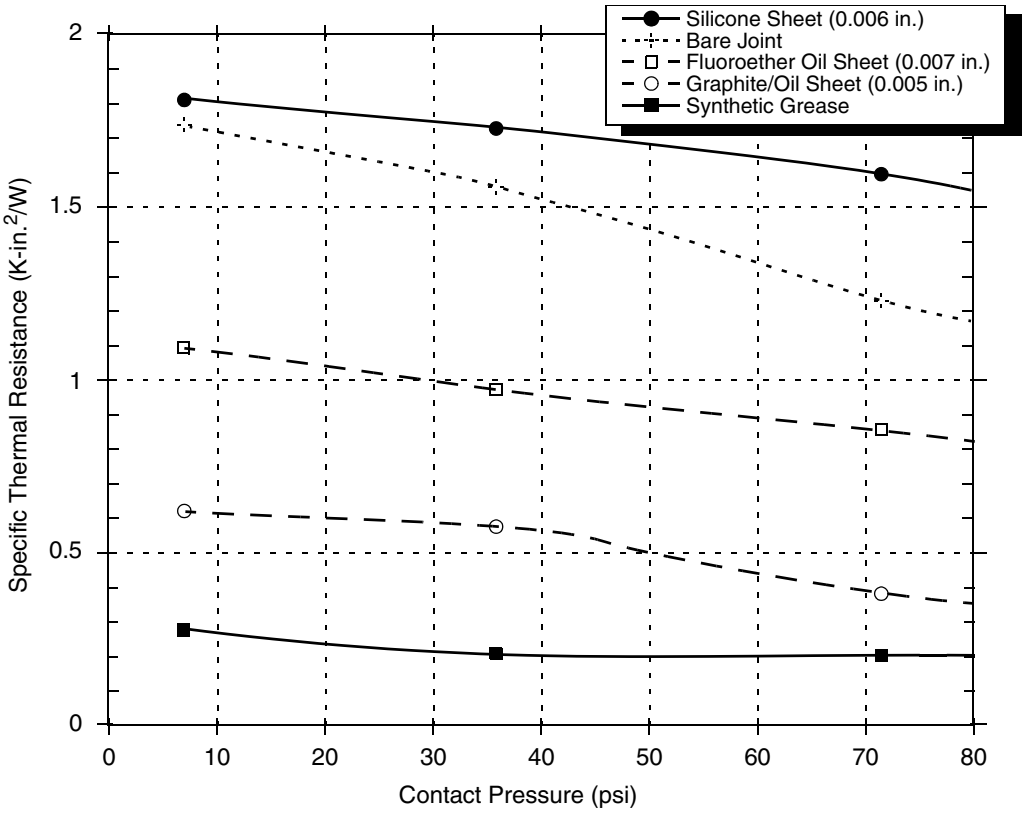


Figure 61. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

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