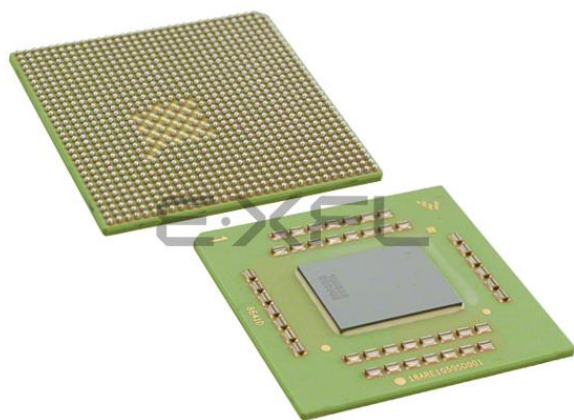




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641hx1500kc

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 2.5\text{ V}$	4, 9
DDR2 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 1.8\text{ V}$	1, 5, 9
Local Bus signals	45 25	$OV_{DD} = 3.3\text{ V}$	2, 6
eTSEC/10/100 signals	45	$T/LV_{DD} = 3.3\text{ V}$	6
	30	$T/LV_{DD} = 2.5\text{ V}$	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage	45	$OV_{DD} = 3.3\text{ V}$	6
I ² C	150	$OV_{DD} = 3.3\text{ V}$	7
SRIO, PCI Express	100	$SV_{DD} = 1.1/1.05\text{ V}$	3, 8

Notes:

1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω . See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See [Section 17, "Signal Listings,"](#) for details on resistor requirements for the calibration of $SDn_IMP_CAL_TX$ and $SDn_IMP_CAL_RX$ transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at $T_j = 105^\circ\text{C}$ and at Dn_GV_{DD} (min).

2.2 Power Up/Down Sequence

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

NOTE

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is as follows:

1. All power rails other than DDR I/O (Dn_GV_{DD} , and Dn_MV_{REF}).

The power dissipation for the MPC8641 single core device is shown in [Table 6](#).

Table 6. MPC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD-Coren} , V _{DD-PLAT} (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	20.3	1, 2
Thermal				105 °C	25.2	1, 3
Maxim					28.9	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	500 MHz	0.95 V, 1.05 V	65 °C	11.6	1, 2, 5
Thermal				105 °C	14.4	1, 3, 5
Maximum					16.5	1, 4, 5

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD-Coren}) and 65°C junction temperature (see [Table 2](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage (V_{DD-Coren}) and maximum operating junction temperature (see [Table 2](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD-Coren}) and maximum operating junction temperature (see [Table 2](#)) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
5. These power numbers are for Part Number MC8641xx1000NX only. V_{DD-Coren} = 0.95 V and V_{DD-PLAT} = 1.05 V.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/ $\overline{MCK}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8641 Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz
8. Per the JEDEC spec the DDR2 duty cycle at 600 MHz is the average low and high cycle time values that are defined as the average pulse widths calculated across any consecutive 200 pulses. Jitter can sometimes force single low and high cycle times to drift from the average values. $t_{JIT} = \pm 125$ ps.
9. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 21](#), it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$ and $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%–80%)	t_{TTXR}^2	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

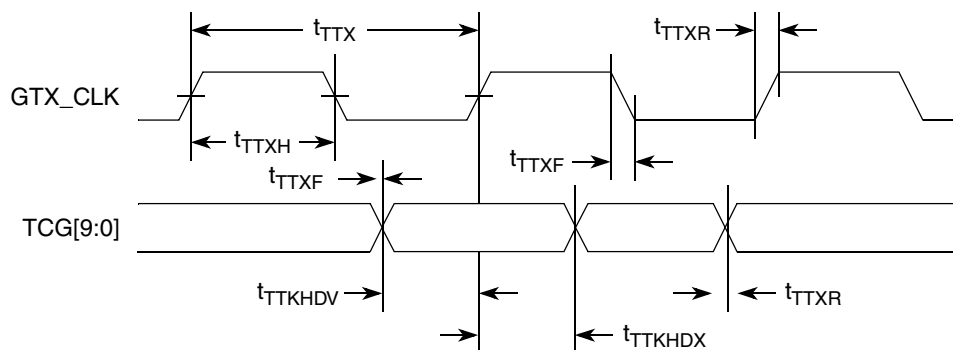


Figure 16. TBI Transmit AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC_n_RX_CLK pin (no receive clock is used on TSEC_n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in [Table 34](#).

Table 34. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}^1	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRR}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXXH}$	1.0	—	—	ns

¹ ±100 ppm tolerance on RX_CLK frequency

A timing diagram for TBI receive appears in [Figure 18](#).

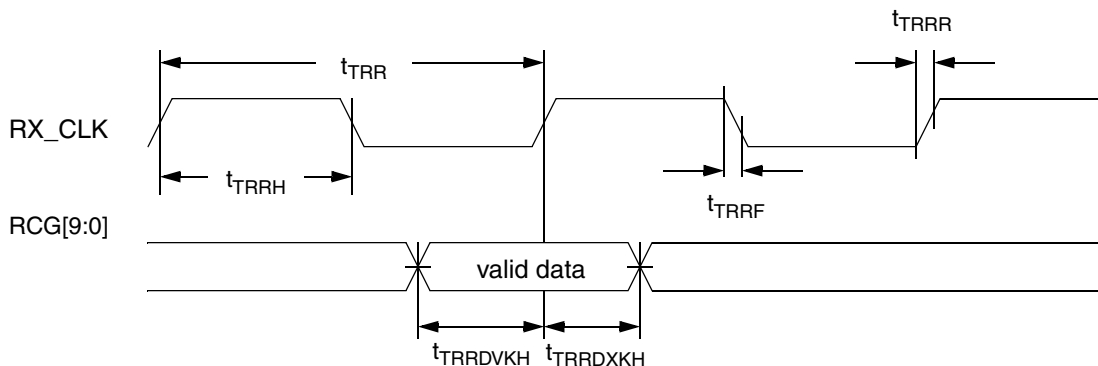


Figure 18. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

[Table 35](#) presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}^5	–500	0	500	ps
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD} = 3.3$ V DC.

Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = OV_{DD}$)	I_{IN}	—	± 5	μA
High-level output voltage ($OV_{DD} = \min$, $I_{OH} = -2$ mA)	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage ($OV_{DD} = \min$, $I_{OL} = 2$ mA)	V_{OL}	—	0.2	V

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL enabled. For information about the frequency range of local bus see Section 18.1, “Clock Ranges.”

Table 41. Local Bus Timing Parameters ($OV_{DD} = 3.3$ V)m - PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Local Bus Duty Cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	—

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8641D SerDes reference clock input's DC requirement.

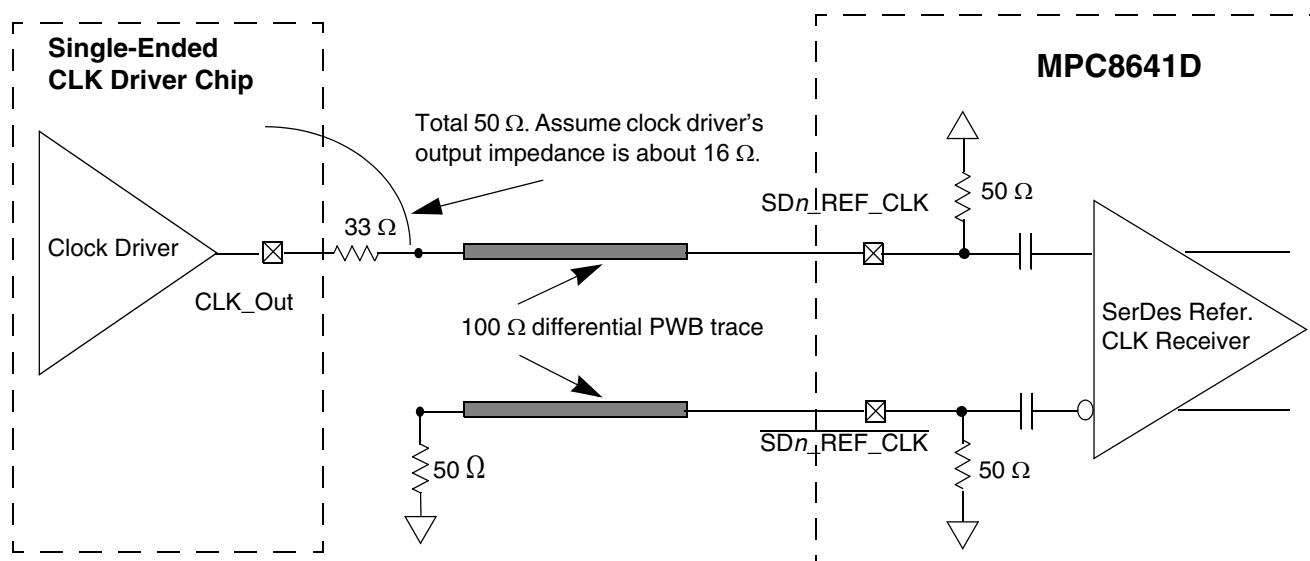


Figure 46. Single-Ended Connection (Reference Only)

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 52](#) should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in [Figure 51](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see [Figure 52](#)). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 51](#) is specified using the passive compliance/test measurement load (see [Figure 52](#)) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 52](#)) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

Table 55. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 56. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 60. Receiver AC Timing Specifications—2.5 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 55](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 61. Receiver AC Timing Specifications—3.125 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 55](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18
SD1_DLL_TPD	N28	O	SV _{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)⁴				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV _{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV _{DD}	34
$\overline{\text{SD2_TX}}[0:3]$	Y25, AA28, AB26, AC28	O	SV _{DD}	—
$\overline{\text{SD2_TX}}[4:7]$	AE28, AG28, AJ28, AL28	O	SV _{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35
$\overline{\text{SD2_RX}}[0:3]$	Y29, AA31, AB29, AC31	I	SV _{DD}	—
$\overline{\text{SD2_RX}}[4:7]$	AH29, AJ31, AK29, AL31	I	SV _{DD}	35
SD2_REF_CLK	AE32	I	SV _{DD}	—
$\overline{\text{SD2_REF_CLK}}$	AE31	I	SV _{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30
SD2_PLL_TPD	AF29	O	SV _{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV _{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals⁵				
EC1_GTX_CLK125	AL23	I	LV _{DD}	39
EC2_GTX_CLK125	AM23	I	TV _{DD}	39
EC_MDC	G31	O	OV _{DD}	—
EC_MDIO	G32	I/O	OV _{DD}	—
eTSEC Port 1 Signals⁵				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
XV _{DD} _SRDS2	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for SerDes Port 2	XV _{DD} _SRDS2 1.05/1.1 V	—
V _{DD} _Core0	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V _{DD} _Core0 0.95/1.05/1.1 V	—
V _{DD} _Core1	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V _{DD} _Core1 0.95/1.05/1.1 V	12, S1
V _{DD} _PLAT	M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V _{DD} _PLAT 1.05/1.1 V	—
AV _{DD} _Core0	B20	Core 0 PLL Supply	AV _{DD} _Core0 0.95/1.05/1.1 V	—
AV _{DD} _Core1	A19	Core 1 PLL Supply	AV _{DD} _Core1 0.95/1.05/1.1 V	12, S2
AV _{DD} _PLAT	B19	Platform PLL supply voltage	AV _{DD} _PLAT 1.05/1.1 V	—
AV _{DD} _LB	A20	Local Bus PLL supply voltage	AV _{DD} _LB 1.05/1.1 V	—
AV _{DD} _SRDS1	P32	SerDes Port 1 PLL & DLL Power Supply	AV _{DD} _SRDS1 1.05/1.1 V	—
AV _{DD} _SRDS2	AF32	SerDes Port 2 PLL & DLL Power Supply	AV _{DD} _SRDS2 1.05/1.1 V	—
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11, U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23, Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	—	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
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37. This pin is only an output in FIFO mode when used as Rx Flow Control.
38. This pin functions as `cfg_dram_type[0 or 1]` at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.
39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).
40. See [Section 18.4.2, “Platform to FIFO Restrictions”](#) for clock speed limitations for this pin when used in FIFO mode.
41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.
42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

Special Notes for Single Core Device:

- S1. Solder ball for this signal will not be populated in the single core package.
- S2. The PLL filter from V_{DD_Core1} to AV_{DD_Core1} should be removed. AV_{DD_Core1} should be pulled to ground with a weak (2–10 k Ω) resistor. See [Section 20.2.1, “PLL Power Supply Filtering”](#) for more details.
- S3. This pin should be pulled to GND for the single core device.
- S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

[Table 64](#) provides the clocking specifications for the processor cores and [Table 65](#) provides the clocking specifications for the memory bus. [Table 66](#) provides the clocking for the Platform/MPX bus and [Table 67](#) provides the clocking for the Local bus.

Table 64. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

- Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 18.2, “MPX to SYSCLK PLL Ratio,”](#) and [Section 18.3, “e600 to MPX clock PLL Ratio,”](#) for ratio settings.
- The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

18.4.1 SYCLK to Platform Frequency Options

Table 70 shows some SYCLK frequencies and the expected MPX frequency values based on the MPX clock to SYCLK ratio. Note that frequencies between 400 MHz and 500 MHz are NOT supported on the platform. See note regarding *cfg_platform_freq* in Section 17, “Signal Listings,” because it is a reset configuration pin that is related to platform frequency.

Table 70. Frequency Options of SYCLK with Respect to Platform/MPX Clock Speed

MPX to SYCLK Ratio	SYCLK (MHz)					
	66	83	100	111	133	167
	Platform/MPX Frequency (MHz) ¹					
2						
3					400	500
4				400	533	
5			500	555		
6	400	500	600			
8	533					
9	600					

¹ SYCLK frequency range is 66-167 MHz. Platform clock/ MPX frequency range is 400 MHz, 500-600 MHz.

18.4.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency}/4.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz

For FIFO encoded mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock frequency}/3.2$$

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

Tyco Electronics
 Chip Coolers™
 P.O. Box 3668
 Harrisburg, PA 17105-3668
 Internet: www.chipcoolers.com
 Wakefield Engineering
 33 Bridge St.
 Pelham, NH 03076
 Internet: www.wakefield.com

800-522-6752

603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in [Table 71](#), the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

[Figure 60](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

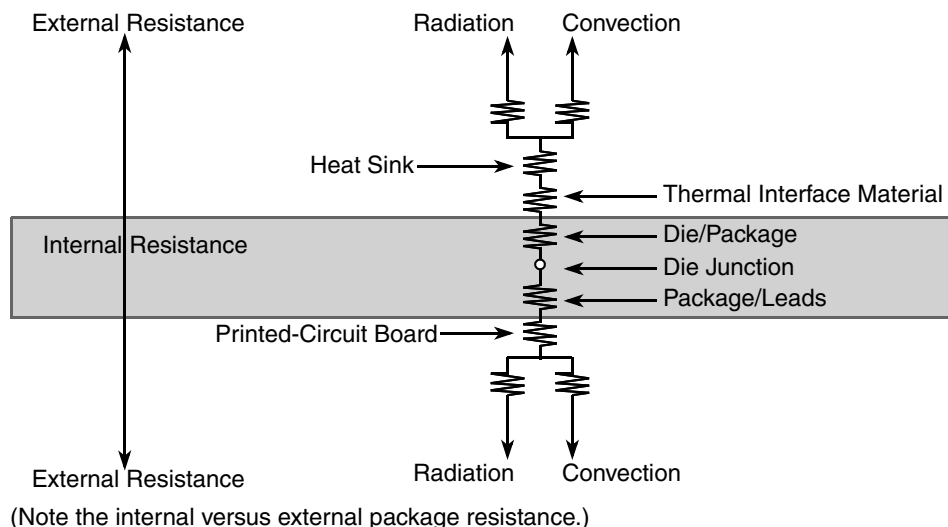


Figure 60. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 61 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 59). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

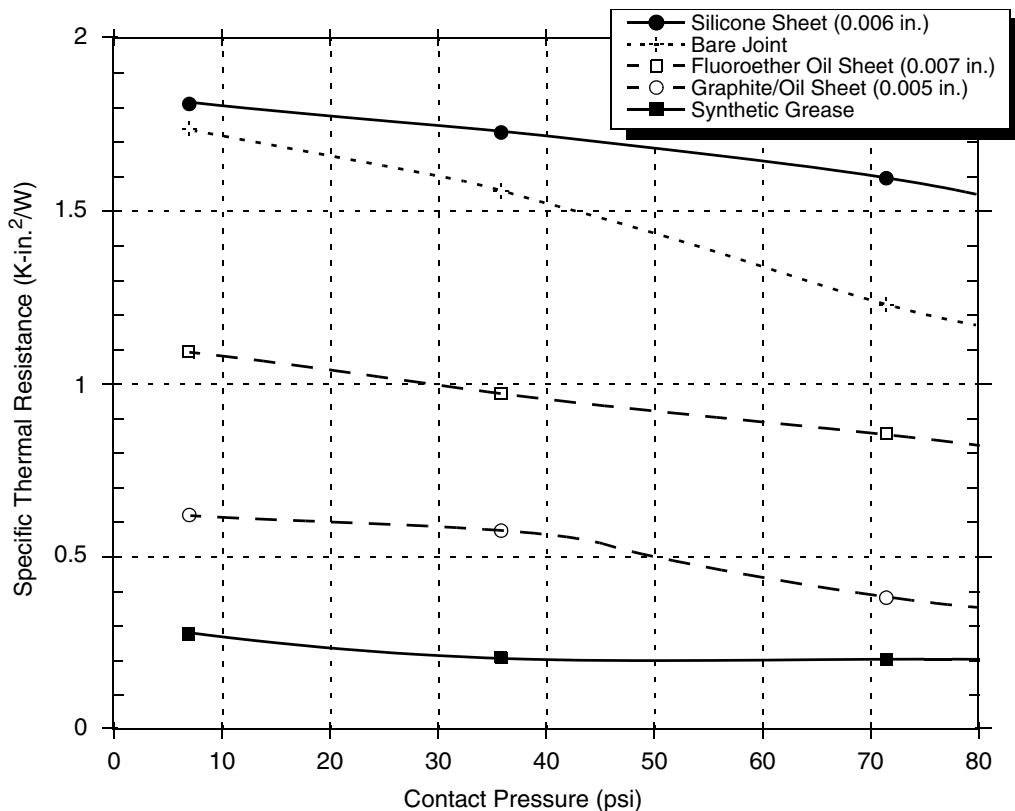


Figure 61. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78 th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

- T_j is the die-junction temperature
- T_i is the inlet cabinet ambient temperature
- T_r is the air temperature rise within the computer cabinet
- $R_{\theta JC}$ is the junction-to-case thermal resistance
- $R_{\theta int}$ is the adhesive or interface material thermal resistance
- $R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
- P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in [Table 2](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

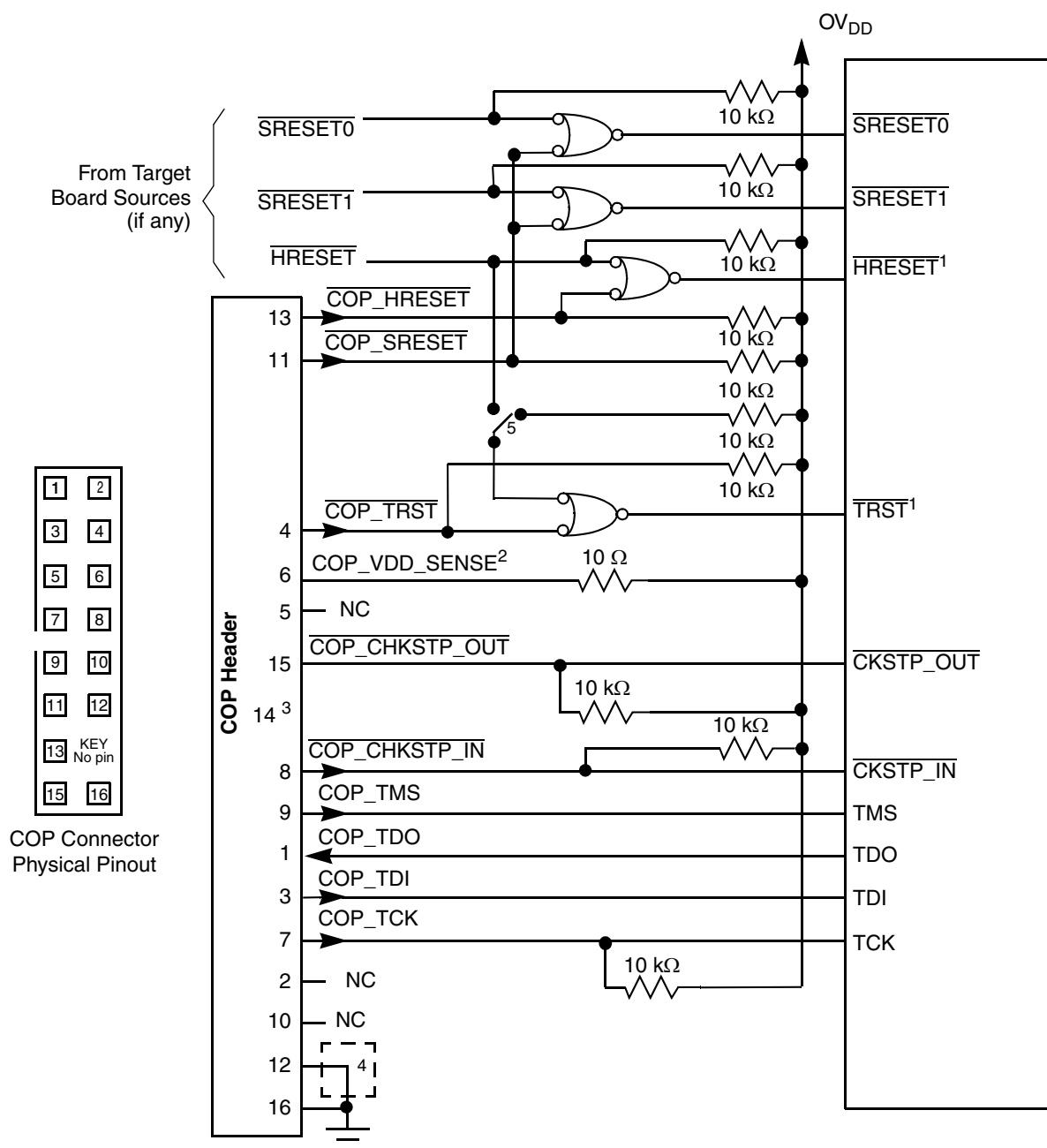
20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 68](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 67](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.



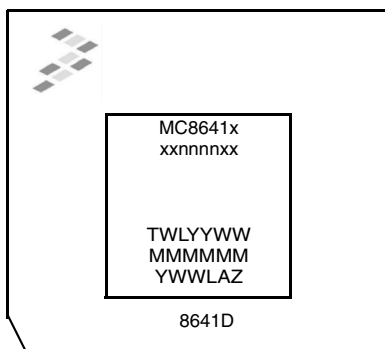
Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device

21.2 Part Marking

Parts are marked as the example shown in [Figure 70](#).



NOTE:

TWLYYWW is the test code

MMMMMM is the M00 (mask) number.

YWWLAZ is the assembly traceability code.

Figure 70. Part Marking for FC-CBGA Device

22 Document Revision History

[Table 76](#) provides a revision history for the MPC8641D hardware specification.

Table 76. Document Revision History

Revision	Date	Substantive Change(s)
3	05/2014	- Updated the Serial RapidIO equation in Section 4.4, "Platform Frequency Requirements for PCI-Express and Serial RapidIO" - Updated Section 19.2.4, "Temperature Diode," by removing the ideality factor value. - Added VJ package type designator and footnotes to Table 74, "Part Numbering Nomenclature" and Section 16.1, "Package Parameters for the MPC8641."
2	07/2009	- Added note 8 to Table 49, "Differential Transmitter (TX) Output Specifications." - Added Revision E to Table 74, "Part Numbering Nomenclature."
1	11/2008	- Added Section 4.4, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." - Removed the statement "Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)" from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core). - Added Note 8 to Figure 57 and Figure 58.
0	07/2008	Initial Release