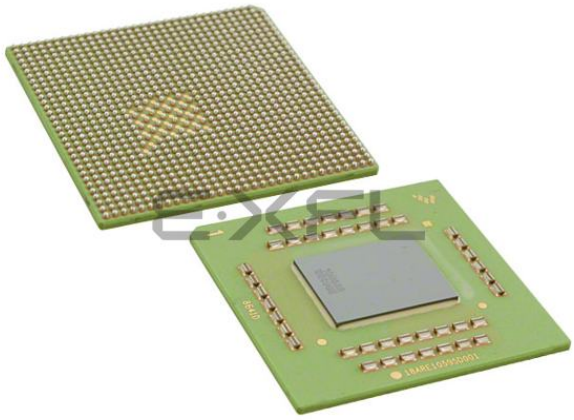

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

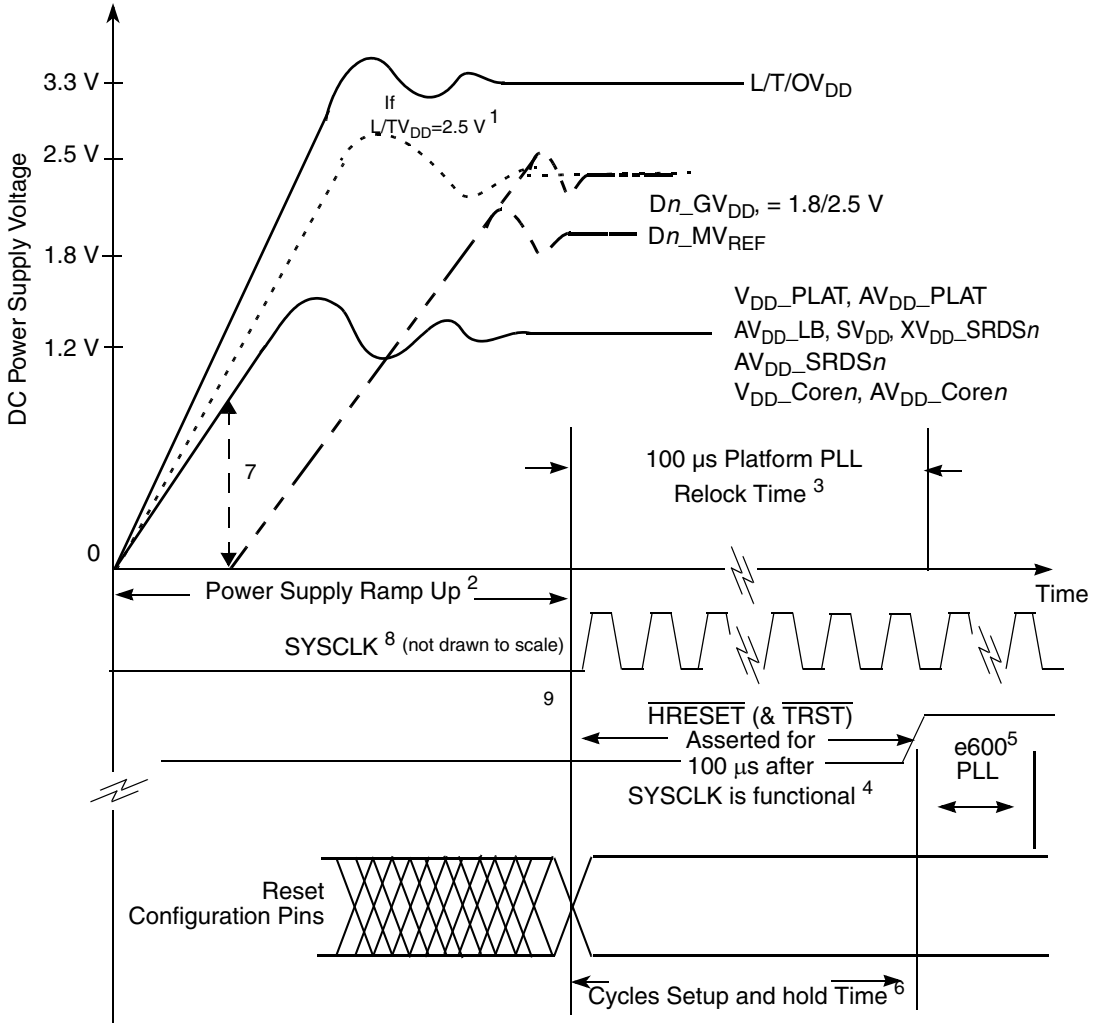
## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e600 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.25GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 994-BCBGA, FCCBGA |
| Supplier Device Package | 994-FCCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641thx1250hc |

- DDR memory controllers
  - Dual 64-bit memory controllers (72-bit with ECC)
  - Support of up to a 300-MHz clock rate and a 600-MHz DDR2 SDRAM
  - Support for DDR, DDR2 SDRAM
  - Up to 16 Gbytes per memory controller
  - Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification*, Revision 1.2
  - Both 1x and 4x LP-Serial link interfaces
  - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
  - RapidIO–compliant message unit
  - RapidIO atomic transactions to the memory controller
- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports x1, x2, x4, and x8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support of the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
  - Support a full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP off-load
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
  - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
  - RMON statistics support
  - MII management interface for control and status
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts
  - Allows processors to interrupt each other with 32b messages

Figure 3 illustrates the Power Up sequence as described above.




**Notes:**

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 2.
2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to Section 5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 11 for additional information on reset configuration pin setup timing requirements. In addition see Figure 68 regarding HRESET and JTAG connection details including TRST.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See Section 5, "RESET Initialization" for more information on setup and hold time of reset configuration signals.
7. V$_{DD}$_PLAT, AV$_{DD}$_PLAT must strictly reach 90% of their recommended voltage before the rail for D$n$_GV$_{DD}$, and D$n$_MV$_{REF}$ reaches 10% of their recommended voltage.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4],TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

**Figure 3. MPC8641 Power-Up and Reset Sequence**

should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

**Table 9. Spread Spectrum Clock Source Recommendations**

At recommended operating conditions. See Table 2.

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Frequency modulation | — | 50 | kHz | 1 |
| Frequency spread | — | 1.0 | % | 1, 2 |

**Notes:**
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 4.3 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks (EC1_GTX_CLK125 and EC2_GTX_CLK125) AC timing specifications for the MPC8641.

**Table 10. EC*n*_GTX_CLK125 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC*n*_GTX_CLK125 frequency | $f_{G125}$ | — | 125 ±100 ppm | — | MHz | 3 |
| EC*n*_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC*n*_GTX_CLK125 peak-to-peak jitter | $t_{G125J}$ | — | — | 250 | ps | 1 |

**Table 29. GMII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock fall time (80%-20%) | $t_{GRXF}$[2] | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

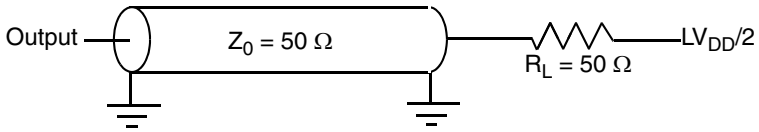



**Figure 11. eTSEC AC Test Load**

Figure 12 shows the GMII receive AC timing diagram.

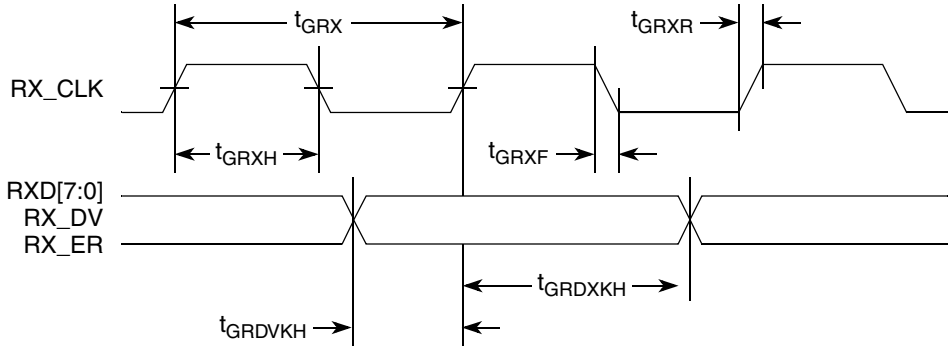



**Figure 12. GMII Receive AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

**Table 31. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$[2,3] | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$[3] | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise time (20%-80%) | $t_{MRXR}$[2] | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{MRXF}$[2] | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.

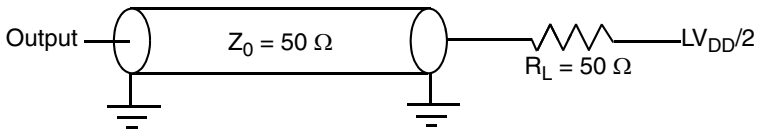



**Figure 14. eTSEC AC Test Load**

Figure 15 shows the MII receive AC timing diagram.

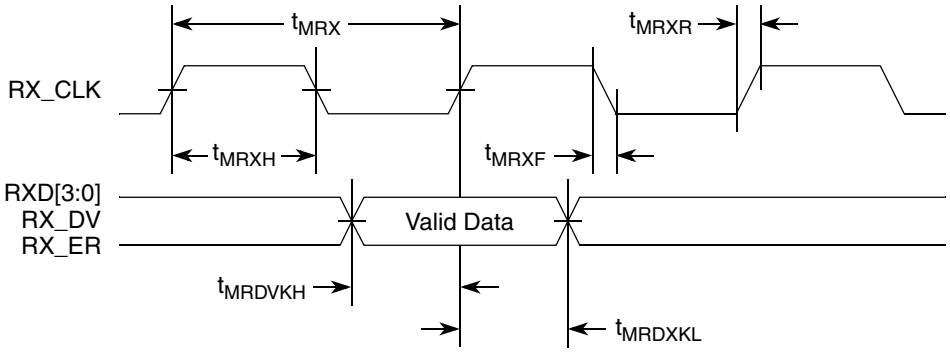



**Figure 15. MII Receive AC Timing Diagram**

**Table 35. RGMII and RTBI AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock period duration [3] | $t_{RGT}$[5,6] | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 4] | $t_{RGTH}/t_{RGT}$[5] | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$[5] | — | — | 0.75 | ns |
| Fall time (80%–20%) | $t_{RGTF}$[5] | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

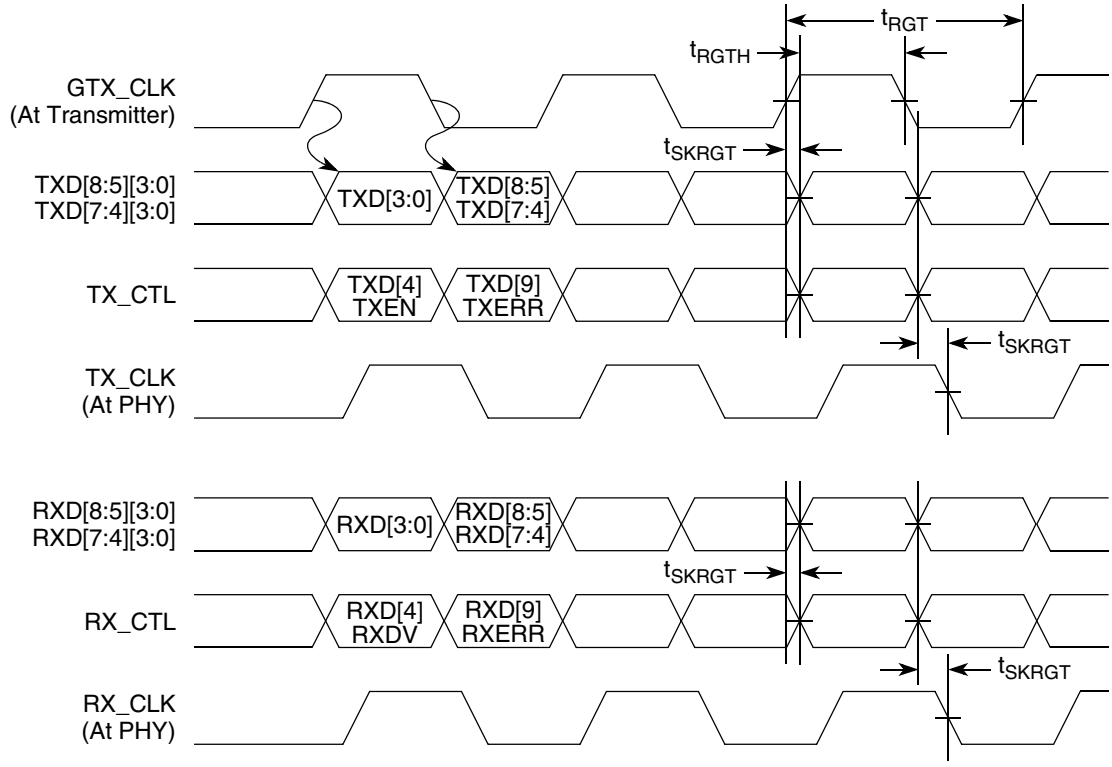



**Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams**

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

## 10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD}$ = 3.3 V DC.

**Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at $OV_{DD}$ = 3.3 V with PLL enabled. For information about the frequency range of local bus see Section 18.1, "Clock Ranges."

**Table 41. Local Bus Timing Parameters ($OV_{DD}$ = 3.3 V)m - PLL Enabled**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Local Bus Duty Cycle | $t_{LBKH}/t_{LBK}$ | 45 | 55 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.0 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.2 | ns | — |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | — |

Figure 26 to Figure 31 show the local bus signals.

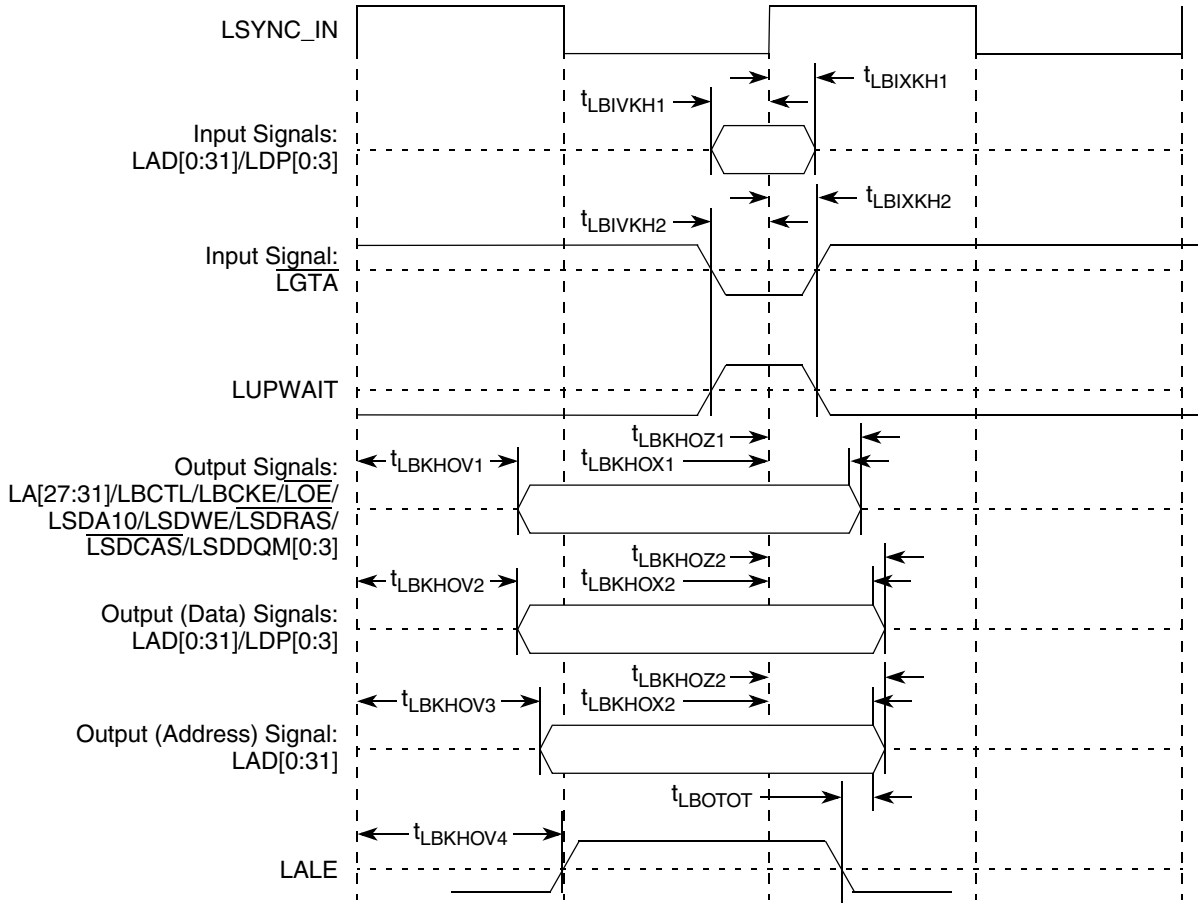



**Figure 26. Local Bus Signals (PLL Enabled)**

**NOTE**

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at $OV_{DD}$ = 3.3 V with PLL bypassed.

**Table 42. Local Bus Timing Parameters—PLL Bypassed**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 12 | — | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 45 | 55 | % | — |
| Internal launch/capture clock to LCLK delay | $t_{LBKHKT}$ | 2.3 | 3.9 | ns | 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 5.7 | — | ns | 4, 5 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKL2}$ | 5.6 | — | ns | 4, 5 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | –1.8 | — | ns | 4, 5 |

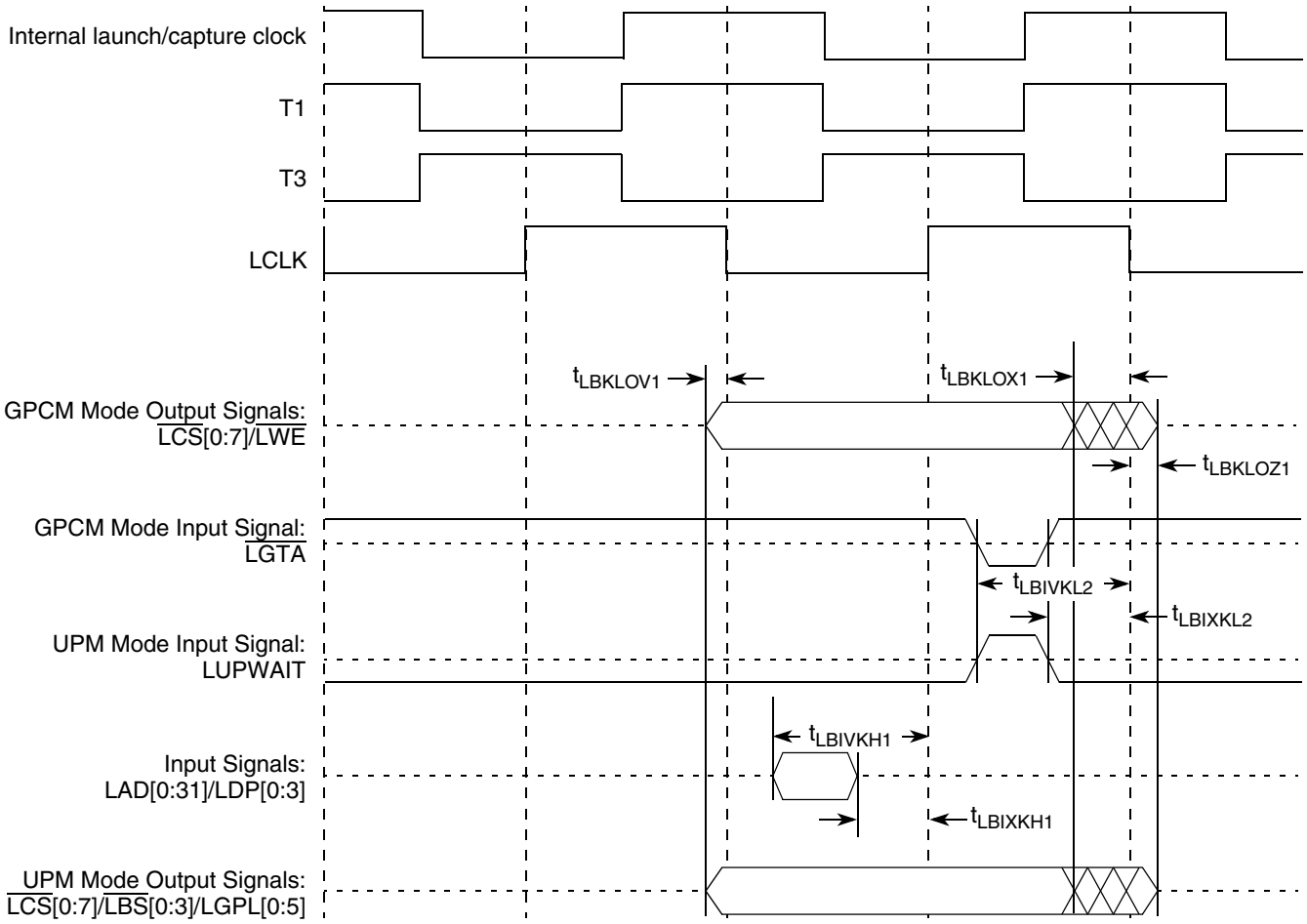



**Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)**

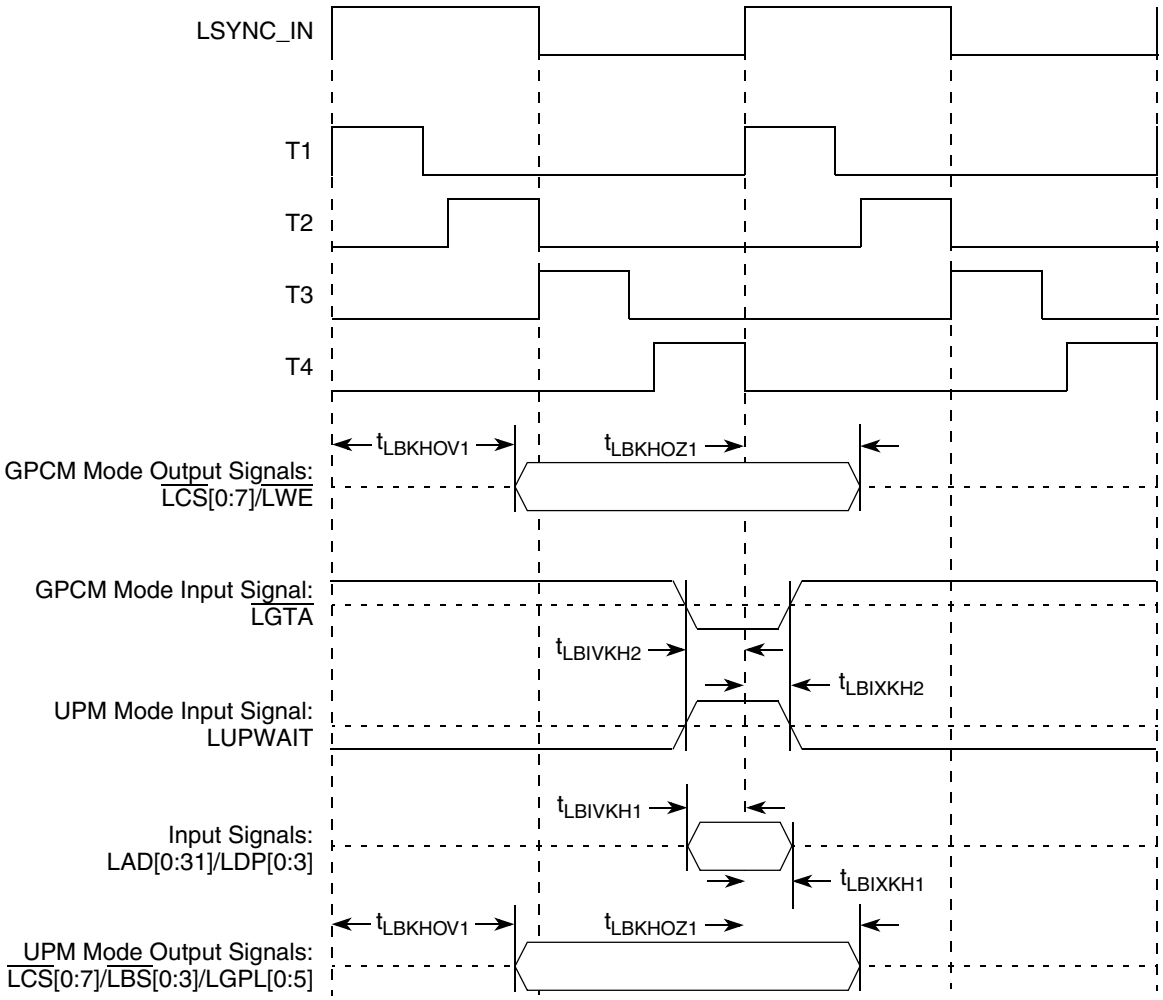



**Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)**

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)**

At recommended operating conditions (see Table 3).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>30<br>30 | <br>—<br>— | ns | 5, 6 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.

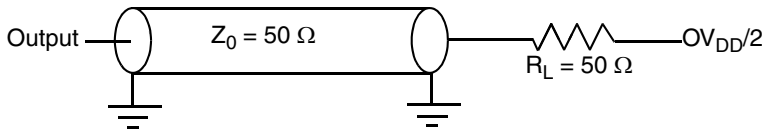



**Figure 32. AC Test Load for the JTAG Interface**

Figure 33 provides the JTAG clock input timing diagram.

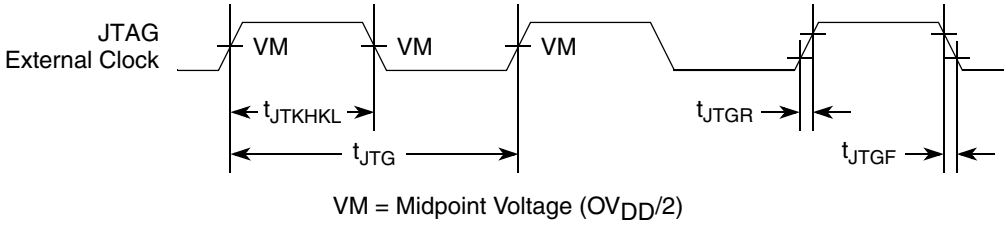



**Figure 33. JTAG Clock Input Timing Diagram**

### 13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 47 describes some AC parameters common to PCI Express and Serial RapidIO protocols.

**Table 47. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD}$_SRDS1 or $XV_{DD}$_SRDS2 = 1.1V ± 5% and 1.05V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Rising Edge Rate | Rise Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling Edge Rate | Fall Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential Input High Voltage | $V_{IH}$ | +200 | | mV | 2 |
| Differential Input Low Voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching | Rise-Fall Matching | — | 20 | % | 1, 4 |

**Notes:**

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.

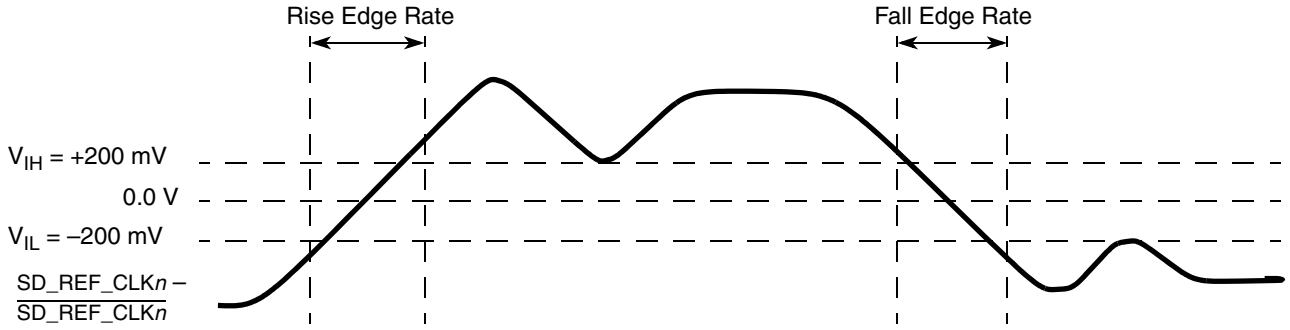



**Figure 47. Differential Measurement Points for Rise and Fall Time**

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see Figure 52). Note that the series capacitors, $C_{TX}$, are optional for the return loss measurement.

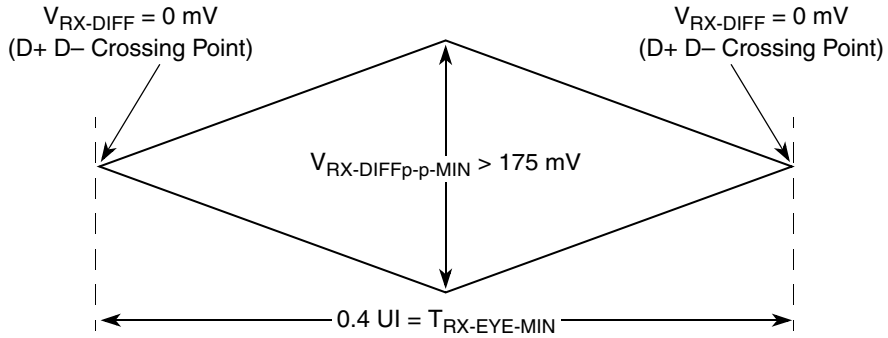



**Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification**

### 14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

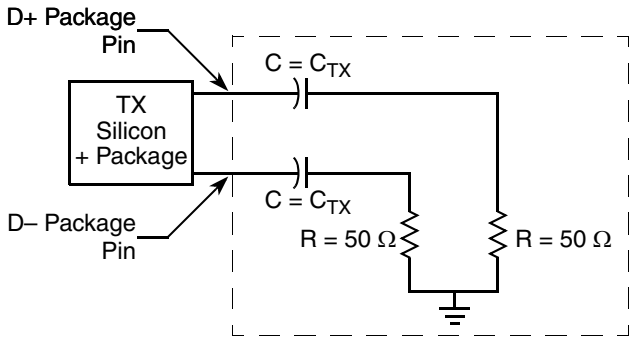



**Figure 52. Compliance Test/Measurement Load**

# 15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

## 15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

## 15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.

## 15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

## 15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

**Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/– 100 ppm |

**Table 55. Long Run Transmitter AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | +/– 100 ppm |

**Table 56. Long Run Transmitter AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | +/– 100 ppm |

# 17 Signal Listings

Table 63 provides the pin assignments for the signals. Notes for the signal changes on the single core device (MPC8641) are italicized and prefixed by *"S"*.

**Table 63. MPC8641 Signal Reference by Functional Block**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DDR Memory Interface 1 Signals[2,3]** | | | | |
| D1_MDQ[0:63] | D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17 | I/O | $D1\_GV_{DD}$ | — |
| D1_MECC[0:7] | M8, M7, R8, T10, L11, L10, P9, R10 | I/O | $D1\_GV_{DD}$ | — |
| D1_MDM[0:8] | C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10 | O | $D1\_GV_{DD}$ | — |
| D1_MDQS[0:8] | A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9 | I/O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MDQS}}$[0:8] | D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10 | I/O | $D1\_GV_{DD}$ | — |
| D1_MBA[0:2] | AA8, AA10, T9 | O | $D1\_GV_{DD}$ | — |
| D1_MA[0:15] | Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6 | O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MWE}}$ | AB11 | O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MRAS}}$ | AB12 | O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MCAS}}$ | AC10 | O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MCS}}$[0:3] | AB9, AD10, AC12, AD11 | O | $D1\_GV_{DD}$ | — |
| D1_MCKE[0:3] | P7, M10, N8, M11 | O | $D1\_GV_{DD}$ | 23 |
| D1_MCK[0:5] | W6, E13, AH11, Y7, F14, AG10 | O | $D1\_GV_{DD}$ | — |
| $\overline{\text{D1\_MCK}}$[0:5] | Y6, E12, AH12, AA7, F13, AG11 | O | $D1\_GV_{DD}$ | — |
| D1_MODT[0:3] | AC9, AF12, AE11, AF10 | O | $D1\_GV_{DD}$ | — |
| D1_MDIC[0:1] | E15, G14 | IO | $D1\_GV_{DD}$ | 27 |
| $D1\_MV_{REF}$ | AM18 | DDR Port 1 reference voltage | $D1\_GV_{DD}$ /2 | 3 |
| **DDR Memory Interface 2 Signals[2,3]** | | | | |

- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

**Table 68. MPX:SYSCLK Ratio**

| Binary Value of LA[28:31] Signals | MPX:SYSCLK Ratio |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | 2:1 |
| 0011 | 3:1 |
| 0100 | 4:1 |
| 0101 | 5:1 |
| 0110 | 6:1 |
| 0111 | Reserved |
| 1000 | 8:1 |
| 1001 | 9:1 |

## 18.3 e600 to MPX clock PLL Ratio

Table 69 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 69.

**Table 69. e600 Core to MPX Clock Ratio**

| Binary Value of LDP[0:3], LA[27] Signals | e600 core: MPX Clock Ratio |
|---|---|
| 01000 | 2:1 |
| 01100 | 2.5:1 |
| 10000 | 3:1 |
| 11100 | 3.5:1 |
| 10100 | 4:1 |
| 01110 | 4.5:1 |

## 18.4 Frequency Options

Local Bus - If parity is not used, tie LDP[0:3] to ground via a 4.7 kΩ resistor, tie LPBSE to $OV_{DD}$ via a 4.7 kΩ resistor (pull-up resistor). For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

SerDes - Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 20.5.1, "Guidelines for High-Speed Interface Termination."

## 20.5.1 Guidelines for High-Speed Interface Termination

### 20.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:3] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 72 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

**Table 72. SerDes Port Enabled/Disabled Configurations**

| | Disabled through POR input | Enabled through POR input |
|---|---|---|
| **Enabled through DEVDISR** | SerDes port is disabled (and cannot be enabled through DEVDISR)<br><br>Complete termination required (Reference Clock not required) | SerDes port is enabled<br><br>Partial termination may be required[1] (Reference Clock is required) |
| **Disabled through DEVDISR** | SerDes port is disabled (through POR input)<br><br>Complete termination required (Reference Clock not required) | SerDes port is disabled after software disables port<br><br>Same termination requirements as when the port is enabled through POR input[2] (Reference Clock is required) |

**Notes:**

1 Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in x8 PCI Express mode, no termination is required because all pins are being used. If the port is in x1/x2/x4 PCI Express mode, termination is required on the unused pins. If the port is in x4 Serial RapidIO mode termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

# 21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

## 21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 74. Part Numbering Nomenclature**

| MC | nnnn | x | xx | nnnn | x | x |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Core Count** | **Package [1]** | **Core Processor Frequency [2] (MHz)** | **DDR speed (MHz)** | **Product Revision Level** |
| MC | 8641 | Blank = Single Core<br>D = Dual Core | HX = High-lead HCTE FC-CBGA<br>VU = RoHS lead-free HCTE FC-CBGA[5]<br>VJ = lead-free HCTE FC-CBGA[6] | 1000, 1250, 1333, 1500 | N = 500 MHz[4]<br>K = 600 MHz<br>J = 533 MHz<br>H = 500 MHz<br>G = 400 MHz | Revision B = 2.0<br>System Version Register Value for Rev B:<br>0x8090_0020 - MPC8641<br>0x8090_0120 - MPC8641D<br><br>Revision C = 2.1<br>System Version Register Value for Rev C:<br>0x8090_0021 - MPC8641<br>0x8090_0121 - MPC8641D<br><br>Revision E = 3.0<br>System Version Register Value for Rev E:<br>0x8090_0030 - MPC8641<br>0x8090_0130 - MPC8641D |

**Notes:**

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low $V_{DD}$_Core*n* device. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.