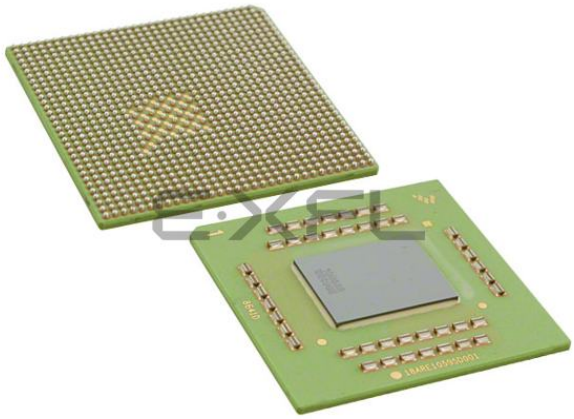


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641vu1000nc

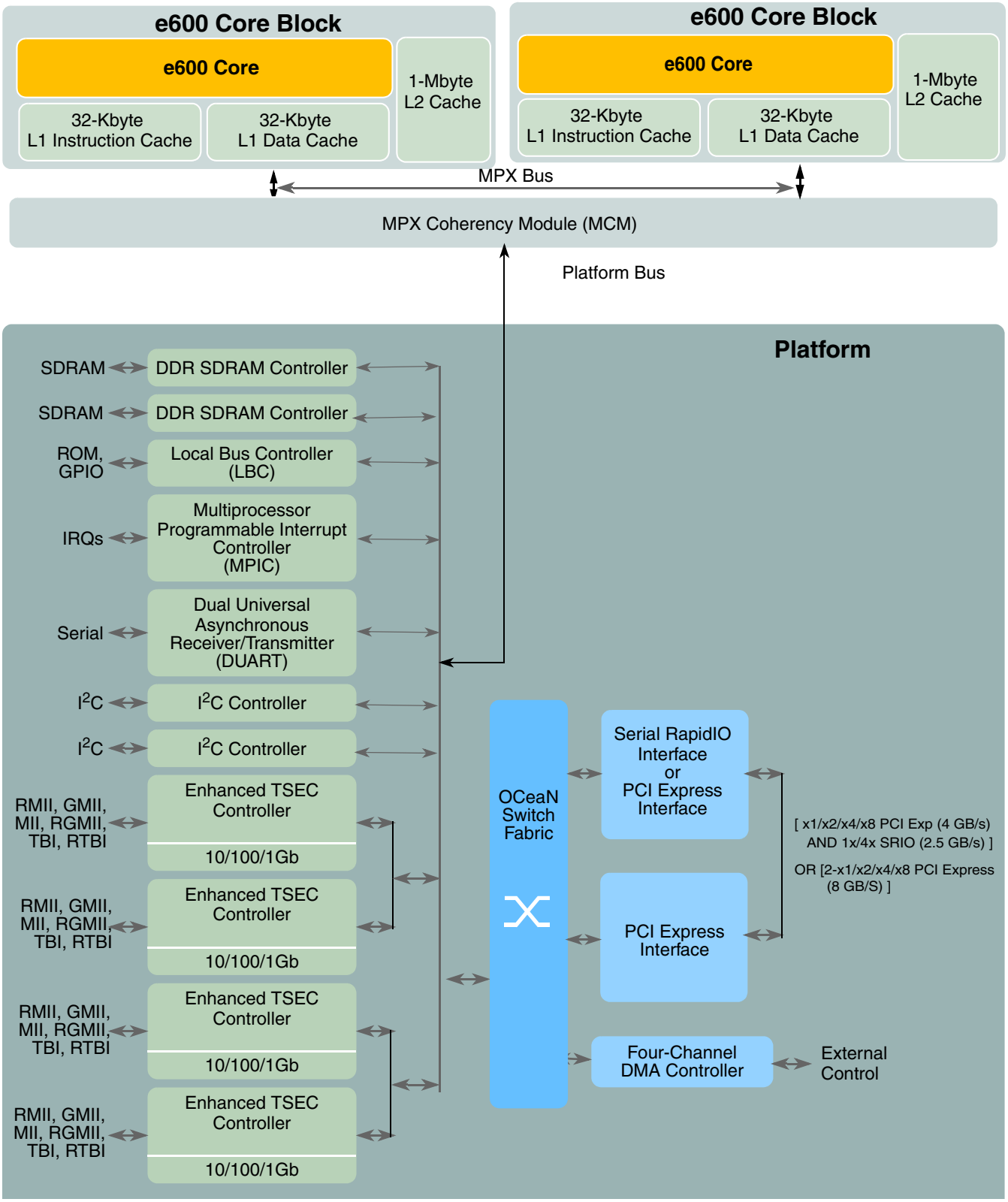


Figure 1. MPC8641 and MPC8641D

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
SerDes Serial I/O Supply Port 1		XV_{DD}_SRDS1	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
SerDes Serial I/O Supply Port 2		XV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
SerDes DLL and PLL supply voltage for Port 1 and Port 2		AV_{DD}_SRDS1, AV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Platform Supply voltage		V_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Local Bus and Platform PLL supply voltage		AV_{DD}_LB, AV_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
DDR and DDR2 SDRAM I/O supply voltages		D1_GV_{DD}, D2_GV_{DD}	2.5 V ± 125 mV	V	9
			1.8 V ± 90 mV	V	9
eTSEC 1 and 2 I/O supply voltage		LV_{DD}	3.3 V ± 165 mV	V	10
			2.5 V ± 125 mV	V	10
eTSEC 3 and 4 I/O supply voltage		TV_{DD}	3.3 V ± 165 mV	V	10
			2.5 V ± 125 mV	V	10
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	5
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	GND to D*n*_GV_{DD}	V	3, 6
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	D*n*_GV_{DD}/2 ± 1%	V	
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4, 6
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to OV_{DD}	V	5,6

4 Input Clocks

Table 7 provides the system clock (SYSCLK) DC specifications for the MPC8641.

Table 7. SYSCLK DC Electrical Characteristics (OVDD = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	166.66	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	150	ps	4, 5

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter

Table 10. EC*n*_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC*n*_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. ±100 ppm tolerance on EC*n*_GTX_CLK125 frequency

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg\_plat\_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	2.375	2.625	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF} + 0.15	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF}– 0.15	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 16 provides the DDR capacitance when D*n*_GV_{DD} (typ)=2.5 V.

Table 16. DDR SDRAM Capacitance for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

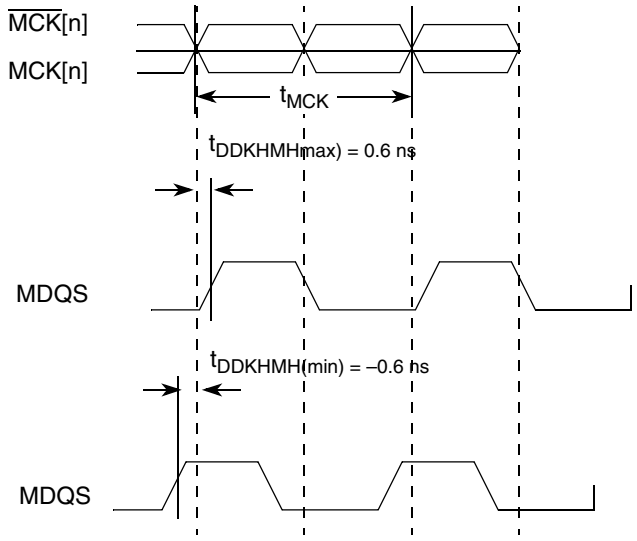


Figure 5. Timing Diagram for tDDKHMH

Figure 6 shows the DDR SDRAM output timing diagram.

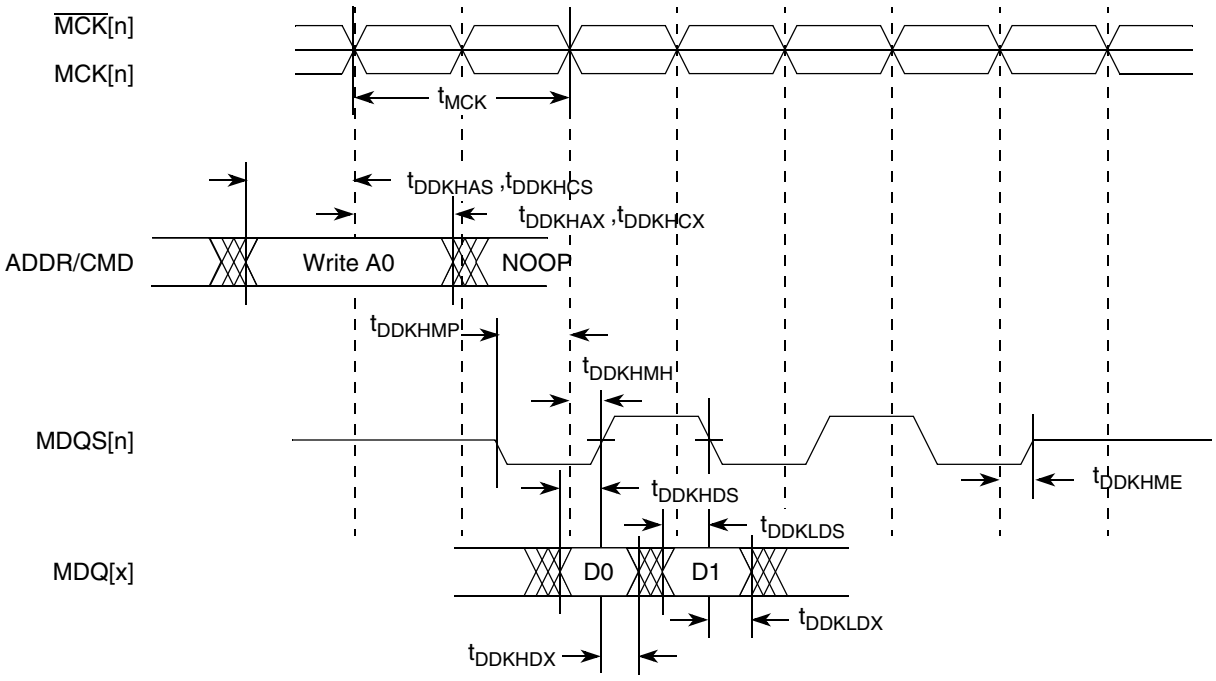


Figure 6. DDR SDRAM Output Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

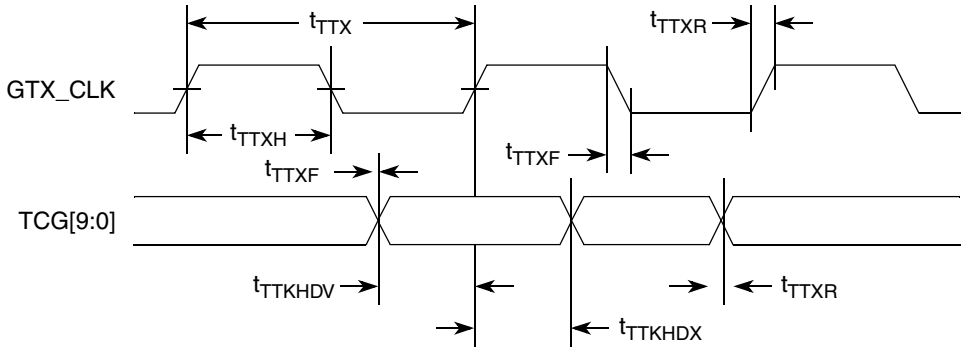


Figure 16. TBI Transmit AC Timing Diagram

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	–0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	–0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.2	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.2	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

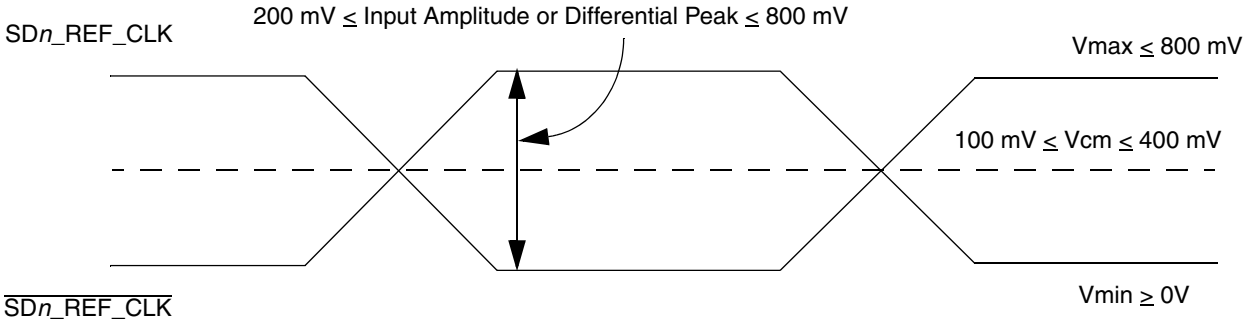


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

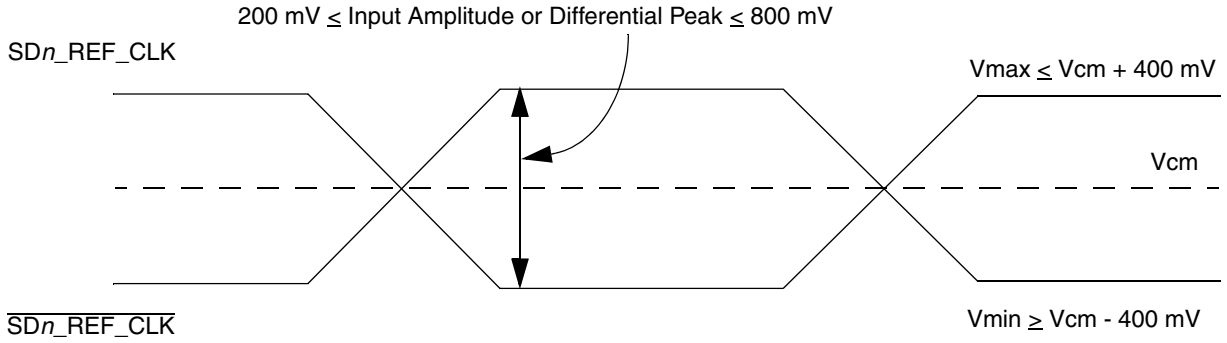


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

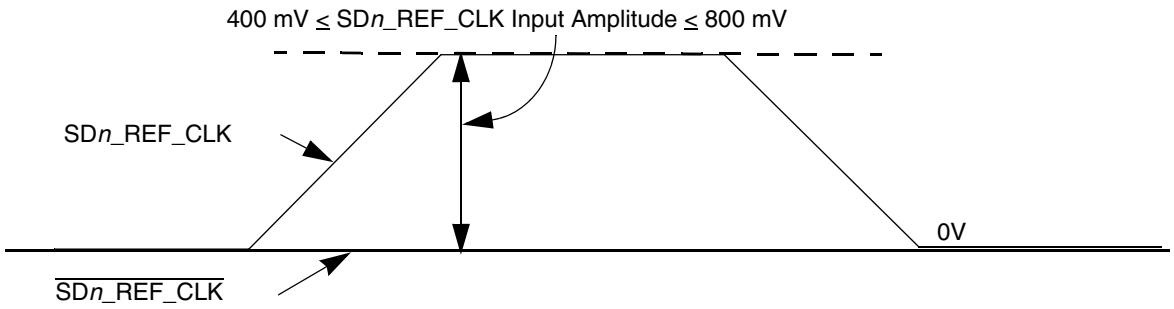


Figure 42. Single-Ended Reference Clock Input DC Requirements

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.2, "SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.

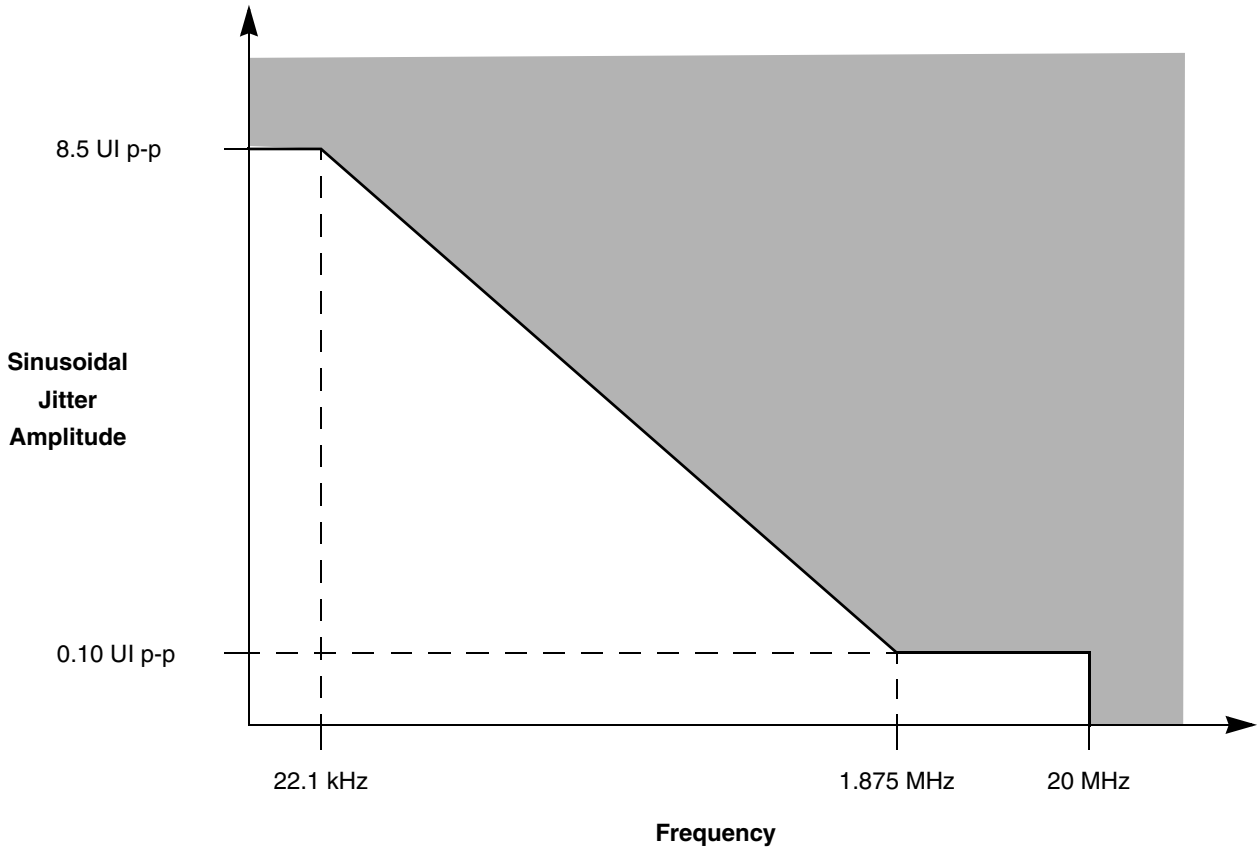


Figure 55. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 59, Table 60, Table 61) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 56 with the parameters specified in Table . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω +/– 5% differential resistive load.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LCS[6]/DMA_DACK[2]	E23	O	OV_{DD}	7, 10
LCS[7]/DMA_DDONE[2]	F23	O	OV_{DD}	7, 10
LWE[0:3]/ LSDDQM[0:3]/ LBS[0:3]	E21, F21, D22, E20	O	OV_{DD}	6
LBCTL	D21	O	OV_{DD}	—
LALE	E19	O	OV_{DD}	—
LGPL0/LSDA10	F20	O	OV_{DD}	25
LGPL1/LSDWE	H20	O	OV_{DD}	25
LGPL2/LOE/ LSDRAS	J20	O	OV_{DD}	—
LGPL3/LSDCAS	K20	O	OV_{DD}	6
LGPL4/LGTA/ LUPWAIT/LPBSE	L21	I/O	OV_{DD}	42
LGPL5	J19	O	OV_{DD}	6
LCKE	H19	O	OV_{DD}	—
LCLK[0:2]	G19, L19, M20	O	OV_{DD}	—
LSYNC_IN	M19	I	OV_{DD}	—
LSYNC_OUT	D20	O	OV_{DD}	—
DMA Signals[5]				
DMA_DREQ[0:1]	E31, E32	I	OV_{DD}	—
DMA_DREQ[2]/LCS[5]	B23	I	OV_{DD}	9, 10
DMA_DREQ[3]/IRQ[9]	B30	I	OV_{DD}	10
DMA_DACK[0:1]	D32, F30	O	OV_{DD}	—
DMA_DACK[2]/LCS[6]	E23	O	OV_{DD}	10
DMA_DACK[3]/IRQ[10]	C30	O	OV_{DD}	9, 10
DMA_DDONE[0:1]	F31, F32	O	OV_{DD}	—
DMA_DDONE[2]/LCS[7]	F23	O	OV_{DD}	10
DMA_DDONE[3]/IRQ[11]	D30	O	OV_{DD}	9, 10
Programmable Interrupt Controller Signals[5]				
MCP_0	F17	I	OV_{DD}	—
MCP _1	H17	I	OV_{DD}	12, *S4*
IRQ[0:8]	G28, G29, H27, J23, M23, J27, F28, J24, L23	I	OV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*	—	—
Reset Configuration Signals[20]				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV_{DD}	—
TSEC1_TXD[1]/ cfg_platform_freq	AC23	—	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	—	LV_{DD}	—
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	—	LV_{DD}	—
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV_{DD}	—
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV_{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	—	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	—	LV_{DD}	—
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV_{DD}	—
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	—
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	—	LV_{DD}	—
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	—	LV_{DD}	—

19 Thermal

This section describes the thermal specifications of the MPC8641.

19.1 Thermal Characteristics

Table 71 provides the package thermal characteristics for the MPC8641.

Table 71. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JA}$	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	5	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	°C/W	5

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

19.2 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8641 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 19.2.4, “Temperature Diode,” for more information.

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 59 shows a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 68. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 67 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 67, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 67; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 67 is common to all known emulators.

For a multi-processor non-daisy chain configuration, Figure 68, can be duplicated for each processor. The recommended daisy chain configuration is shown in Figure 69. Please consult with your tool vendor to determine which configuration is supported by their emulator.

20.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 68. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

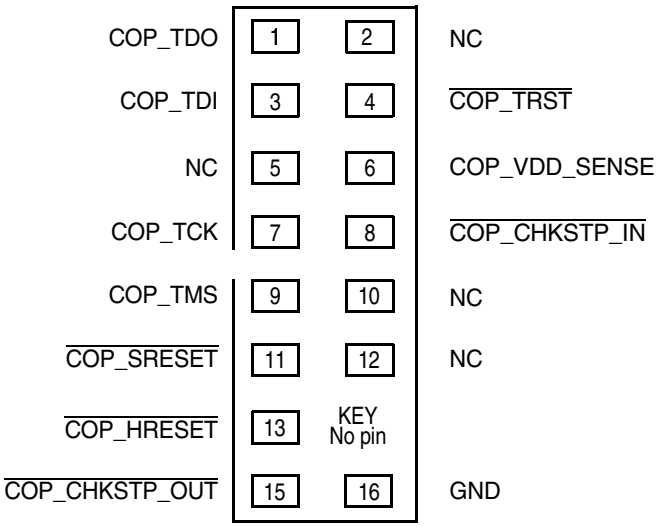
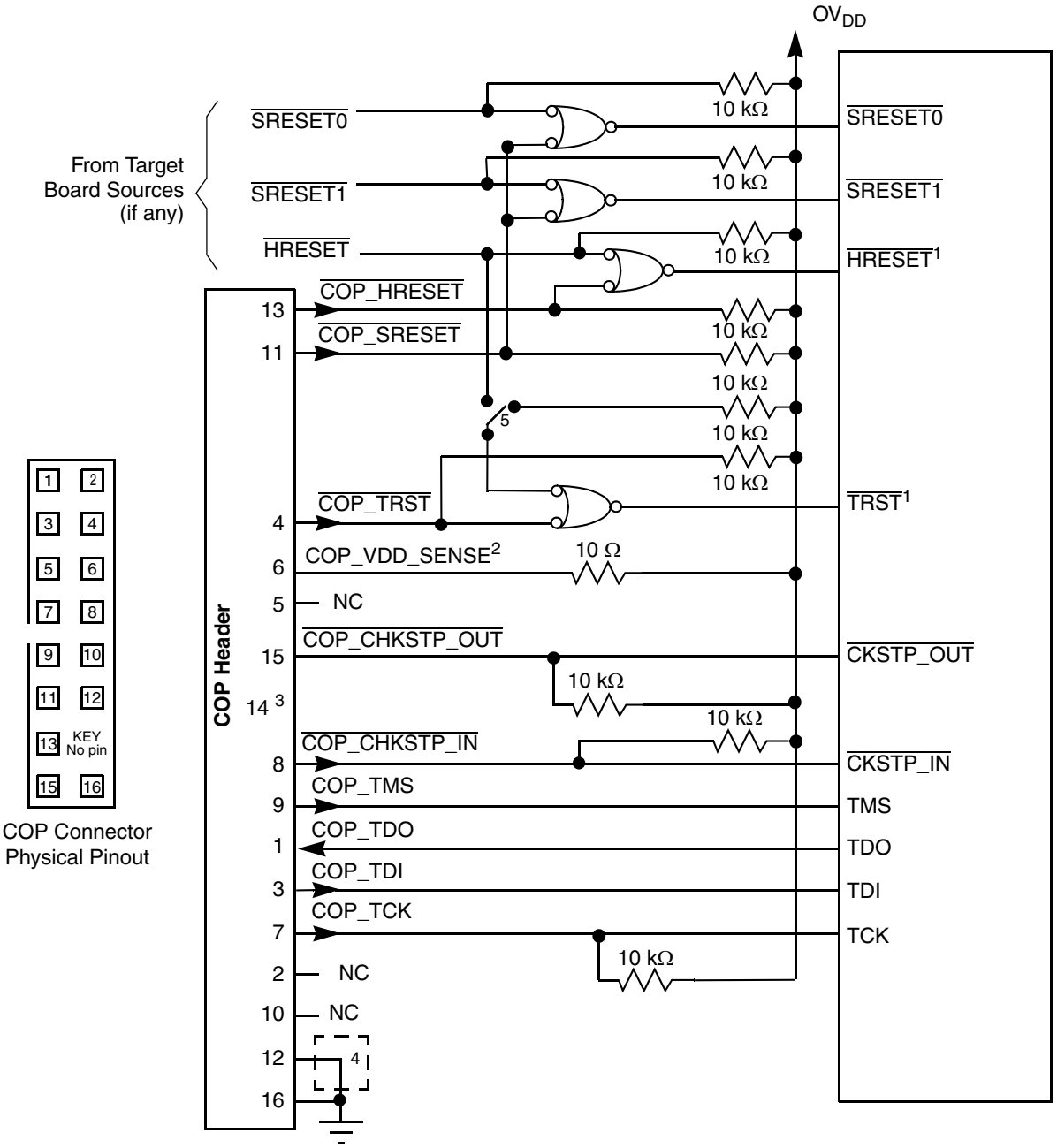


Figure 67. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	**Part Identifier**	**Core Count**	**Package [1]**	**Core Processor Frequency [2] (MHz)**	**DDR speed (MHz)**	**Product Revision Level**
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA[5] VJ = lead-free HCTE FC-CBGA[6]	1000, 1250, 1333, 1500	N = 500 MHz[4] K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD}_Core*n* device. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.