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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641vu1250hb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview



Figure 1. MPC8641 and MPC8641D



- Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects support eight external slaves
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and the remote masters
 - Supports transfers to or from any local memory or I/O port
 - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compatible, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic ball grid array (FC-CBGA)



Electrical Characteristics

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V _{DD} _Core0, V _{DD} _Core1	-0.3 to 1.21 V	V	2
Cores PLL supply	AV _{DD} _Core0, AV _{DD} _Core1	–0.3 to 1.21 V	V	_
SerDes Transceiver Supply (Ports 1 and 2)	SV _{DD}	–0.3 to 1.21 V	V	_
SerDes Serial I/O Supply Port 1	XV _{DD} _SRDS1	–0.3 to 1.21V	V	_
SerDes Serial I/O Supply Port 2	XV _{DD} _SRDS2	-0.3 to 1.21 V	V	
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV _{DD} _SRDS1, AV _{DD} _SRDS2	-0.3 to 1.21V	V	—
Platform Supply voltage	V _{DD} _PLAT	–0.3 to 1.21V	V	
Local Bus and Platform PLL supply voltage	AV _{DD} _LB, AV _{DD} _PLAT	-0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV _{DD,}	–0.3 to 2.75 V	V	3
	D2_GV _{DD}	–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV _{DD}	–0.3 to 3.63 V	V	4
		-0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV _{DD}	-0.3 to 3.63 V	V	4
		-0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV _{DD}	–0.3 to 3.63 V	V	—

Electrical Characteristics

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8641.



Figure 2. Overshoot/Undershoot Voltage for Dn_M/O/L/TV_{IN}

The MPC8641 core voltage must always be provided at nominal V_{DD} _Core*n* (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and L/TV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied Dn_MV_{REF} signal (nominally set to $Dn_GV_{DD}/2$) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.





Table 10. ECn_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC <i>n</i> _GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	1, 2

Notes:

1. Timing is guaranteed by design and characterization.

2. ECn_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. ECn_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

3. ±100 ppm tolerance on ECn_GTX_CLK125 frequency

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

527 MHz x (PCI-Express link width) 16 / (1 + cfg_plat_freq)

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

2 × (0.8512) × (Serial RapidIO interface frequency) × (Serial RapidIO link width)

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4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.



6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is $Dn_GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $Dn_GV_{DD}(typ) = 1.8$ V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when $Dn_GV_{DD}(typ) = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	1.71	1.89	V	1
I/O reference voltage	Dn_MV _{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 imes Dn_{DD}$	V	2
I/O termination voltage	V _{TT}	D <i>n</i> _MV _{REF} – 0.0 4	D <i>n_</i> MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	D <i>n_</i> MV _{REF} + 0.1 25	D <i>n_</i> GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	D <i>n</i> _MV _{REF} - 0.125	V	_
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	_	mA	_
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 13. DDR2 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 1.8 V

Notes:

1. $Dn_{GV_{DD}}$ is expected to be within 50 mV of the DRAM $Dn_{GV_{DD}}$ at all times.

2. Dn_MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF}. This rail should track variations in the DC level of Dn_MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq Dn_GV_{DD}.

Table 14 provides the DDR2 capacitance when $Dn_{GV_{DD}(typ)} = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.



8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 36.

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
REF_CLK clock period	t _{RMT}	—	20.0	—	ns
REF_CLK duty cycle	t _{RMTH} /t _{RMT}	35	50	65	%
REF_CLK peak-to-peak jitter	t _{RMTJ}	—	_	250	ps
Rise time REF_CLK (20%-80%)	t _{RMTR}	1.0	_	2.0	ns
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 20 shows the RMII transmit AC timing diagram.



Figure 20. RMII Transmit AC Timing Diagram



Local Bus



Figure 27. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock, with the exception of the LGTA/LUPWAIT signal, which is captured at the rising edge of the internal clock.



Local Bus



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Enabled)







Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)







Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)



High-Speed Serial Interfaces (HSSI)

MPC8641D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8641D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)



Transmitter Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 58. Transmitter Differential Output Eye Diagram Parameters

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Characteristic	Symbol	Ra	nge	Unit	Notes
Characteristic	Symbol	Min	Мах	Unit	Notes
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	_	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10 ⁻¹²	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 59. Receiver AC Timing Specifications—1.25 GBaud

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100Ω resistive +/- 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/- 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.



16.2 Mechanical Dimensions of the MPC8641 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the MPC8641D (dual core) and MPC8641 (single core) high-lead FC-CBGA (package option: HCTE HX) and lead-free FC-CBGA (package option: HCTE VU) are shown respectfully in Figure 57 and Figure 58.





NOTES for Figure 57

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
- 7. All dimensions symmetrical about centerlines unless otherwise specified.



8. Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).





NOTES for Figure 58

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
- 7. All dimensions symmetrical about centerlines unless otherwise specified.
- Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).



• Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

|--|

18.3 e600 to MPX clock PLL Ratio

Table 69 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 69.

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

Table 69. e600 Core to MPX Clock Ratio

18.4 Frequency Options





Figure 59. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC8641 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC)818-842-7277 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770



System Design Information

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n \text{ RX}}[7:0]$
- SD*n*_REF_CLK
- SDn_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = $0xE_0F08$) and SRDS2CR1[0:7] register (offset = $0xE_0F44$.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 k Ω is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/LSDWE, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 k Ω) to OVDD

LSSD_MODE, TEST_MODE[0:3]. The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100- Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200- Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-k Ω pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and SENSEV_{DD}_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for SENSEV_{SS}_Core1 and needs to be connected to ground with a weak (2-10 k Ω) pull down resistor. Likewise, AV_{DD}_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."



System Design Information

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 68. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 67 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.