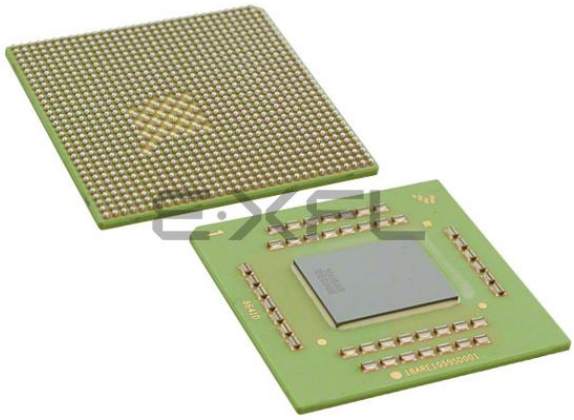

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e600 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.25GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 994-BCBGA, FCCBGA |
| Supplier Device Package | 994-FCCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641vu1250hc |

**Table 1. Absolute Maximum Ratings[1] (continued)**

| Characteristic | | Symbol | Absolute Maximum Value | Unit | Notes |
|---|---|---|---|---|---|
| Input voltage | DDR and DDR2 SDRAM signals | D*n*_$MV_{IN}$ | – 0.3 to (D*n*_$GV_{DD}$ + 0.3) | V | 5 |
| | DDR and DDR2 SDRAM reference | D*n*_$MV_{REF}$ | – 0.3 to (D*n*_$GV_{DD}$/2 + 0.3) | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to ($LV_{DD}$+ 0.3)<br>GND to ($TV_{DD}$+ 0.3) | V | 5 |
| | DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{IN}$ | GND to ($OV_{DD}$+ 0.3) | V | 5 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8641D. If two separate power supplies are used for $V_{DD}$_Core0 and $V_{DD}$_Core1, they must be kept within 100 mV of each other during normal run time.
3. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
4. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
5. During run time (M,L,T,O)$V_{IN}$ and D*n*_$MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

## 2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8641. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Cores supply voltages | $V_{DD}$_Core0,<br>$V_{DD}$_Core1 | 1.10 ± 50 mV | V | 1, 2, 8 |
| | | 1.05 ± 50 mV | | 1, 2, 7 |
| | | 0.95 ± 50 mV | | 1, 2, 12 |
| Cores PLL supply | $AV_{DD}$_Core0,<br>$AV_{DD}$_Core1 | 1.10 ± 50 mV | V | 8, 13 |
| | | 1.05 ± 50 mV | | 7, 13 |
| | | 0.95 ± 50 mV | | 12, 13 |
| SerDes Transceiver Supply (Ports 1 and 2) | $SV_{DD}$ | 1.10 ± 50 mV | V | 8, 11 |
| | | 1.05 ± 50 mV | | 7, 11 |

**Table 10. EC*n*_GTX_CLK125 AC Timing Specifications (continued)**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC*n*_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 1, 2 |

**Notes:**
1. Timing is guaranteed by design and characterization.
2. EC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC*n*_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. ±100 ppm tolerance on EC*n*_GTX_CLK125 frequency

**NOTE**

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

## 4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg\_plat\_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

## 4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_$GV_{DD}$(typ) = 2.5 V.

**Table 15. DDR SDRAM DC Electrical Characteristics for D*n*_$GV_{DD}$ (typ) = 2.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | D*n*_$GV_{DD}$ | 2.375 | 2.625 | V | 1 |
| I/O reference voltage | D*n*_$MV_{REF}$ | 0.49 × D*n*_$GV_{DD}$ | 0.51 × D*n*_$GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | D*n*_$MV_{REF}$ – 0.04 | D*n*_$MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | D*n*_$MV_{REF}$ + 0.15 | D*n*_$GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | D*n*_$MV_{REF}$– 0.15 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.95 V) | $I_{OH}$ | –16.2 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.35 V) | $I_{OL}$ | 16.2 | — | mA | — |

**Notes:**
1. D*n*_$GV_{DD}$ is expected to be within 50 mV of the DRAM D*n*_$GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to 0.5 × D*n*_$GV_{DD}$, and to track D*n*_$GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on D*n*_$MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_$MV_{REF}$. This rail should track variations in the DC level of D*n*_$MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ D*n*_$GV_{DD}$.

Table 16 provides the DDR capacitance when D*n*_$GV_{DD}$ (typ)=2.5 V.

**Table 16. DDR SDRAM Capacitance for D*n*_$GV_{DD}$ (typ) = 2.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. D*n*_$GV_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = D*n*_GVDD/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for $MV_{REF}$.

**Table 17. Current Draw Characteristics for $MV_{REF}$**

| Parameter / Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for $MV_{REF}$ | $I_{MVREF}$ | — | 500 | μA | 1 |

1. The voltage regulator for $MV_{REF}$ must be able to supply up to 500 μA current.

Figure 7 provides the AC test load for the DDR bus.

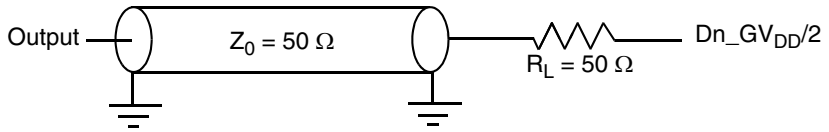



**Figure 7. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

## 7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

**Table 23. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | MPX clock/1,048,576 | baud | 1,2 |
| Maximum baud rate | MPX clock/16 | baud | 1,3 |
| Oversample rate | 16 | — | 1,4 |

**Notes:**
1. Guaranteed by design.
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

# 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving $V_{OH}$ into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$<br>$TV_{DD}$ | 3.135 | 3.465 | V | 1, 2 |
| Output high voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | — | V | — |
| Output low voltage ($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | — | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1, 2,3 |

clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 18.4.2, "Platform to FIFO Restrictions."

**NOTE**

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

A summary of the FIFO AC specifications appears in Table 26 and Table 27.

**Table 26. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period (GMII mode) | $t_{FIT}$ | 7.0 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK clock period (Encoded mode) | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK | $t_{FITDV}$ | 2.0 | — | — | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$ | 0.5 | — | 3.0 | ns |

**Table 27. FIFO Mode Receive AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period (GMII mode) | $t_{FIR}$[1] | 7.0 | 8.0 | 100 | ns |
| RX_CLK clock period (Encoded mode) | $t_{FIR}$[1] | 5.3 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIR}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

[1] ±100 ppm tolerance on RX_CLK frequency

### 8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

**Table 31. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$[2,3] | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$[3] | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise time (20%-80%) | $t_{MRXR}$[2] | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{MRXF}$[2] | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.

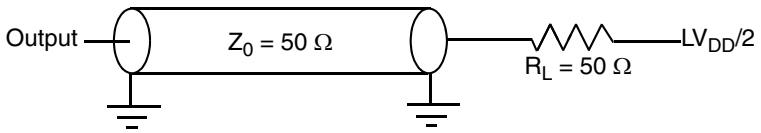



**Figure 14. eTSEC AC Test Load**

Figure 15 shows the MII receive AC timing diagram.

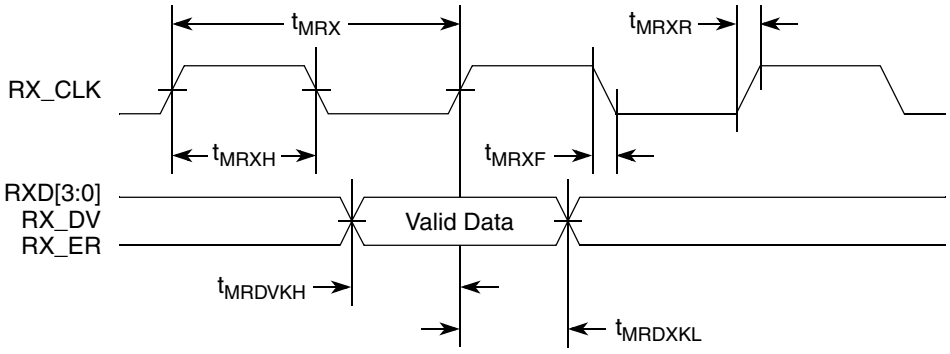



**Figure 15. MII Receive AC Timing Diagram**

### 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 34.

**Table 34. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRR}$[1] | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRR}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

[1] ±100 ppm tolerance on RX_CLK frequency

A timing diagram for TBI receive appears in Figure 18.

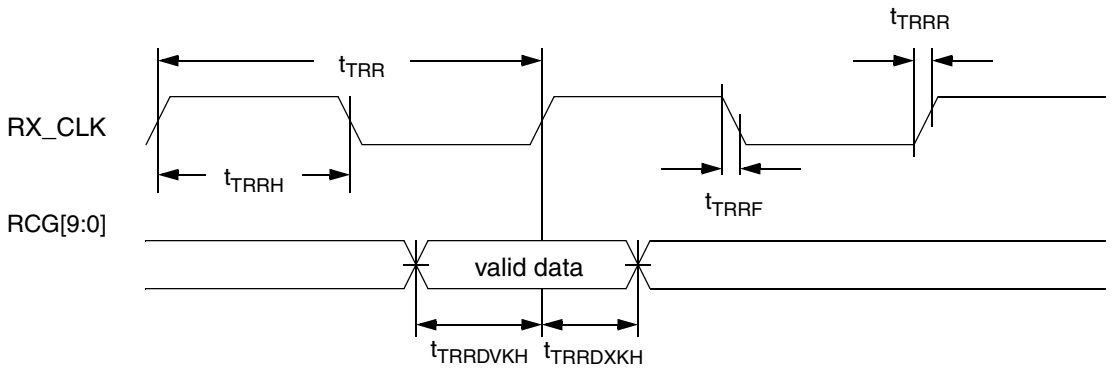



**Figure 18. TBI Single-Clock Mode Receive AC Timing Diagram**

### 8.2.6 RGMII and RTBI AC Timing Specifications

Table 35 presents the RGMII and RTBI AC timing specifications.

**Table 35. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$[5] | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |

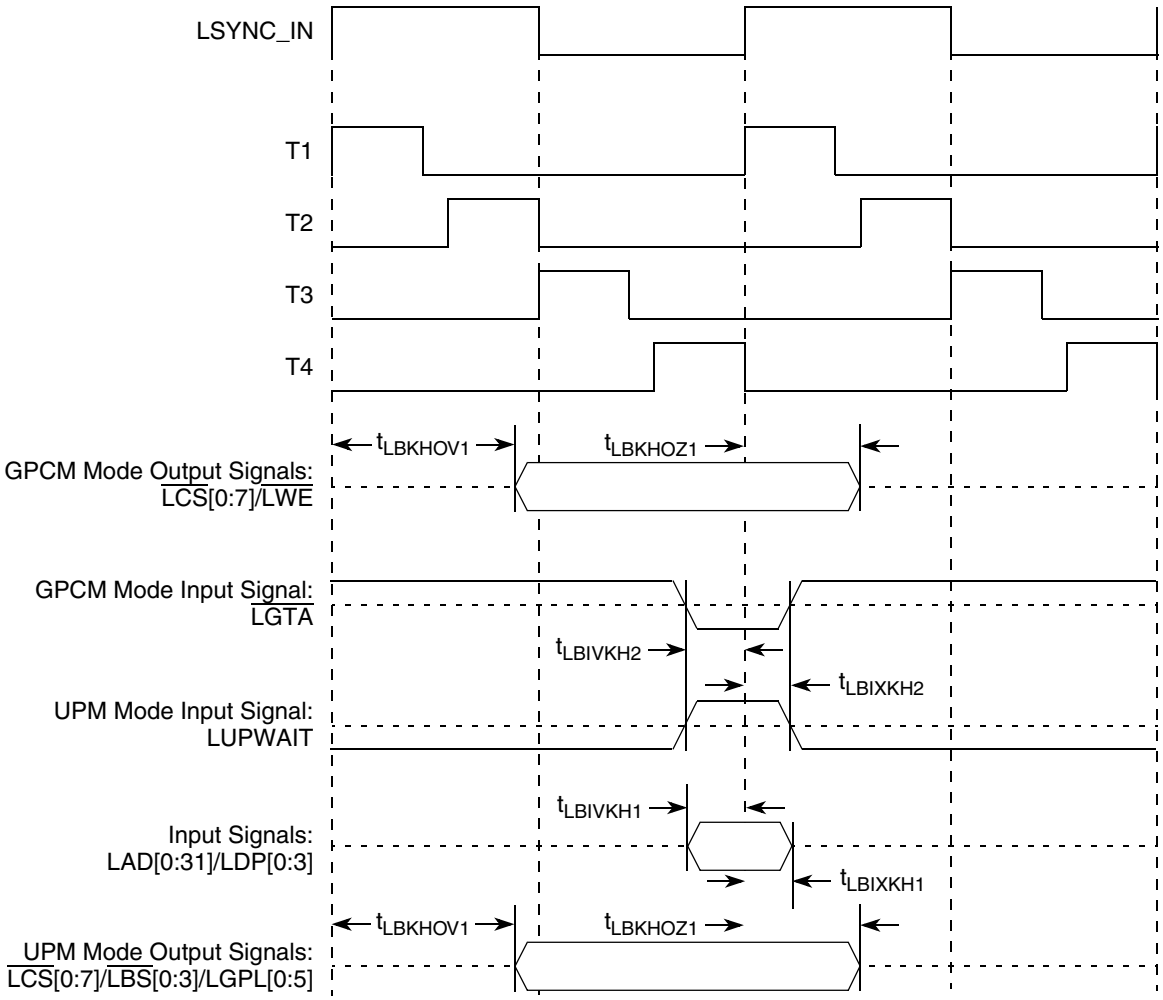



**Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)**

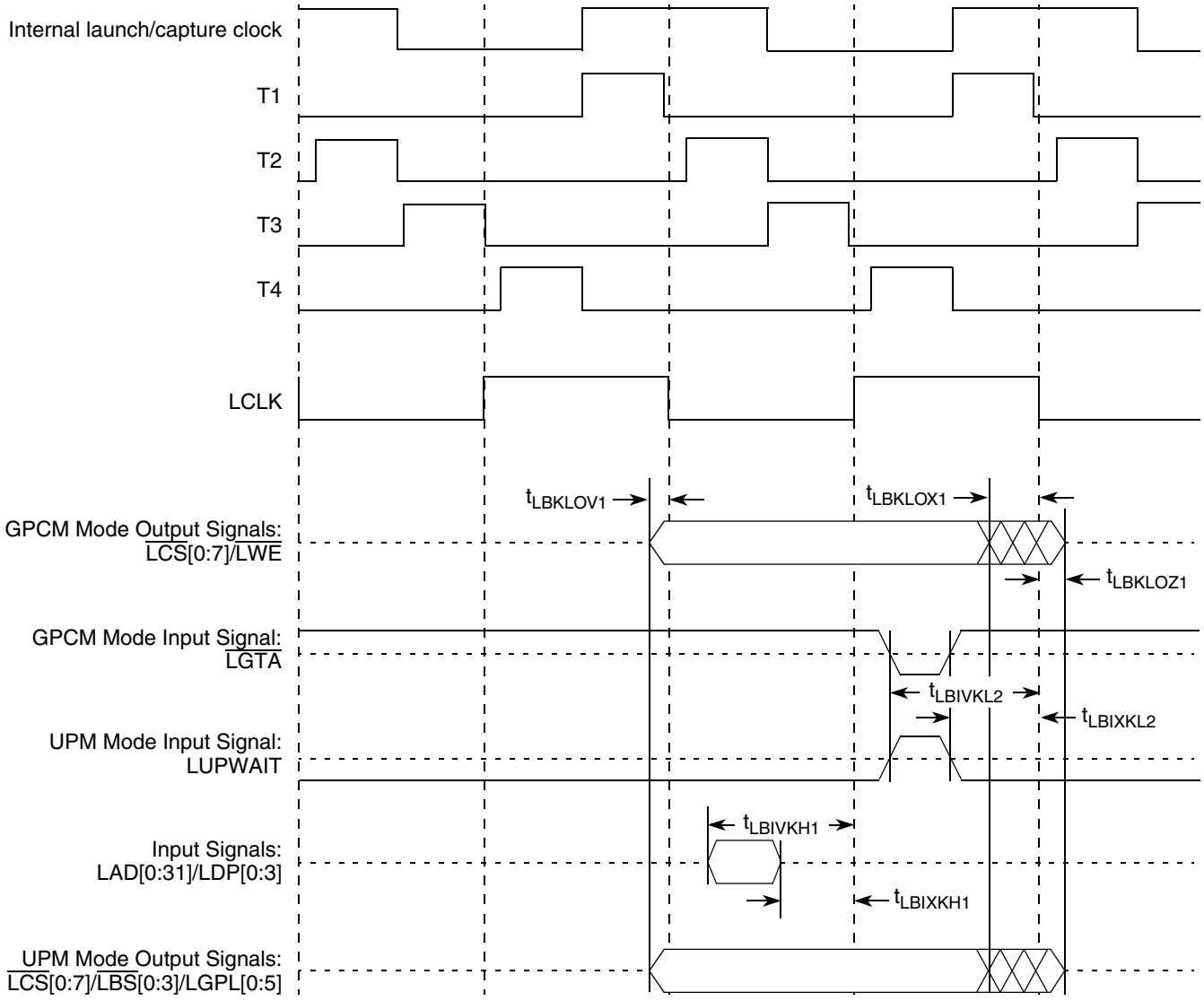



**Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)**

### 13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.

MPC8641D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8641D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

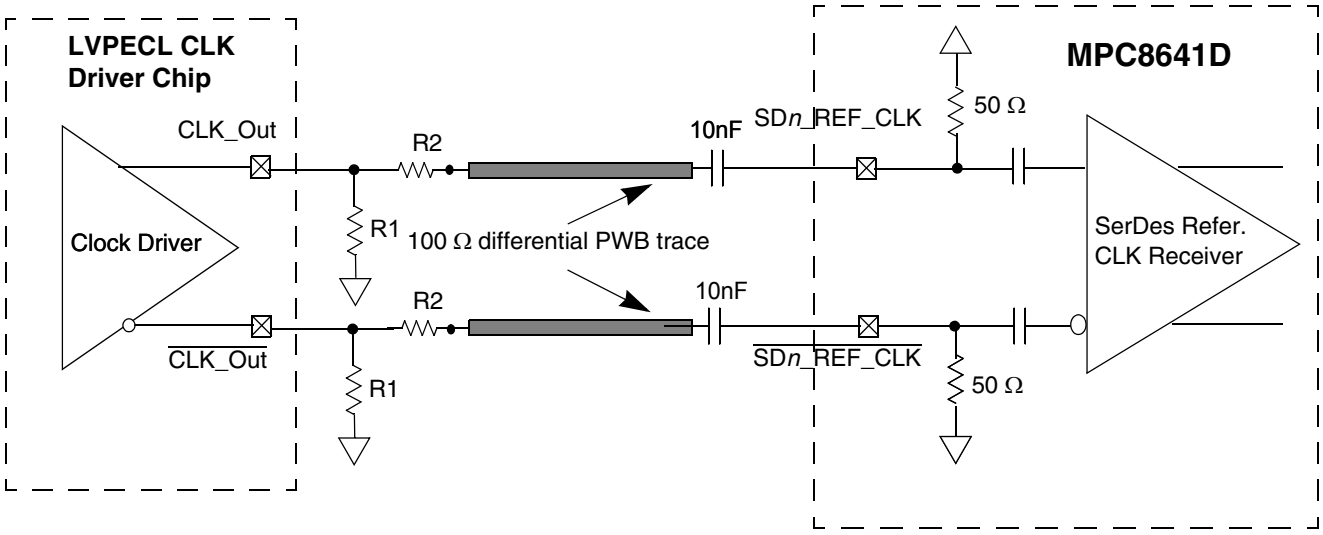



**Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

**Table 51. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10(8) | — | ns | 8 ns applies only to serial RapidIO with 125-MHz reference clock |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 80 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –40 | — | 40 | ps | — |

## 15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 53 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B Volts
2. The differential output signal of the transmitter, $V_{OD}$, is defined as $V_{TD}–V_{\overline{TD}}$
3. The differential input signal of the receiver, $V_{ID}$, is defined as $V_{RD}–V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A – B) Volts

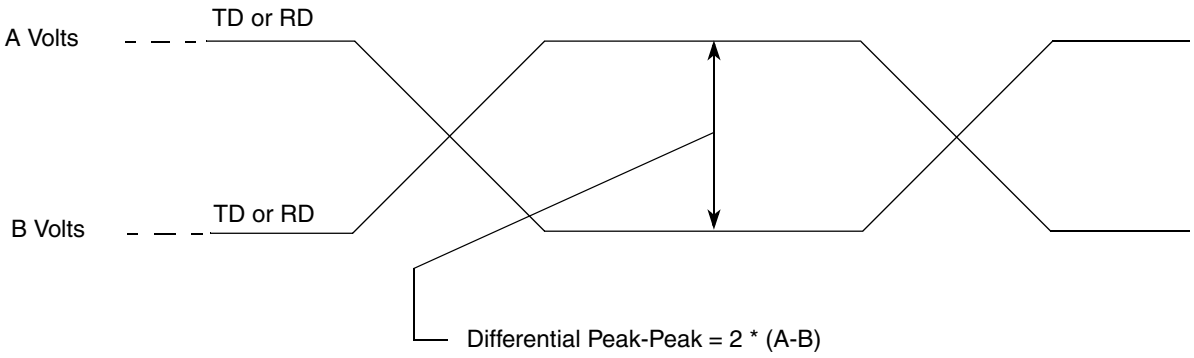



**Figure 53. Differential Peak-Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

**Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | +/– 100 ppm |

**Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple Output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | +/– 100 ppm |

**Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |

**Table 57. Long Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/– 100 ppm |

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 54 with the parameters specified in Table 58 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

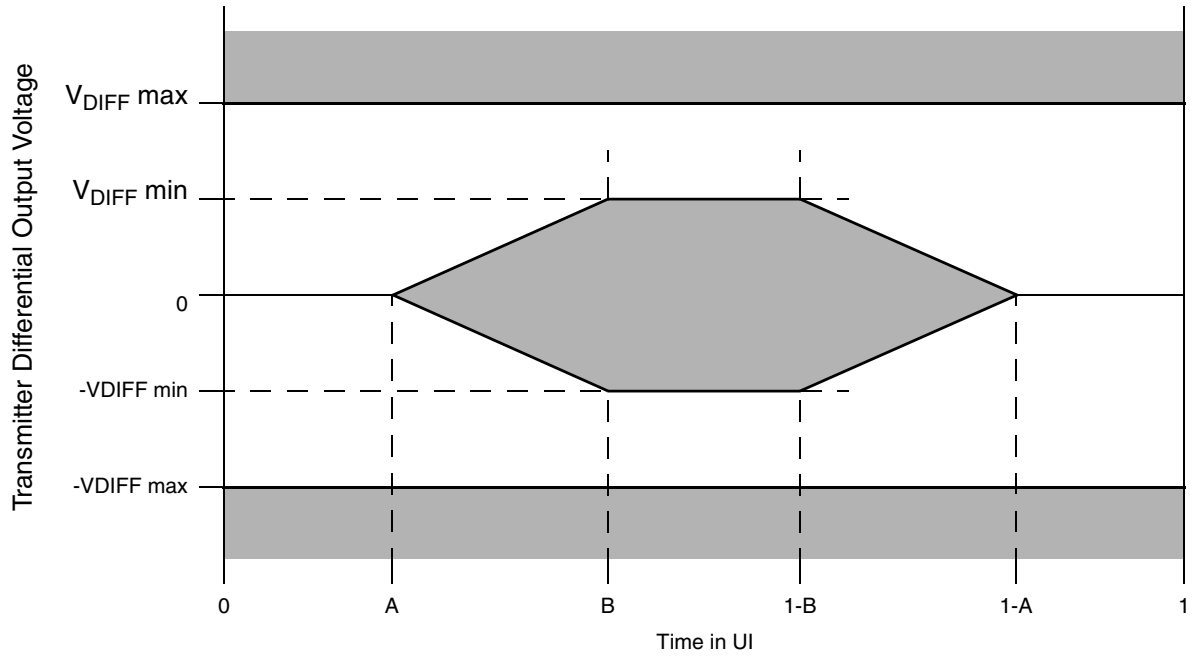



**Figure 54. Transmitter Output Compliance Mask**

## 16.2 Mechanical Dimensions of the MPC8641 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the MPC8641D (dual core) and MPC8641 (single core) high-lead FC-CBGA (package option: HCTE HX) and lead-free FC-CBGA (package option: HCTE VU) are shown respectfully in Figure 57 and Figure 58.

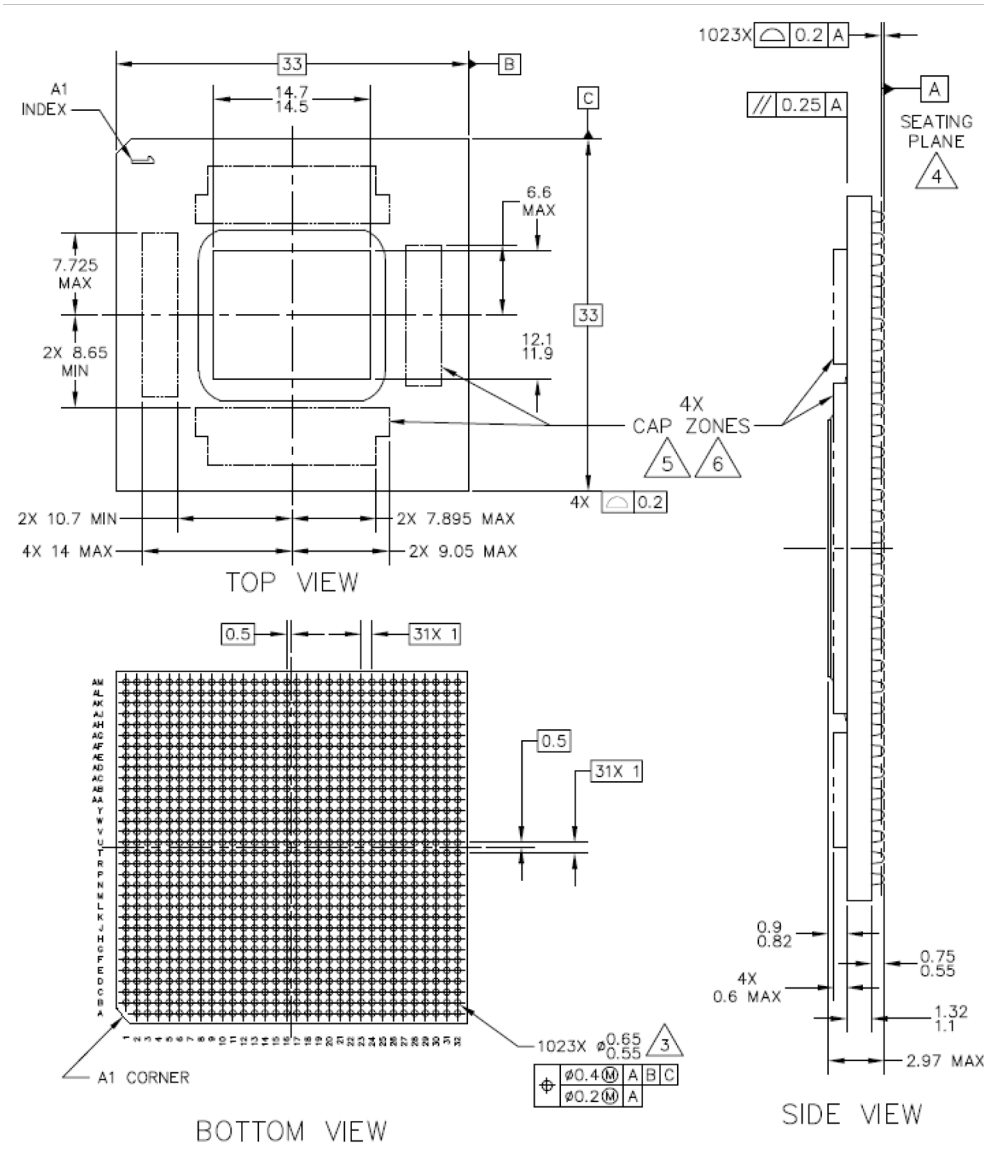



**Figure 57. MPC8641D High-Head FC-CBGA Dimensions**

**NOTES for Figure 57**

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.

### 19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 61 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 59). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

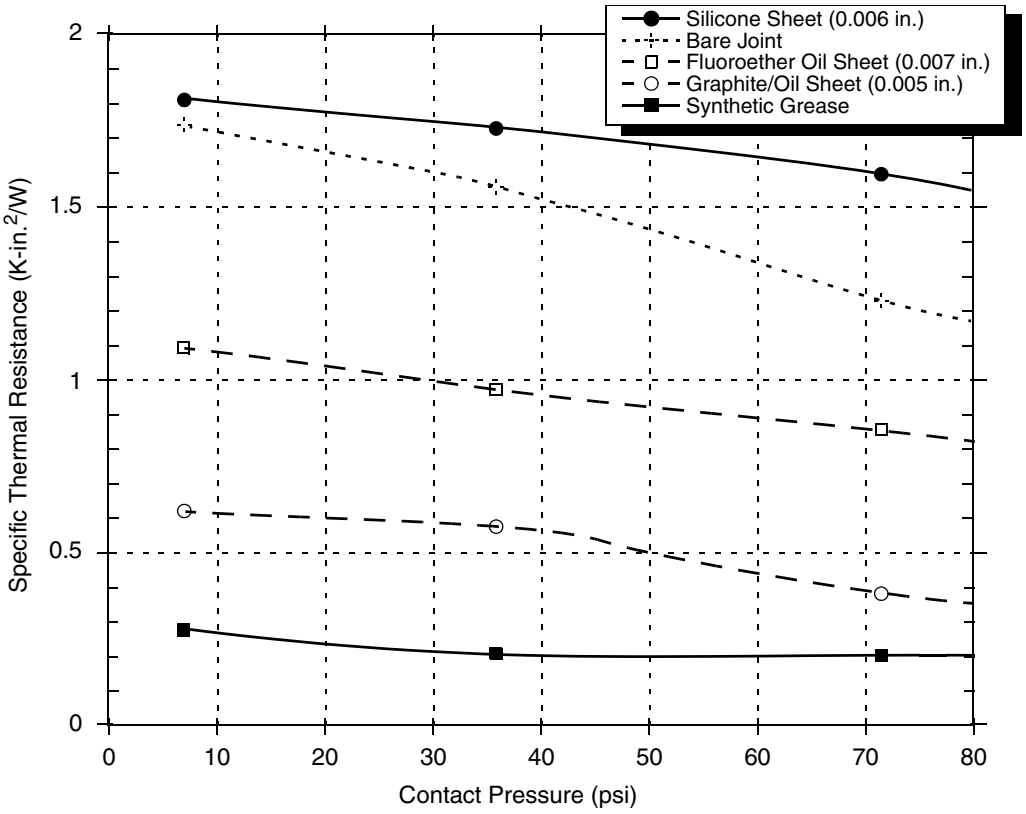



**Figure 61. Thermal Performance of Select Thermal Interface Material**

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

## 20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 kΩ) to OVDD

LSSD_MODE, TEST_MODE[0:3].The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-kΩ pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

### 20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and $\text{SENSEV}_{\text{DD}}$_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for $\text{SENSEV}_{\text{SS}}$_Core1 and needs to be connected to ground with a weak (2-10 kΩ) pull down resistor. Likewise, $\text{AV}_{\text{DD}}$_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."

# 21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

## 21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 74. Part Numbering Nomenclature**

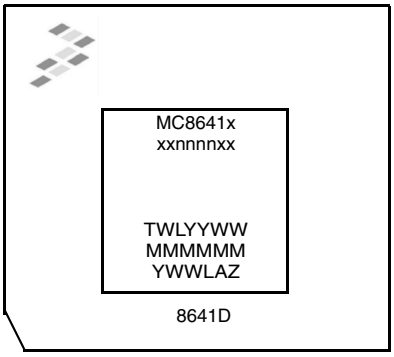
| MC | nnnn | x | xx | nnnn | x | x |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Core Count** | **Package [1]** | **Core Processor Frequency [2] (MHz)** | **DDR speed (MHz)** | **Product Revision Level** |
| MC | 8641 | Blank = Single Core<br>D = Dual Core | HX = High-lead HCTE FC-CBGA<br>VU = RoHS lead-free HCTE FC-CBGA[5]<br>VJ = lead-free HCTE FC-CBGA[6] | 1000, 1250, 1333, 1500 | N = 500 MHz[4]<br>K = 600 MHz<br>J = 533 MHz<br>H = 500 MHz<br>G = 400 MHz | Revision B = 2.0<br>System Version Register Value for Rev B:<br>0x8090_0020 - MPC8641<br>0x8090_0120 - MPC8641D<br><br>Revision C = 2.1<br>System Version Register Value for Rev C:<br>0x8090_0021 - MPC8641<br>0x8090_0121 - MPC8641D<br><br>Revision E = 3.0<br>System Version Register Value for Rev E:<br>0x8090_0030 - MPC8641<br>0x8090_0130 - MPC8641D |

**Notes:**

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low $V_{DD}$_Core*n* device. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.

## 21.2 Part Marking

Parts are marked as the example shown in Figure 70.




NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

**Figure 70. Part Marking for FC-CBGA Device**

# 22 Document Revision History

Table 76 provides a revision history for the MPC8641D hardware specification.

**Table 76. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 3 | 05/2014 | • Updated the Serial RapidIO equation in Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO”<br>• Updated Section 19.2.4, “Temperature Diode,” by removing the ideality factor value.<br>• Added VJ package type designator and footnotes to Table 74, “Part Numbering Nomenclature” and Section 16.1, “Package Parameters for the MPC8641.” |
| 2 | 07/2009 | • Added note 8 to Table 49, “Differential Transmitter (TX) Output Specifications.”<br>• Added Revision E to Table 74, “Part Numbering Nomenclature.” |
| 1 | 11/2008 | • Added Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.”<br>• Removed the statement “Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)” from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core).<br>• Added Note 8 to Figure 57 and Figure 58. |
| 0 | 07/2008 | • Initial Release |