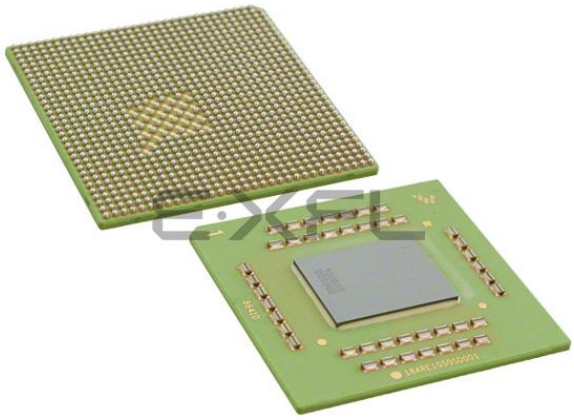

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641vu1333jb

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Absolute Maximum Value	Unit	Notes
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	– 0.3 to (D*n*_GV_{DD} + 0.3)	V	5
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	– 0.3 to (D*n*_GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to (LV_{DD}+ 0.3) GND to (TV_{DD}+ 0.3)	V	5
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to (OV_{DD}+ 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8641D. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be kept within 100 mV of each other during normal run time.
3. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
4. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
5. During run time (M,L,T,O)V_{IN} and D*n*_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8641. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	1.10 ± 50 mV	V	1, 2, 8
		1.05 ± 50 mV		1, 2, 7
		0.95 ± 50 mV		1, 2, 12
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	1.10 ± 50 mV	V	8, 13
		1.05 ± 50 mV		7, 13
		0.95 ± 50 mV		12, 13
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	1.10 ± 50 mV	V	8, 11
		1.05 ± 50 mV		7, 11

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T_J	0 to 105	°C	—

Notes:

1. Core 1 characteristics apply only to MPC8641D
2. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
3. **Caution:** D*n*_MV_{IN} must meet the overshoot/undershoot requirements for D*n*_GV_{DD} as shown in Figure 2.
4. **Caution:** L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in Figure 2 during regular run time.
5. **Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2 during regular run time.
6. Timing limitations for M,L,T,O)V_{IN} and D*n*_MV_{REF} during regular run time is provided in Figure 2
7. Applies to devices marked with a core frequency of 1333 MHz and below. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
8. Applies to devices marked with a core frequency above 1333 MHz. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
9. The 2.5 V ± 125 mV range is for DDR and 1.8 V ± 90 mV range is for DDR2.
10. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
11. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to Section 14.4.3, "Differential Receiver (RX) Input Specifications."
12. Applies to Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V devices. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for V_{DD}_Core*n* = 0.95 V.
13. This voltage is the input to the filter discussed in Section 20.2, "Power Supply Design and Sequencing," and not necessarily the voltage at the AV_{DD}_Core*n* pin, which may be reduced from V_{DD}_Core*n* by the filter.

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz	11.50	5
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz	0.0125	5
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 500 MHz	9.80	5
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

The power dissipation for the MPC8641 single core device is shown in Table 6.

Table 6. MPC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	20.3	1, 2
Thermal				105 °C	25.2	1, 3
Maxim					28.9	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	500 MHz	0.95 V, 1.05 V	65 °C	11.6	1, 2, 5
Thermal				105 °C	14.4	1, 3, 5
Maximum					16.5	1, 4, 5

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
5. These power numbers are for Part Number MC8641xx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF}+ 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. D*n*_MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 14 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock period duration [3]	t_{RGT}[5,6]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

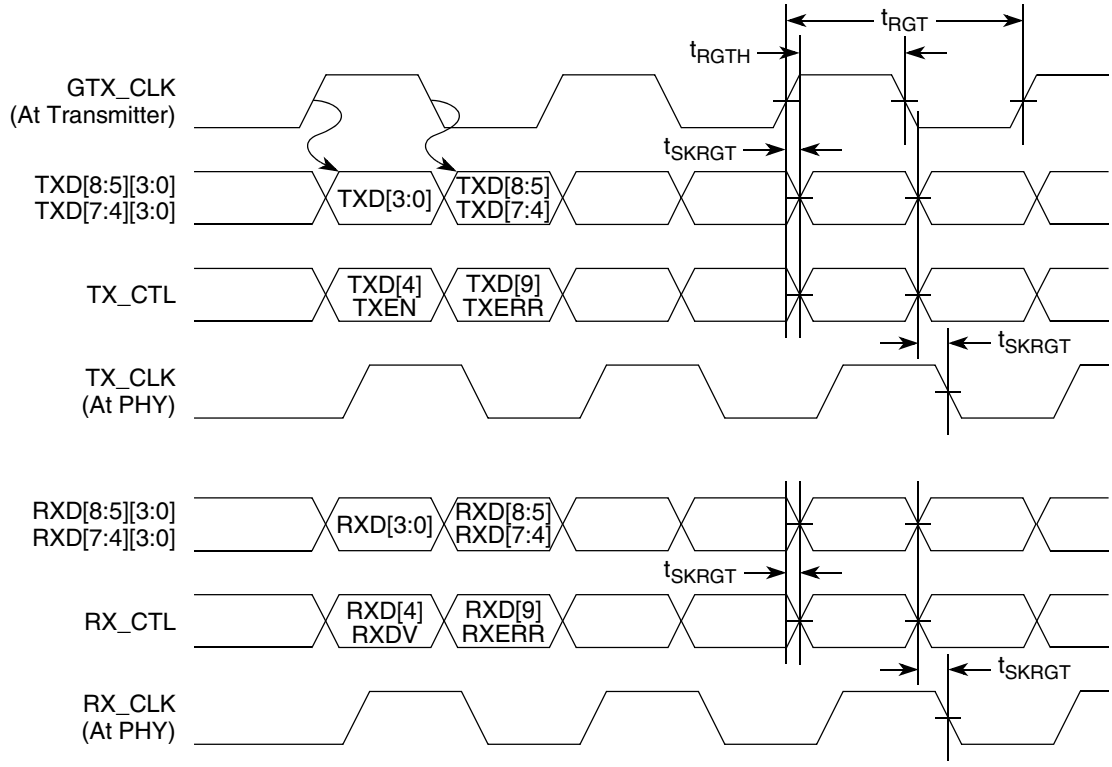

Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

Table 38. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	—	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

Table 39. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	9.3	MHz	2, 4
MDC period	t_{MDC}	80	—	400	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16*t_{MPXCLK}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	10	—	$16*t_{MPXCLK}$	ns	3, 5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—

Figure 26 to Figure 31 show the local bus signals.

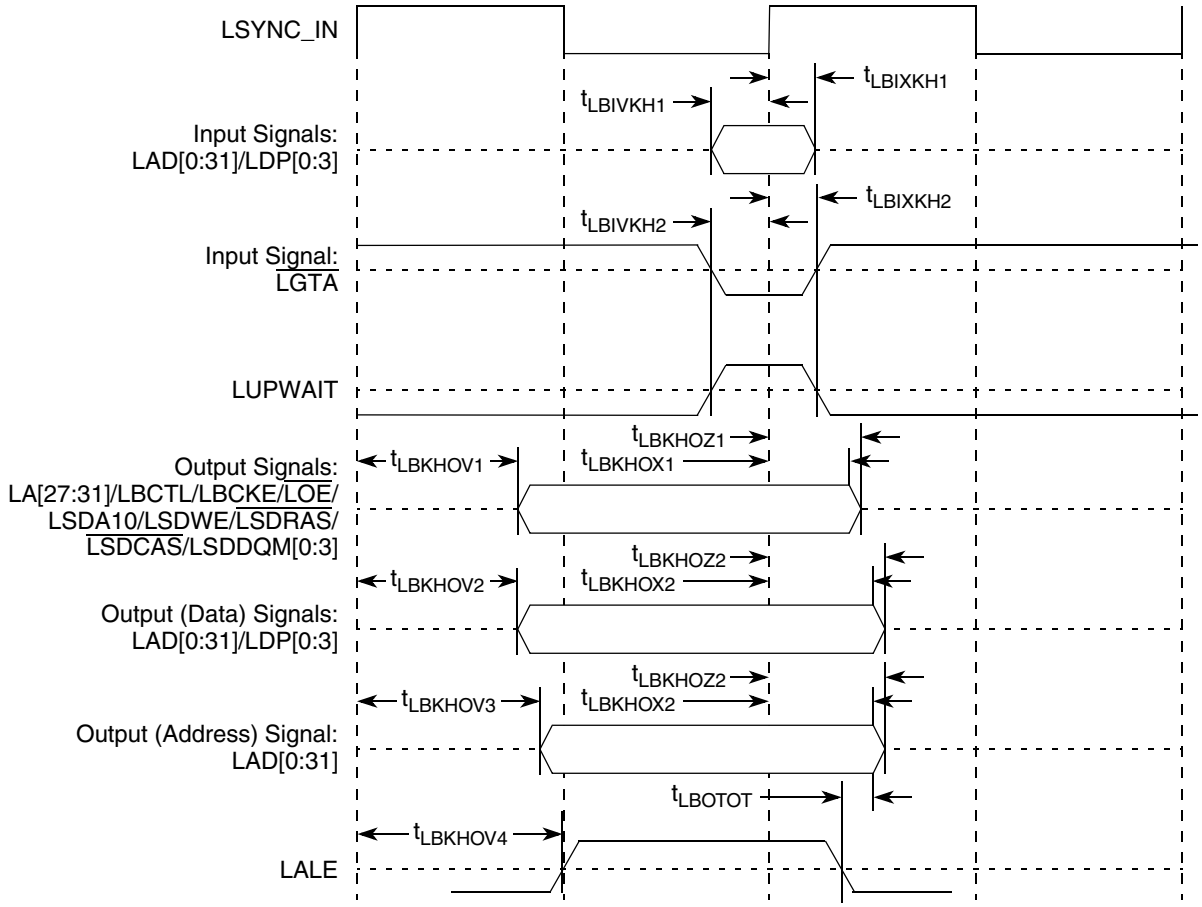

Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL bypassed.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	5.7	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5

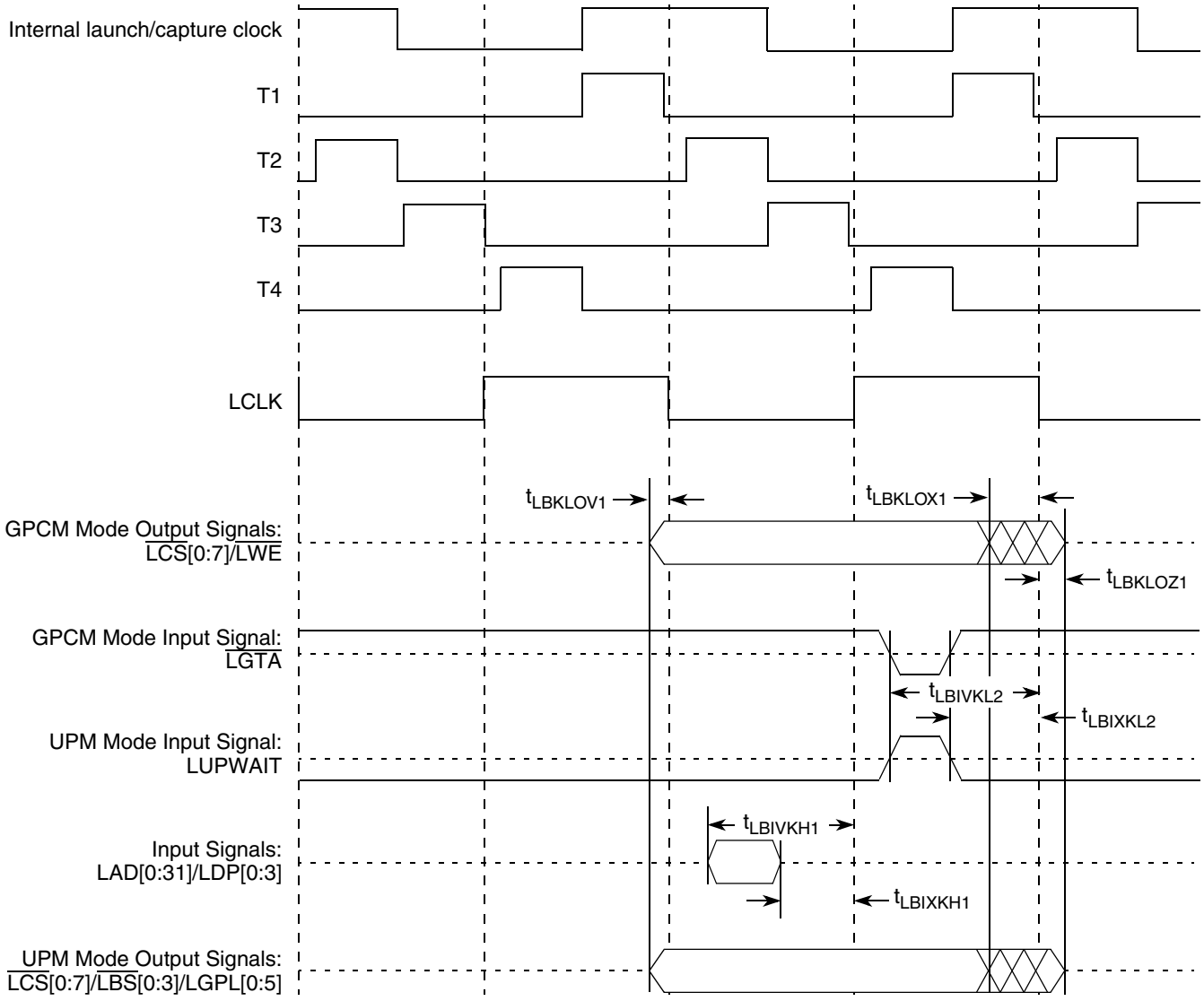

Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

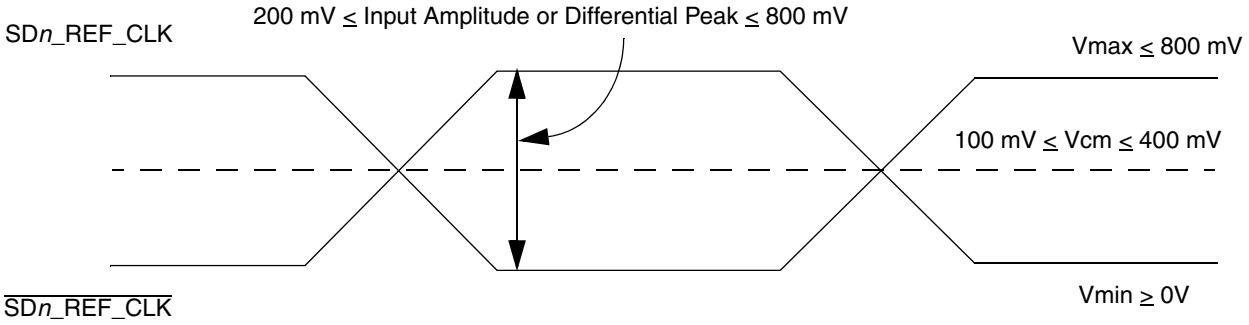

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

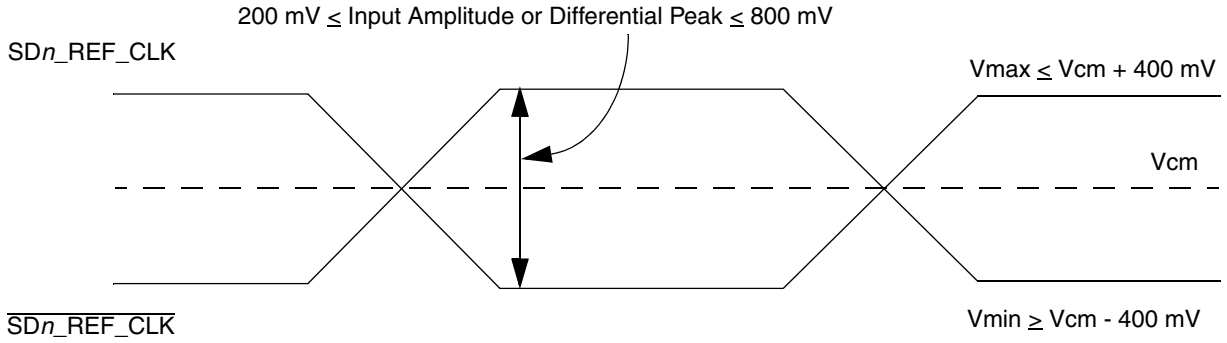

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

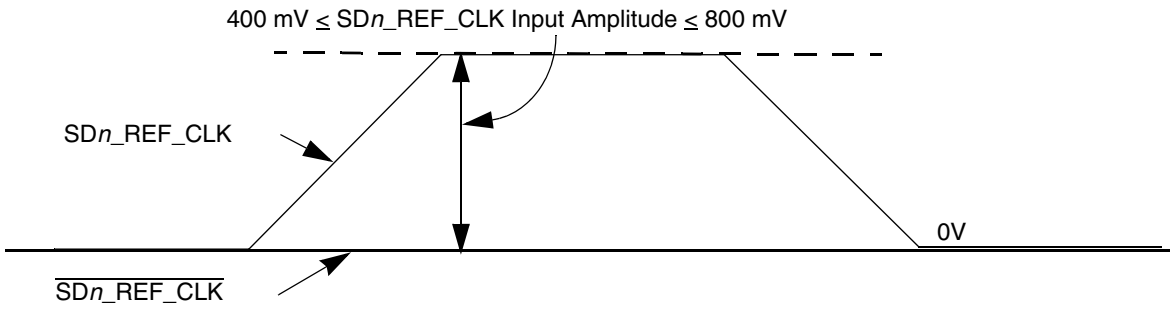

Figure 42. Single-Ended Reference Clock Input DC Requirements

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.2, "SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see Figure 52). Note that the series capacitors, C_{TX}, are optional for the return loss measurement.

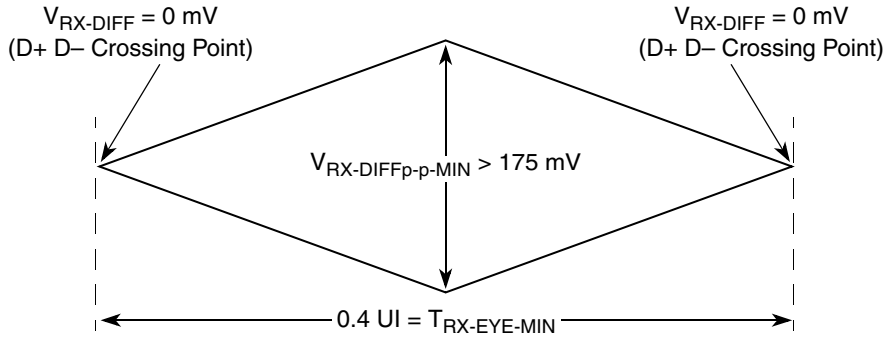

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

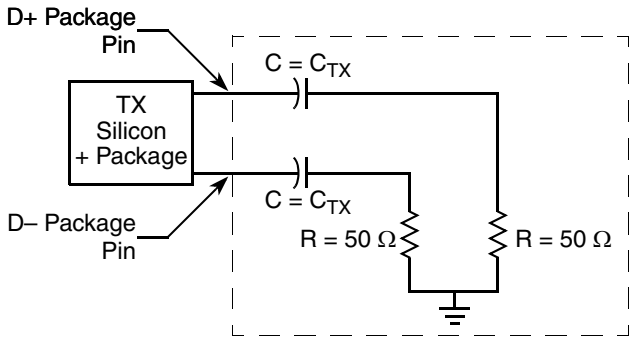

Figure 52. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 55. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 56. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

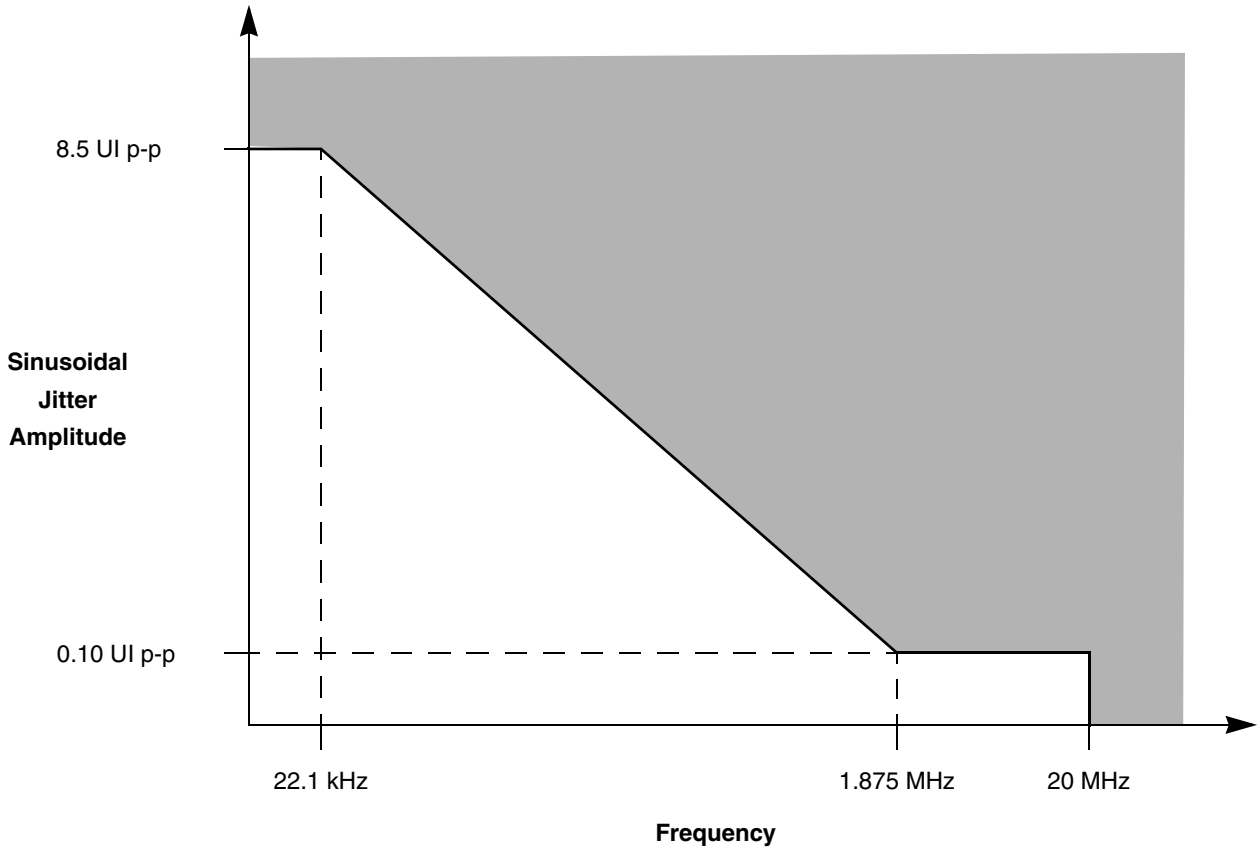

Figure 55. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 59, Table 60, Table 61) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 56 with the parameters specified in Table . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω +/– 5% differential resistive load.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$SENSEV_{SS}$_Core0	P14	Core0 GND sensing pin	—	31
$SENSEV_{SS}$_Core1	V20	Core1 GND sensing pin	—	12, 31, *S3*
$SENSEV_{DD}$_PLAT	N18	V_{DD}_PLAT sensing pin	—	28
$SENSEV_{SS}$_PLAT	P18	Platform GND sensing pin	—	29
$D1\_GV_{DD}$	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	$D1\_GV_{DD}$ 2.5 - DDR 1.8 DDR2	—
$D2\_GV_{DD}$	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	$D2\_GV_{DD}$ 2.5 V - DDR 1.8 V - DDR2	—
OV_{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD} 3.3 V	—
LV_{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV_{DD} 2.5/3.3 V	—
TV_{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV_{DD} 2.5/3.3 V	—
SV_{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV_{DD} 1.05/1.1 V	—
XV_{DD}_SRDS1	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV_{DD}_SRDS1 1.05/1.1 V	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*	—	—
Reset Configuration Signals[20]				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV_{DD}	—
TSEC1_TXD[1]/ cfg_platform_freq	AC23	—	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	—	LV_{DD}	—
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	—	LV_{DD}	—
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV_{DD}	—
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV_{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	—	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	—	LV_{DD}	—
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV_{DD}	—
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	—
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	—	LV_{DD}	—
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	—	LV_{DD}	—

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Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For