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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	994-BCBGA, FCCBGA
Supplier Device Package	994-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641vu1500kb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects support eight external slaves
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and the remote masters
 - Supports transfers to or from any local memory or I/O port
 - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compatible, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic ball grid array (FC-CBGA)



Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	TJ	0 to 105	°C	

Notes:

- 1. Core 1 characteristics apply only to MPC8641D
- 2. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
- 3. Caution: Dn_MV_{IN} must meet the overshoot/undershoot requirements for Dn_GV_{DD} as shown in Figure 2.
- 4. Caution: L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in Figure 2 during regular run time.
- 5. Caution: OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2 during regular run time.
- 6. Timing limitations for M,L,T,O)V_{IN} and Dn_MV_{REF} during regular run time is provided in Figure 2
- 7. Applies to devices marked with a core frequency of 1333 MHz and below. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
- 8. Applies to devices marked with a core frequency above 1333 MHz. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
- 9. The 2.5 V \pm 125 mV range is for DDR and 1.8 V \pm 90 mV range is for DDR2.
- 10. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
- 11. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to Section 14.4.3, "Differential Receiver (RX) Input Specifications."
- 12. Applies to Part Number MC8641xxx1000NX only. V_{DD} _Core n = 0.95 V and V_{DD} _PLAT = 1.05 V devices. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for V_{DD} _Core n = 0.95 V.
- 13. This voltage is the input to the filter discussed in Section 20.2, "Power Supply Design and Sequencing," and not necessarily the voltage at the AV_{DD}_Core*n* pin, which may be reduced from V_{DD}_Core*n* by the filter.

Electrical Characteristics

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8641.



Figure 2. Overshoot/Undershoot Voltage for Dn_M/O/L/TV_{IN}

The MPC8641 core voltage must always be provided at nominal V_{DD} _Core*n* (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and L/TV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied Dn_MV_{REF} signal (nominally set to $Dn_GV_{DD}/2$) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.



Power Characteristics

3 Power Characteristics

The power dissipation for the dual core MPC8641D device is shown in Table 4.

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD} _Coren, V _{DD} _PLAT (Volts)	Junction Temperature	Power (Watts)	Notes			
Typical				65 °C	32.1	1, 2			
Thermal	1500 MHz	600 MHz	1.1 V		43.4	1, 3			
Maximum				105 °C	49.9	1, 4			
Typical				65 °C	23.9	1, 2			
Thermal	1333 MHz	533 MHz	1.05 V		30.0	1, 3			
Maximum							105 °C	34.1	1, 4
Typical				65 °C	23.9	1, 2			
Thermal	1250 MHz	1250 MHZ 500 MHz	1.05 V		30.0	1, 3			
Maximum				105 °C	34.1	1, 4			
Typical				65 °C	23.9	1, 2			
Thermal	1000 MHz	400 MHz	1.05 V		30.0	1, 3			
Maximum				105 °C	34.1	1, 4			
Typical			/	65 °C	16.2	1, 2, 5			
Thermal	1000 MHz	500 MHz	0.95 V, 1.05 V		21.8	1, 3, 5			
Maximum				105 °C	25.0	1, 4, 5			

Table 4. MPC8641D Power Dissipation (Dual Core)

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.

- Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
- 3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
- 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
- 5. These power numbers are for Part Number MC8641Dxx1000NX only. V_{DD} -Coren = 0.95 V and V_{DD} -PLAT = 1.05 V.



4 Input Clocks

Table 7 provides the system clock (SYSCLK) DC specifications for the MPC8641.

Table 7. SYSCLK DC Electrical Characteristics (OVDD = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD})$	I _{IN}		±5	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	fsysclk	66	—	166.66	MHz	1
SYSCLK cycle time	t _{SYSCLK}	6	—	_	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	_			150	ps	4, 5

Notes:

- Caution: The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the short term jitter only and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter



6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is $Dn_GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $Dn_GV_{DD}(typ) = 1.8$ V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when $Dn_GV_{DD}(typ) = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	1.71	1.89	V	1
I/O reference voltage	Dn_MV _{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 imes Dn_{DD}$	V	2
I/O termination voltage	V _{TT}	D <i>n</i> _MV _{REF} – 0.0 4	D <i>n_</i> MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	D <i>n_</i> MV _{REF} + 0.1 25	D <i>n_</i> GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	D <i>n</i> _MV _{REF} - 0.125	V	_
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	_	mA	_
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 13. DDR2 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 1.8 V

Notes:

1. $Dn_{GV_{DD}}$ is expected to be within 50 mV of the DRAM $Dn_{GV_{DD}}$ at all times.

2. Dn_MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF}. This rail should track variations in the DC level of Dn_MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq Dn_GV_{DD}.

Table 14 provides the DDR2 capacitance when $Dn_{GV_{DD}(typ)} = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

DDR and DDR2 SDRAM

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when $Dn_GV_{DD}(typ) = 2.5 \text{ V}.$

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	2.375	2.625	V	1
I/O reference voltage	Dn_MV _{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V _{TT}	D <i>n</i> _MV _{REF} – 0.04	D <i>n</i> _MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	D <i>n</i> _MV _{REF} + 0.15	D <i>n</i> _GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	D <i>n</i> _MV _{REF} - 0.15	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-16.2	—	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	16.2	_	mA	—

Table	15 DDR	SDRAM DC	Electrical	Characteristics	for Dn	GV	(tvn)	- 251	/
lable	15. DDn	SURAW DC	Electrical	Characteristics			(LYP)	= 2.5	

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

2. MV_{REF} is expected to be equal to $0.5 \times Dn_{GV_{DD}}$, and to track $Dn_{GV_{DD}}$ DC variations as measured at the receiver. Peak-to-peak noise on $Dn_{MV_{REF}}$ may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF}. This rail should track variations in the DC level of Dn_MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq D*n*_GV_{DD}.

Table 16 provides the DDR capacitance when $Dn \text{ } \text{GV}_{DD}$ (typ)=2.5 V.

Table 16. DDR SDRAM Capacitance for Dn_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = Dn_GVDD/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV_{REF} .

Table 17. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.



8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.135	3.465	V	1, 2
Output high voltage $(LV_{DD}/TV_{DD} = Min, I_{OH} = -4.0 \text{ mA})$	V _{OH}	2.40	_	V	—
Output low voltage $(LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 \text{ mA})$	V _{OL}	_	0.50	V	_
Input high voltage	V _{IH}	2.0	—	V	_
Input low voltage	V _{IL}	—	0.90	V	_
Input high current $(V_{IN} = LV_{DD}, V_{IN} = TV_{DD})$	IIH	_	40	μA	1, 2,3

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Мах	Unit	Notes
Input low current (V _{IN} = GND)	Ι _{ΙL}	-600	_	μA	3

Notes:

¹ LV_{DD} supports eTSECs 1 and 2.

² TV_{DD} supports eTSECs 3 and 4.

³ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.375	2.625	V	1,2
Output high voltage $(LV_{DD}/TV_{DD} = Min, I_{OH} = -1.0 mA)$	V _{OH}	2.00	_	V	_
Output low voltage ($LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA$)	V _{OL}	—	0.40	V	—
Input high voltage	V _{IH}	1.70	—	V	—
Input low voltage	V _{IL}	—	0.90	V	—
Input high current $(V_{IN} = LV_{DD}, V_{IN} = TV_{DD})$	IIH	—	10	μA	1, 2,3
Input low current (V _{IN} = GND)	I _{IL}	-15	—	μA	3

Note:

 $^1\,$ LV_{DD} supports eTSECs 1 and 2.

² TV_{DD} supports eTSECs 3 and 4.

³ Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 29. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock fall time (80%-20%)	t _{GRXF} 2		_	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

2. Guaranteed by design.

3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.



Figure 11. eTSEC AC Test Load

Figure 12 shows the GMII receive AC timing diagram.



Figure 12. GMII Receive AC Timing Diagram



10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD} = 3.3 \text{ V}$ DC.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = OV_{DD})$	I _{IN}	_	±5	μA
High-level output voltage (OV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	OV _{DD} – 0.2	_	V
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.2	V

Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL enabled. For information about the frequency range of local bus see Section 18.1, "Clock Ranges."

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	—	ns	2
Local Bus Duty Cycle	t _{LBKH} /t _{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.2	ns	—
Local bus clock to address valid for LAD	t _{LBKHOV3}		2.3	ns	_

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled



Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to LALE assertion	t _{LBKHOV4}	_	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	—
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}		2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.5	ns	5

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled (continued)

Note:

- The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Figure 25 provides the AC test load for the local bus.



Figure 25. Local Bus AC Test Load



Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8641D SerDes reference clock input's DC requirement.



Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8641D SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features $50-\Omega$ termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with



PCI Express

Table 49. Differential Transmitter	· (TX) Output S	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Мах	Units	Comments
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set		_	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
RL _{TX-DIFF}	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL _{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
Z _{TX-DIFF-DC}	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z _{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
L _{TX-SKEW}	Lane-to-Lane Output Skew	_	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C _{TX}	AC Coupling Capacitor	75	—	—	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.
T _{crosslink}	Crosslink Random Timeout	0			ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.

- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
- 8. MPC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.



Serial RapidIO

Characteristic	Symbol	Ra	nge	Unit	Notes
Characteristic	Symbol	Min	Мах	Onit	Notes
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic Jitter	J _D	—	0.17	UI p-p	—
Total Jitter	J _T	—	0.35	UI p-p	—
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notes
Characteristic	Symbol	Min	Мах	Onic	Notes
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic Jitter	J _D	—	0.17	UI p-p	—
Total Jitter	J _T	—	0.35	UI p-p	—
Multiple Output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notes
Unaracteristic	Symbol	Min	Max		Notes
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic Jitter	J _D	—	0.17	UI p-p	—
Total Jitter	J _T	—	0.35	UI p-p	—



19 Thermal

This section describes the thermal specifications of the MPC8641.

19.1 Thermal Characteristics

Table 71 provides the package thermal characteristics for the MPC8641.

Table 71. Package Thermal Characteristics¹

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{ ext{ heta}JA}$	18	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	R_{\thetaJA}	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	R_{\thetaJMA}	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	R_{\thetaJMA}	9	°C/W	1, 3
Junction-to-board thermal resistance	R_{\thetaJB}	5	°C/W	4
Junction-to-case thermal resistance	$R_{ ext{ heta}JC}$	< 0.1	°C/W	5

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

- 2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
- 3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

19.2 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8641 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 19.2.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 59 shows a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.





Note: For single core device the filter circuit (in the dashed box) should be removed and AV_{DD} _Core1 should be tied to ground with a weak (2-10 k Ω) pull-down resistor.

Figure 64. MPC8641 PLL Power Supply Filter Circuit (for cores)

The AV_{DD}_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003- μ F capacitor is closest to the balls, followed by the two 2.2- μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 65. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS*n* should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the SV_{DD} power plan.

20.2.2 PLL Power Supply Sequencing

For details on power sequencing for the AV_{DD} type and supplies refer to Section 2.2, "Power Up/Down Sequence."

20.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system



System Design Information

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 68. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 67 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.



The COP interface has a standard header, shown in Figure 67, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 67; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 67 is common to all known emulators.

For a multi-processor non-daisy chain configuration, Figure 68, can be duplicated for each processor. The recommended daisy chain configuration is shown in Figure 69. Please consult with your tool vendor to determine which configuration is supported by their emulator.

20.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 68. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



Figure 67. COP Connector Physical Pinout



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