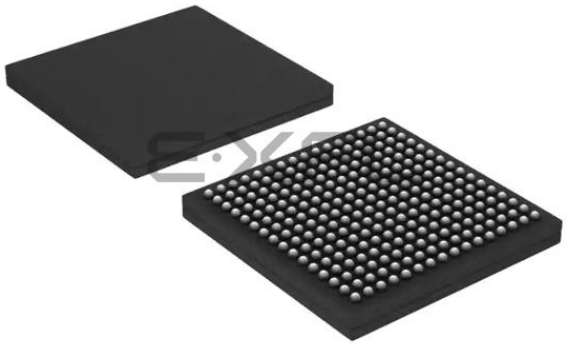

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM9® |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | EBI/EMI, IrDA, Microwire, Memory Card, SmartCard, SPI, SSI, SSP, UART/USART, USB |
| Peripherals | AC'97, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 60 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LFBGA |
| Supplier Device Package | 256-LFBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lh7a400n0f000b5-55 |

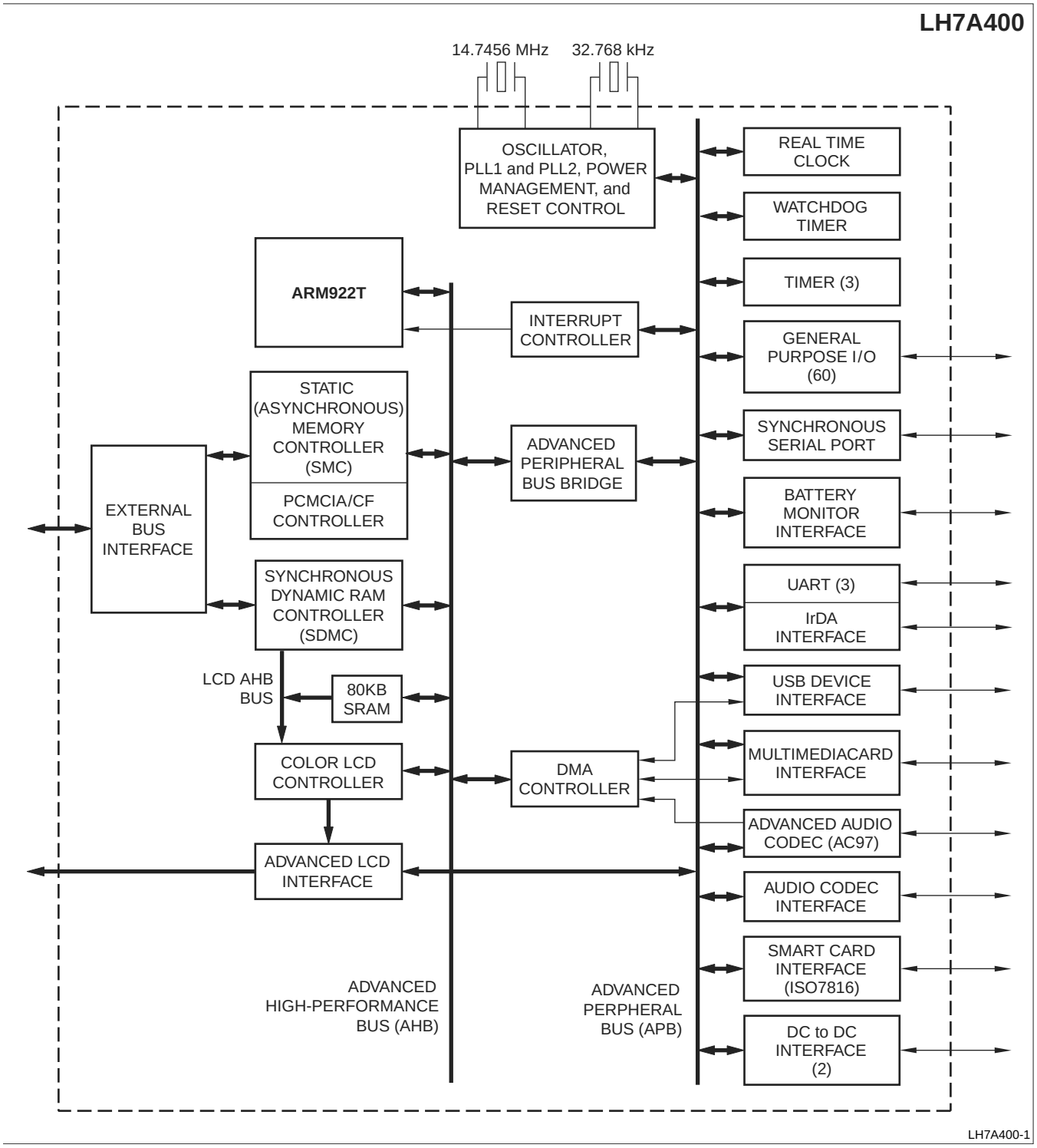



**Figure 1. LH7A400 block diagram**

**Table 3. Functional Pin List (Cont'd)**

| BGA PIN | LFBGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE | I/O | NOTES |
|---|---|---|---|---|---|---|---|---|
| C13 | B13 | D26 | Data Bus | LOW | LOW | 12 mA | I/O | |
| E12 | B14 | D27 | | | | | | |
| G10 | C12 | D28 | | | | | | |
| B12 | A14 | D29 | | | | | | |
| B11 | B12 | D30 | | | | | | |
| D11 | A12 | D31 | | | | | | |
| M16 | M15 | A0/nWE1 | • Asynchronous Address Bus<br>• Asynchronous Memory Write Byte Enable 1 | HIGH: nWE1 | HIGH | 12 mA | O | |
| N14 | M16 | A1/nWE2 | • Asynchronous Address Bus<br>• Asynchronous Memory Write Byte Enable 2 | HIGH: nWE2 | HIGH | 12 mA | O | |
| M13 | L15 | A2/SA0 | • Asynchronous Address Bus<br>• Synchronous Address Bus | LOW | LOW | 12 mA | O | |
| K16 | K12 | A3/SA1 | | | | | | |
| K15 | K13 | A4/SA2 | | | | | | |
| K14 | K16 | A5/SA3 | | | | | | |
| J8 | J13 | A6/SA4 | | | | | | |
| J16 | J11 | A7/SA5 | | | | | | |
| J14 | J16 | A8/SA6 | | | | | | |
| J9 | H15 | A9/SA7 | | | | | | |
| H16 | H10 | A10/SA8 | | | | | | |
| H14 | H12 | A11/SA9 | | | | | | |
| G16 | G15 | A12/SA10 | | | | | | |
| G14 | G10 | A13/SA11 | | | | | | |
| G13 | G11 | A14/SA12 | | | | | | |
| F16 | F16 | A15/SA13 | | | | | | |
| F14 | E16 | A16/SB0 | • Async Address Bus<br>• Sync Device Bank Address 0 | LOW | LOW | 12 mA | O | |
| E16 | F13 | A17/SB1 | • Async Address Bus<br>• Sync Device Bank Address 1 | LOW | LOW | 12 mA | O | |
| E13 | E14 | A18 | Asynchronous Address Bus | LOW | LOW | 12 mA | O | |
| F11 | D15 | A19 | | | | | | |
| D15 | C16 | A20 | | | | | | |
| C16 | C15 | A21 | | | | | | |
| B16 | C14 | A22 | | | | | | |
| A15 | B15 | A23 | | | | | | |
| A13 | E11 | A24 | | | | | | |
| G8 | D8 | A25/SCIO | • Async Memory Address Bus<br>• Smart Card Interface I/O (Data) | LOW: A25 | LOW | 12 mA | I/O | |
| F8 | B7 | A26/SCCLK | • Async Memory Address Bus<br>• Smart Card Interface Clock | LOW: A26 | LOW | 12 mA | I/O | |
| A8 | A7 | A27/SCRST | • Async Memory Address Bus<br>• Smart Card Interface Reset | LOW: A27 | LOW | 12 mA | O | |
| D8 | C8 | nOE | Async Memory Output Enable | HIGH | No Change | 12 mA | O | |
| C8 | F8 | nWE0 | Async Memory Write Byte Enable 0 | HIGH | No Change | 12 mA | O | |
| D10 | D9 | nWE3 | Async Memory Write Byte Enable 3 | HIGH | No Change | 8 mA | O | |
| B10 | E9 | CS6/SCKE1_2 | • Async Memory Chip Select 6<br>• Sync Memory Clock Enable 1 or 2 | LOW: CS6 | No Change | 12 mA | O | |
| C10 | A10 | CS7/SCKE0 | • Async Memory Chip Select 7<br>• Sync Memory Clock Enable 0 | LOW: CS7 | No Change | 12 mA | O | |
| G9 | A11 | SCKE3 | Sync Memory Clock Enable 3 | LOW | LOW | 12 mA | O | |
| A10 | B10 | SCLK | Sync Memory Clock | LOW | No Change | | I/O | 2 |
| C14 | C13 | nSCS0 | Sync Memory Chip Select 0 | HIGH | No Change | 12 mA | O | |

**Table 3. Functional Pin List (Cont'd)**

| BGA PIN | LFBGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE | I/O | NOTES |
|---|---|---|---|---|---|---|---|---|
| D13 | A15 | nSCS1 | Sync Memory Chip Select 1 | HIGH | No Change | 12 mA | O | |
| E11 | D11 | nSCS2 | Sync Memory Chip Select 2 | HIGH | No Change | 12 mA | O | |
| A12 | E10 | nSCS3 | Sync Memory Chip Select 3 | HIGH | No Change | 12 mA | O | |
| C12 | A13 | nSWE | Sync Memory Write Enable | HIGH | No Change | 12 mA | O | |
| C11 | B11 | nCAS | Sync Memory Column Address Strobe Signal | HIGH | No Change | 12 mA | O | |
| F9 | C11 | nRAS | Sync Memory Row Address Strobe Signal | HIGH | No Change | 12 mA | O | |
| A9 | C9 | DQM0 | Sync Memory Data Mask 0 | HIGH | No Change | 12 mA | O | |
| B9 | A9 | DQM1 | Sync Memory Data Mask 1 | HIGH | No Change | 12 mA | O | |
| D9 | B9 | DQM2 | Sync Memory Data Mask 2 | HIGH | No Change | 12 mA | O | |
| E9 | A8 | DQM3 | Sync Memory Data Mask 3 | HIGH | No Change | 12 mA | O | |
| J5 | K1 | PA0/LCDVD16 | • GPIO Port A<br>• LCD Data bit 16. This CLCDC output signal is always LOW. | Input: PA0 | No Change | 8 mA | I/O | |
| K1 | K2 | PA1/LCDVD17 | • GPIO Port A<br>• LCD Data bit 17. This CLCDC output signal is always LOW. | Input: PA1 | No Change | 8 mA | I/O | |
| K2 | K3 | PA2 | GPIO Port A | Input | No Change | 8 mA | I/O | |
| K3 | K4 | PA3 | | | | | I/O | |
| K5 | K6 | PA4 | | | | | I/O | |
| L1 | K5 | PA5 | | | | | I/O | |
| L2 | L1 | PA6 | | | | | I/O | |
| L3 | L2 | PA7 | | | | | I/O | |
| L4 | L3 | PB0/ UARTRX1 | • GPIO Port B<br>• UART1 Receive Data Input | Input: PB0 | No Change | 8 mA | I/O | |
| L5 | M1 | PB1/UARTTX3 | • GPIO Port B<br>• UART3 Transmit Data Out | Input: PB1 | LOW if PINMUX: UART3CON = 1 (bit 3); otherwise No Change | 8 mA | I/O | |
| L7 | M2 | PB2/ UARTRX3 | • GPIO Port B<br>• UART3 Receive Data In | Input: PB2 | No Change | 8 mA | I/O | |
| M2 | M3 | PB3/ UARTCTS3 | • GPIO Port B<br>• UART3 Clear to Send | Input: PB3 | No Change | 8 mA | I/O | |
| M4 | L5 | PB4/ UARTDCD3 | • GPIO Port B<br>• UART3 Data Carrier Detect | Input: PB4 | No Change | 8 mA | I/O | |
| N1 | N1 | PB5/ UARTDSR3 | • GPIO Port B<br>• UART3 Data Set Ready | Input: PB5 | No Change | 8 mA | I/O | |
| N2 | N2 | PB6/SWID/ SMBD | • GPIO Port B<br>• Single Wire Data<br>• Smart Battery Data | Input: PB6 | No Change | 8 mA | I/O | |
| N3 | M4 | PB7/ SMBCLK | • GPIO Port B<br>• Smart Battery Clock | Input: PB7 | No Change | 8 mA | I/O | 7 |
| P1 | P1 | PC0/ UARTTX1 | • GPIO Port C<br>• UART1 Transmit Data Output | LOW: PC0 | No Change | 12 mA | I/O | |
| P2 | P2 | PC1/LCDPS | • GPIO Port C<br>• HR-TFT Power Save | LOW: PC1 | No Change | 12 mA | I/O | |
| R1 | R1 | PC2/ LCDVDDEN | • GPIO Port C<br>• HR-TFT Power Sequence Control | LOW: PC2 | No Change | 12 mA | I/O | |
| K6 | M5 | PC3/LCDREV | • GPIO Port C<br>• HR-TFT Gray Scale Voltage Reverse | LOW: PC3 | No Change | 12 mA | I/O | |
| L8 | P3 | PC4/ LCDSPS | • GPIO Port C<br>• HR-TFT Reset Row Driver Counter | LOW: PC4 | No Change | 12 mA | I/O | |

**Table 3. Functional Pin List (Cont'd)**

| BGA PIN | LFBGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE | I/O | NOTES |
|---|---|---|---|---|---|---|---|---|
| T1 | N4 | PC5/ LCDCLS | • GPIO Port C<br>• HR-TFT Row Driver Clock | LOW: PC5 | No Change | 12 mA | I/O | |
| T2 | R2 | PC6/LCDHR-LP | • GPIO Port C<br>• LCD Latch Pulse | LOW: PC6 | No Change | 12 mA | I/O | |
| R2 | N5 | PC7/ LCDSPL | • GPIO Port C<br>• LCD Start Pulse Left | LOW: PC7 | No Change | 12 mA | I/O | |
| M11 | M9 | PD0/LCDVD8 | • GPIO Port D<br>• LCD Video Data Bus | LOW: PD0 | LOW if PINMUX: PDOCON = 1 (bit 1); otherwise, No Change | 12 mA | I/O | |
| L11 | K10 | PD1/LCDVD9 | | LOW: PD1 | | | I/O | |
| K8 | P10 | PD2/LCDVD10 | | LOW: PD2 | | | I/O | |
| N11 | T11 | PD3/LCDVD11 | | LOW: PD3 | | | I/O | |
| R9 | T12 | PD4/LCDVD12 | | LOW: PD4 | | | I/O | |
| T9 | R11 | PD5/LCDVD13 | | LOW: PD5 | | | I/O | |
| P10 | R12 | PD6/LCDVD14 | | LOW: PD6 | | | I/O | |
| R10 | T13 | PD7/LCDVD15 | | LOW: PD7 | | | I/O | |
| L10 | T9 | PE0/LCDVD4 | • GPIO Port E<br>• LCD Video Data Bus | Input: PE0 | LOW if PINMUX: PDOCON or PEOCON = 1 (bits [1:0]); otherwise No Change | 12 mA | I/O | |
| N10 | K9 | PE1/LCDVD5 | | Input: PE1 | | | I/O | |
| M9 | T10 | PE2/LCDVD6 | | Input: PE2 | | | I/O | |
| M10 | R10 | PE3/LCDVD7 | | Input: PE3 | | | I/O | |
| A6 | A5 | PF0/INT0 | • GPIO Port F<br>• External FIQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. | Input: PF0 | No Change | 8 mA | I/O | 3 |
| B6 | B4 | PF1/INT1 | • GPIO Port F<br>• External IRQ Interrupts. Interrupts can be level or edge triggered and are internally debounced. | Input: PF1 | No Change | 8 mA | I/O | 3 |
| C6 | E7 | PF2/INT2 | | Input: PF2 | No Change | 8 mA | I/O | 3 |
| H8 | B3 | PF3/INT3 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. | Input: PF3 | No Change | 8 mA | I/O | 3 |
| B5 | C5 | PF4/INT4/ SCVCCEN | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Smart Card Supply Voltage Enable | Input: PF4 | LOW if SCI is Enabled; otherwise No Change | 8 mA | I/O | 3 |
| D6 | D6 | PF5/INT5/ SCDETECT | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Smart Card Detection | Input: PF5 | No Change | 8 mA | I/O | 3 |
| E6 | A4 | PF6/INT6/ PCRDY1 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Ready for Card 1 for PC Card (PCMCIA or CF) in single or dual card mode | Input: PF6 | No Change | 8 mA | I/O | 3 |
| C5 | A3 | PF7/INT7/ PCRDY2 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Ready for Card 2 for PC Card (PCMCIA or CF) in single or dual card mode | Input: PF7 | No Change | 8 mA | I/O | 3 |
| R3 | M6 | PG0/nPCOE | • GPIO Port G<br>• Output Enable for PC Card (PCMCIA or CF) in single or dual card mode | LOW: PG0 | No Change | 8 mA | I/O | |
| T3 | T1 | PG1/nPCWE | • GPIO Port G<br>• Write Enable for PC Card (PCMCIA or CF) in single or dual card mode | LOW: PG1 | No Change | 8 mA | I/O | |

**Table 3. Functional Pin List (Cont'd)**

| BGA PIN | LFBGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE | I/O | NOTES |
|---|---|---|---|---|---|---|---|---|
| F6 | G2 | COL0 | Keyboard Interface | HIGH | HIGH | 8 mA | O | |
| F5 | G1 | COL1 | | | | | | |
| G1 | H3 | COL2 | | | | | | |
| G2 | H5 | COL3 | | | | | | |
| G4 | H6 | COL4 | | | | | | |
| G5 | H7 | COL5 | | | | | | |
| H1 | H2 | COL6 | | | | | | |
| H2 | H1 | COL7 | | | | | | |
| H3 | J1 | TBUZ | Timer Buzzer (254 kHz MAX.) | LOW | LOW | 8 mA | O | |
| C3 | F5 | MEDCHG | Boot Device Media Change. Used with WIDTH0 and WIDTH1 to specify boot memory device. | Input | No Change | | I | 3 |
| P11 | T14 | WIDTH0 | External Memory Width Pins. Also, used with MEDCHG to specify the boot memory device size. The pins must be pulled HIGH with a 33 kΩ resistor. | Input | No Change | | I | 3 |
| R12 | T15 | WIDTH1 | | | | | | |
| D1 | E3 | BATOK | Battery OK | Input | No Change | | I | 3 |
| D2 | F6 | nBATCHG | Battery Change | Input | No Change | | I | 3 |
| A1 | E5 | TDI | JTAG Data In. This signal is internally pulled-up t o VDD. | Input | No Change | | I | 4 |
| B1 | C2 | TCK | JTAG Clock. This signal should be externally pulled-up to VDD with a 33 kΩ resistor. | Input | No Change | | I | 3 |
| B2 | D3 | TDO | JTAG Data Out. This signal should be externally pulled up to VDD with a 33 kΩ resistor. | High-Z | No Change | 4 mA | O | |
| C1 | C1 | TMS | JTAG Test Mode select. This signal is internally pulled-up to VDD. | Input | No Change | | I | 4 |
| T12 | P15 | nTEST0 | Test Pin 0. Internally pulled up to VDD. For Normal mode, leave open. For JTAG mode, tie to GND. See Table 4. | Input | No Change | | I | 4 |
| R15 | P13 | nTEST1 | Test Pin 1. internally pulled up to VDD. For Normal and JTAG mode, leave open. See Table 4. | | | | | |

1. Signals beginning with 'n' are Active LOW.
2. The SCLK pin can source up to 12 mA and sink up to 20 mA. See 'DC Characteristics'.
3. Schmitt trigger input; see 'DC Specifications', page 31 for triggers points and hysteresis.
4. Input only for JTAG boundary scan mode.
5. Output only for JTAG boundary scan mode.
6. The internal pullup and pull-down resistance on all digital I/O pins is 50 kΩ
7. When used as SMBCLK, this pin must have a resistor.
8. The RESET STATE is defined as the state during power-on reset.
9. The STANDBY STATE is defined as the state when the device is in standby. During this state, I/O cells are forced to input (Input), output driving low (LOW), output driving high (HIGH), or their current state is preserved (No Change). In some case, function selection has an overall effect on the standby state.
10. All unused USB Device pins with a differential pair must be pulled to ground with a 15 kΩ resistor.

**Table 4. nTest Pin Function**

| MODE | nTEST0 | nTEST1 | nURESET |
|---|---|---|---|
| JTAG | 0 | 1 | 1 |
| Normal | 1 | 1 | x |

**Table 7. 256-Ball LFBGA Package Numerical Pin List**

| LFBGA PIN | SIGNAL |
|---|---|
| F10 | VDDC |
| F11 | VDD |
| F12 | D19 |
| F13 | A17/SB1 |
| F14 | VDD |
| F15 | D16 |
| F16 | A15/SA13 |
| G1 | COL1 |
| G2 | COL0 |
| G3 | UARTRX2 |
| G4 | UARTDSR2 |
| G5 | UARTIRTX1 |
| G6 | UARTIRRX1 |
| G7 | VSSC |
| G8 | VDD |
| G9 | D13 |
| G10 | A13/SA11 |
| G11 | A14/SA12 |
| G12 | D15 |
| G13 | VSS |
| G14 | D14 |
| G15 | A12/SA10 |
| G16 | D12 |
| H1 | COL7 |
| H2 | COL6 |
| H3 | COL2 |
| H4 | VSSC |
| H5 | COL3 |
| H6 | COL4 |
| H7 | COL5 |
| H8 | VSSC |
| H9 | VSS |
| H10 | A10/SA8 |
| H11 | D11 |
| H12 | A11/SA9 |
| H13 | VDD |
| H14 | D10 |
| H15 | A9/SA7 |
| H16 | D9 |
| J1 | TBUZ |
| J2 | SSPFRM/nSSPFRM |
| J3 | SSPCLK |
| J4 | VDDC |
| J5 | PGMCLK |

**Table 7. 256-Ball LFBGA Package Numerical Pin List**

| LFBGA PIN | SIGNAL |
|---|---|
| J6 | SSPRX |
| J7 | SSPTX |
| J8 | VDDC |
| J9 | VDD |
| J10 | D8 |
| J11 | A7/SA5 |
| J12 | D7 |
| J13 | A6/SA4 |
| J14 | VSS |
| J15 | D6 |
| J16 | A8/SA6 |
| K1 | PA0/LCDVD16 |
| K2 | PA1/LCDVD17 |
| K3 | PA2 |
| K4 | PA3 |
| K5 | PA5 |
| K6 | PA4 |
| K7 | VSS |
| K8 | VDDC |
| K9 | PE1/LCDVD5 |
| K10 | PD1/LCDVD9 |
| K11 | D3 |
| K12 | A3/SA1 |
| K13 | A4/SA2 |
| K14 | D5 |
| K15 | VDD |
| K16 | A5/SA3 |
| L1 | PA6 |
| L2 | PA7 |
| L3 | PB0/UARTRX1 |
| L4 | VSSC |
| L5 | PB4/UARTDCD3 |
| L6 | VDDC |
| L7 | VDD |
| L8 | VSS |
| L9 | VSSC |
| L10 | VSS |
| L11 | D0 |
| L12 | VSS |
| L13 | D1 |
| L14 | D2 |
| L15 | A2/SA0 |
| L16 | D4 |
| M1 | PB1/UARTTX3 |

### AMBA APB BUS

The AMBA APB bus is a lower-speed 32-bit-wide peripheral data bus. The speed of this bus is selectable to be a divide-by-2, divide-by-4 or divide-by-8 of the speed of the AHB bus.

### EXTERNAL BUS INTERFACE

The External Bus Interface (EBI) provides a 32-bit wide, high speed gateway to external memory devices. The memory devices supported include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous memory controller or Synchronous memory controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

### LCD AHB BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

### DMA BUSES

The LH7A400 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core. The DMA engine does not support memory to memory transfers.

## Memory Map

The LH7A400 system has a 32-bit-wide address bus. This allows it to address up to 4GB of memory. This memory space is subdivided into a number of memory banks; see Figure 6. Four of these banks (each of 256MB) are allocated to the Synchronous memory controller. Eight of the banks (again, each 256MB) are allocated to the Asynchronous memory controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest is unused.

The LH7A400 can boot from either synchronous or asynchronous ROM/Flash. The selection is determined by the value of the MEDCHG pin at Power On Reset as shown in Table 8. When booting from synchronous memory, then synchronous bank 4 (nSCS3) is mapped into memory location zero. When booting from asynchronous memory, asynchronous memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 6 shows the memory map of the LH7A400 system for the two boot modes.

Once the LH7A400 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

**Table 8. Boot Modes**

| BOOT MODE | LATCHED BOOT-WIDTH1 | LATCHED BOOT-WIDTH0 | LATCHED MEDCHG |
|---|---|---|---|
| 8-bit ROM | 0 | 0 | 0 |
| 16-bit ROM | 0 | 1 | 0 |
| 32-bit ROM | 1 | 0 | 0 |
| 32-bit ROM | 1 | 1 | 0 |
| 16-bit SFlash (Initializes Mode Register) | 0 | 0 | 1 |
| 16-bit SROM (Initializes Mode Register) | 0 | 1 | 1 |
| 32-bit SFlash (Initializes Mode Register) | 1 | 0 | 1 |
| 32-bit SROM (Initializes Mode Register) | 1 | 1 | 1 |

## Interrupt Controller

The LH7A400 interrupt controller is designed to control the interrupts from 28 different sources. Four interrupt sources are mapped to the FIQ input of the ARM922T and 24 are mapped to the IRQ input. FIQs have a higher priority than the IRQs. If two interrupts with the same priority become active at the same time, the priority must be resolved in software.

When an interrupt becomes active, the interrupt controller generates an FIQ or IRQ if the corresponding mask bit is set. No latching of interrupts takes place in the controller. After a Power On Reset all mask register bits are cleared, therefore masking all interrupts. Hence, enabling of the mask register must be done by software after a power-on-reset.

The Asynchronous Memory Controller has six main functions:

- Memory bank select
- Access sequencing
- Wait states generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

## Synchronous Memory Controller

The Synchronous memory controller provides a high speed memory interface to a wide variety of Synchronous memory devices, including SDRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks that can be independently set up
- Special configuration bits for Synchronous ROM operation
- Ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the SDRAM in quad-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains are provided to enable SDRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

## MultiMediaCard (MMC)

The MMC adapter combines all of the requirements and functions of an MMC host. The adapter supports the full MMC bus protocol, defined by the MMC Definition Group’s specification v.2.11. The controller can also implement the SPI interface to the cards.

### INTERFACE DESCRIPTION AND MMC OVERVIEW

The MMC controller uses the three-wire serial data bus (clock, command, and data) to transfer data to and from the MMC card, and to configure and acquire status information from the card’s registers.

MMC bus lines can be divided into three groups:

- Power supply: VDD and VSS
- Data Transfer: MMCCMD, MMCDATA
- Clock: MMCLK.

### MULTIMEDIACARD ADAPTER

The MultiMediaCard Adapter implements MultiMediaCard specific functions, serves as the bus master for the MultiMediacard Bus and implements the standard interface to the MultiMediaCard Cards (card initialization, CRC generation and validation, command/response transactions, etc.).

## Smart Card Interface (SCI)

The SCI (ISO7816) interfaces to an external Smart Card reader. The SCI can autonomously control data transfer to and from the smart card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

### SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors D = 1, 2, or 4 supported
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous Smart Cards via registered input/output.

### PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Check for maximum time for first character of Answer to Reset - ATR reception
- Check for maximum duration of ATR character stream
- Check for maximum time of receipt of first character of data stream
- Check for maximum time allowed between characters
- Character guard time
- Block guard time
- Transmit/receive character retry.

## Audio Codec Interface (ACI)

The ACI provides:

- A digital serial interface to an off-chip 8-bit CODEC
- All the necessary clocks and timing pulses to perform serialization or de-serialization of the data stream to or from the CODEC device.

The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The ACI includes a programmable frequency divider that generates a common transmit and receive bit clock output from the on-chip ACI clock input (ACICLK). Transmit data values are output synchronous with the rising edge of the bit clock output. Receive data values are sampled on the falling edge of the bit clock output. The start of a data frame is indicated by a synchronization output signal that is synchronous with the bit clock.

## Synchronous Serial Port (SSP)

The LH7A400 SSP is a master-only interface for synchronous serial communication with device peripheral devices that has either Motorola SPI, National Semiconductor MICROWIRE or Texas Instruments Synchronous Serial Interfaces.

The LH7A400 SSP performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on SSPTXD and received on SSPRXD.

The LH7A400 SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLK from the input clock SSPCLK. Bit rates are supported to 2 MHz and beyond, subject to choice of frequency for SSPCLK; the maximum bit rate will usually be determined by peripheral devices.

## UART/IrDA

The LH7A400 contains three UARTs, UART1, UART2, and UART3.

The UART performs:

- Serial-to-Parallel conversion on data received from the peripheral device
- Parallel-to-Serial conversion on data transmitted to the peripheral device.

The transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The UART can generate:

- Four individually maskable interrupts from the receive, transmit and modem status logic blocks
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted and unmasked.

If a framing, parity, or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and the FIFO data is prevented from being overwritten. UART1 also supports IrDA 1.0 (15.2 kbit/s).

The modem status input signals Clear to Send (CTS), Data Carrier Detect (DCD) and Data Set Ready (DSR) are supported on UART2 and UART3.

## Timers

Two identical timers are integrated in the LH7A400. Each of these timers has an associated 16-bit read/write data register and a control register. Each timer is loaded with the value written to the data register immediately, this value will then be decremented on the next active clock edge to arrive after the write. When the timer underflows, it will immediately assert its appropriate interrupt. The timers can be read at any time. The clock source and mode is selectable by writing to various bits in the system control register. Clock sources are 508 kHz and 2 kHz.

Timer 3 (TC3) has the same basic operation, but is clocked from a single 7.3728 MHz source. It has the same register arrangement as Timer 1 and Timer 2, providing a load, value, control and clear register. Once the timer has been enabled and is written to, unlike the Timer 1 and Timer 2, will decrement the timer on the next rising edge of the 7.3728 MHz clock after the data register has been updated. All the timers can operate in two modes, free running mode or pre-scale mode.

### FREE-RUNNING MODE

In free-running mode, the timer will wrap around to 0xFFFF when it underflows and continue counting down.

### PRE-SCALE MODE

In pre-scale (periodic) mode, the value written to each timer is automatically re-loaded when the timer underflows. This mode can be used to produce a programmable frequency to drive an external buzzer or generate a periodic interrupt.

# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

| PARAMETER | MINIMUM | MAXIMUM |
|---|---|---|
| DC Core Supply Voltage (VDDC) | –0.3 V | 2.4 V |
| DC I/O Supply Voltage (VDD) | –0.3 V | 4.6 V |
| DC Analog Supply Voltage (VDDA) | –0.3 V | 2.4 V |
| 5 V Tolerant Digital Input Pin Voltage | –0.5 V | 5.5 V |
| ESD, Human Body Model (Analog pins AN0 - AN9 rated at 500 V) | | 2 kV |
| ESD, Charged Device Model | | 1 kV |
| Storage Temperature | –55°C | 125°C |

**NOTE:** Except for Storage Temperature, these ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

## Recommended Operating Conditions

| PARAMETER | MINIMUM | TYPICAL | MAXIMUM | NOTES |
|---|---|---|---|---|
| DC Core Supply Voltage (VDDC) | 1.71 V | 1.8 V | 1.89 V | 1, 4 |
| DC Core Supply Voltage (VDDC) | 2.0 V | 2.1 V | 2.2 V | 1, 5 |
| DC I/O Supply Voltage (VDD) | 3.0 V | 3.3 V | 3.6 V | 2, 6 |
| DC I/O Supply Voltage (VDD) | 3.14 V | 3.3 V | 3.6 V | 2, 7 |
| DC Analog Supply Voltage for PLLs (VDDA) | 1.71 V | 1.8 V | 1.89 V | |
| Clock Frequency (0°C to +70°C) | 10 MHz | | 200 MHz | 3, 4, 6 |
| Clock Frequency (–40°C to +85°C) | 10 MHz | | 195 MHz | 3, 4, 6 |
| Bus Clock Frequency (–40°C to +85°C) | | | 100 MHz | 3, 4, 6 |
| Clock Frequency (0°C to +70°C) | 10 MHz | | 250 MHz | 3, 5, 7 |
| Clock Frequency (–40°C to +85°C) | 10 MHz | | 245 MHz | 3, 5, 7 |
| Bus Clock Frequency (–40°C to +85°C) | | | 125 MHz | 3, 5, 7 |
| External Clock Input (XTALIN) | 14 MHz | 14.7456 MHz | 20 MHz | 8 |
| External Clock Input (XTALIN) Voltage | 1.71 V | 1.8 V | 1.89 V | |
| Operating Temperature | –40°C | 25°C | +85°C | |

**NOTES:**
1. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 33
2. USB is not functional below 3.0 V
3. Using 14.7456 MHz Main Oscillator Crystal and 32.768 kHz RTC Oscillator Crystal
4. VDDC = 1.71 V to 1.89 V (LH7A400N0G000xx)
5. VDDC = 2.1 V ± 5 % (LH7A400N0G076xx only)
6. VDD = 3.0 V to 3.6 V (LH7A400N0G000xx)
7. VDD = 3.14V to 3.60 V (LH7A400N0G076xx only)
8. IMPORTANT: Most peripherals will NOT function with crystals other than 14.7456 MHz.

## DC/AC SPECIFICATIONS

Unless otherwise noted, all data provided in these specifications are based on –40°C to +85°C, VDDC = 1.71 V to 1.89 V, VDD = 3.0 V to 3.6 V, VDDA = 1.71 V to 1.89 V.

### DC Specifications

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | CONDITIONS | NOTES |
|---|---|---|---|---|---|---|---|
| VIH | CMOS and Schmitt Trigger Input HIGH Voltage | 2.0 | | 5.5 | V | | |
| VIL | CMOS and Schmitt Trigger Input LOW Voltage | –0.2 | | 0.8 | V | | |
| VHST | Schmitt Trigger Hysteresis | 0.25 | | | V | VIL to VIH | |
| VOH | Output Drive 2 | 2.6 | | | V | IOH = –4 mA | |
| | Output Drive 3 | 2.6 | | | V | IOH = –8 mA | |
| | Output Drive 4 and 5 | 2.6 | | | V | IOH = –12 mA | 1 |
| VOL | Output Drive 2 | | | 0.4 | V | IOL = 4 mA | |
| | Output Drive 3 | | | 0.4 | V | IOL = 8 mA | |
| | Output Drive 4 | | | 0.4 | V | IOL = 12 mA | |
| | Output Drive 5 | | | 0.4 | V | IOL = 20 mA | 1 |
| IIN | Input Leakage Current | –10 | | 10 | µA | VIN = VDD or GND | |
| | Input Leakage Current (with pull-up resistors installed) | –200 | | –20 | µA | VIN = VDD or GND | |
| IOZ | Output Tri-state Leakage Current | –10 | | 10 | µA | VOUT = VDD or GND | |
| ISTARTUP | Startup Current | | | 50 | µA | | 2 |
| IACTIVE | Active Current | | 125 | 180 | mA | | |
| IHALT | Halt Current | | 25 | 41 | mA | | |
| ISTANDBY | Standby Current | | 42 | | µA | | |
| CIN | Input Capacitance | | | 4 | pF | | |
| COUT | Output Capacitance | | | 4 | pF | | |

**NOTES:**
1. Output Drive 5 can sink 20 mA of current, but sources 12 mA of current.
2. Current consumption until oscillators are stabilized.

### AC Test Conditions

| PARAMETER | RATING | UNIT |
|---|---|---|
| DC I/O Supply Voltage (VDD) | 3.0 to 3.6 | V |
| DC Core Supply Voltage (VDDC) | 1.71 to 1.89 | V |
| Input Pulse Levels | VSS to 3 | V |
| Input Rise and Fall Times | 2 | ns |
| Input and Output Timing Reference Levels | VDD/2 | V |

## CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 10 were derived under the conditions presented here.

### Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All voltages at maximum specified values
- Maximum specified ambient temperature (tAMB).

### Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- LINUX operating system running from SDRAM
- UART and AC97 peripherals operating; all other peripherals as needed by the OS
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate, data in SDRAM
- I/O loads at nominal
- Cache enabled
- FCLK = 200 MHz or 250 MHz; HCLK = 100 MHz or 125 MHz; PCLK = 50 MHz or 62.5 MHz
- All voltages at typical values
- Nominal case temperature (tAMB).

**Table 10. Current Consumption by Mode**

| SYMBOL | PARAMETER | LH7A400N0G000xx (FCLK = 200 MHz) | | LH7A400N0G076xx (FCLK = 250 MHz) | |
|---|---|---|---|---|---|
| | | TYP. | MAX. | TYP. | UNITS |
| **ACTIVE MODE** | | | | | |
| ICORE | Core Current | 110 | 135 | 250 | mA |
| IIO | I/ O Current | 15 | 45 | | mA |
| **HALT MODE (ALL PERIPHERALS DISABLED)** | | | | | |
| ICORE | Core Current | 24 | 39 | 50 | mA |
| IIO | I/ O Current | 1 | 2 | | mA |
| **STANDBY MODE (TYPICAL CONDITIONS ONLY)** | | | | | |
| ICORE | Core Current | 40 | | 125 | μA |
| IIO | I/ O Current | 2 | | 4 | μA |

## PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 11 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the CPU clock running at 200 MHz, typical conditions, and no I/O loads. This current is supplied by the 1.8 VDDC power supply.

**Table 11. Peripheral Current Consumption**

| PERIPHERAL | TYPICAL | UNITS |
|---|---|---|
| AC97 | 1.3 | mA |
| UART (Each) | 1.0 | mA |
| RTC | 0.005 | mA |
| Timers (Each) | 0.1 | mA |
| LCD (+I/O) | 5.4 (1.0) | mA |
| MMC | 0.6 | mA |
| SCI | 23 | mA |
| PWM (each) | < 0.1 | mA |
| BMI-SWI | 1.0 | mA |
| BMI-SBus | 1.0 | mA |
| SDRAM (+I/O) | 1.5 (14.8) | mA |
| USB (+PLL) | 5.6 (3.3) | mA |
| ACI | 0.8 | mA |

## Power Supply Sequencing

NXP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 μs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

## AC Specifications

All signals described in Table 12 relate to transitions after a reference clock signal. The illustration in Figure 9 represents all cases of these sets of measurement parameters.

The reference clock signals in this design are:

- HCLK, internal System Bus clock ('C' in timing data)
- PCLK, Peripheral Bus clock
- SSPCLK, Synchronous Serial Port clock
- UARTCLK, UART Interface clock
- LCDDCLK, LCD Data clock from the LCD Controller
- ACBITCLK, AC97 clock
- SCLK, Synchronous Memory clock.

All signal transitions are measured at the 50 % point.

For outputs from the LH7A400, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from a valid address bus, or rising edge of the peripheral clock. Maximum requirements for tOVXXX are shown in Table 12.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output will be held valid from the valid address bus, or rising edge of the peripheral clock. Minimum requirements for tOHXXX are listed in Table 12.

For Inputs, tISXXX (e.g. tISD) represents the amount of time the input signal must be valid before a valid address bus, or rising edge of the peripheral clock (except SSP and ACI). Maximum requirements for tISXXX are shown in Table 12.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid from the valid address bus, or rising edge of the peripheral clock (except SSP and ACI). Minimum requirements are shown in Table 12.

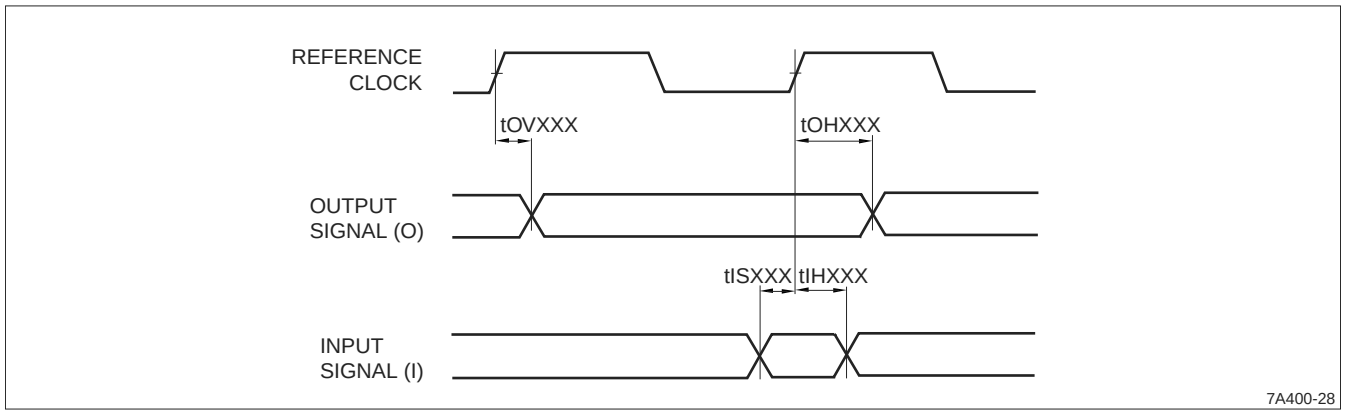



**Figure 9. LH7A400 Signal Timing**

**Table 12. AC Signal Characteristics**

| SIGNAL | TYPE | LOAD | SYMBOL | MIN. | MAX. | DESCRIPTION |
|---|---|---|---|---|---|---|
| **ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ [wait states × HCLK period])[1]** | | | | | | |
| A[27:0] | Output | 50 pF | tRC | 4 × tHCLK – 7.0 ns | 4 × tHCLK + 7.5 ns | Read Cycle Time |
| | Output | 50 pF | tWC | 4 × tHCLK – 7.0 ns | 4 × tHCLK + 7.5 ns | Write Cycle Time |
| | — | — | tWS | tHCLK ns | tHCLK ns | Wait State Width |
| D[31:0] | Output | 50 pF | tDVWE | tHCLK – 6.0 ns | tHCLK – 2.0 ns | Data Valid to Write Edge (nWE invalid) |
| | | | tDHWE | tHCLK – 7.0 ns | tHCLK + 2.0 ns | Data Hold after Write Edge (nWE invalid) |
| | | | tDVBE | tHCLK – 5.0 ns | tHCLK – 1.0 ns | Data Valid to nBLE Invalid |
| | | | tDHBE | tHCLK – 7.0 ns | tHCLK + 3.0 ns | Data Hold after nBLE Invalid |
| | Input | — | tDSCS | 15 ns | — | Data Setup to nCSx Invalid |
| | | | tDHCS | 0 ns | — | Data Hold to nCSx Invalid |
| | | | tDSOE | 15 ns | — | Data Setup to nOE Invalid |
| | | | tDHOE | 0 ns | — | Data Hold to nOE Invalid |
| | | | tDSBE | 15 ns | — | Data Setup to nBLE Invalid |
| | | | tDHBE | 0 ns | — | Data Hold to nBLE Invalid |
| nCS[7:0] | Output | 30 pF | tCS | 2 × tHCLK – 3.0 ns | 2 × tHCLK + 3.0 ns | nCSx Width |
| | | | tAVCS | tHCLK – 4.0 ns | tHCLK | Address Valid to nCSx Valid |
| | | | tAHCS | tHCLK | tHCLK + 4.5 ns | Address Hold after nCSx Invalid |
| **SYNCHRONOUS MEMORY INTERFACE SIGNALS** | | | | | | |
| SA[13:0] | Output | 50 pF | tOVA | | $5.5^3/7.5^4$ ns | Address Valid |
| | | | tOHA | $1.5^3/1.5^4$ ns | | Address Hold |
| SA[17:16]/SB[1:0] | Output | 50 pF | tOVB | | $5.5^3/7.5^4$ ns | Bank Select Valid |
| D[31:0] | Output | 50 pF | tOHD | 1.5ns | | Data Hold |
| | | | tOVD | 2 ns | $5.5^3/7.5^4$ ns | Data Valid |
| | Input | | tISD | $1.5^3/2.5^4$ ns | | Data Setup |
| | | | tIHD | $1.0^3/1.5^4$ ns | | Data Hold |
| nCAS | Output | 30 pF | tOVCA | 2 ns | $5.5^3/7.5^4$ ns | CAS Valid |
| | | | tOHCA | $1.5^3/2^4$ ns | | CAS Hold |
| nRAS | Output | 30 pF | tOVRA | 2 ns | $5.5^3/7.5^4$ ns | RAS Valid |
| | | | tOHRA | $1.5^3/2^4$ ns | | RAS Hold |
| nSWE | Output | 30 pF | tOVSDW | 2 ns | $5.5^3/7.5^4$ ns | Write Enable Valid |
| | | | tOHSDW | $1.5^3/2^4$ ns | | Write Enable Hold |
| SCKE[1:0] | Output | 30 pF | tOVC | 2 ns | $5.5^3/7.5^4$ ns | Clock Enable Valid |
| DQM[3:0] | Output | 30 pF | tOVDQ | 2 ns | $5.5^3/7.5^4$ ns | Data Mask Valid |
| nSCS[3:0] | Output | 30 pF | tOVSC | 2 ns | $5.5^3/7.5^4$ ns | Synchronous Chip Select Valid |
| | | | tOHSC | $1.5^3/2^4$ ns | | Synchronous Chip Select Hold |
| **PCMCIA INTERFACE SIGNALS (+ wait states × HCLK period)** | | | | | | |
| nPCREG | Output | 30 pF | tOVDREG | | tHCLK | nREG Valid |
| | | | tOHDREG | 4 × tHCLK – 5 ns | | nREG Hold |
| D[31:0] | Output | 50 pF | tOVD | | tHCLK | Data Valid |
| | | | tOHD | 4 × tHCLK – 5 ns | | Data Hold |
| | Input | | tISD | | tHCLK - 10 ns | Data Setup Time |
| | | | tIHD | 4 × tHCLK – 5 ns | | Data Hold Time |
| nPCCE1 | Output | 30 pF | tOVCE1 | | tHCLK | Chip Enable 1 Valid |
| | | | tOHCE1 | 4 × tHCLK – 5 ns | | Chip Enable 1 Hold |
| nPCCE2 | Output | 30 pF | tOVCE2 | | tHCLK | Chip Enable 2 Valid |
| | | | tOHCE2 | 4 × tHCLK – 5 ns | | Chip Enable 2 Hold |
| nPCOE | Output | 30 pF | tOVOE | | tHCLK + 1 ns | Output Enable Valid |
| | | | tOHOE | 3 × tHCLK – 5 ns | | Output Enable Hold |
| nPCWE | Output | 30 pF | tOVWE | | tHCLK + 1 ns | Write Enable Valid |
| | | | tOHWE | 3 × tHCLK – 5 ns | | Write Enable Hold |
| PCDIR | Output | 30 pF | tOVPCD | | tHCLK | Card Direction Valid |
| | | | tOHPCD | 4 × tHCLK – 5 ns | | Card Direction Hold |

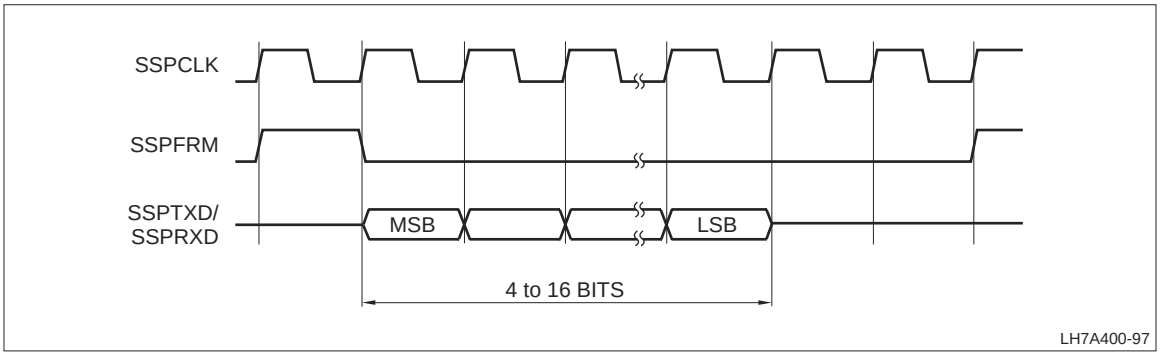



**Figure 16. Texas Instruments Synchronous Serial Frame Format (Single Transfer)**

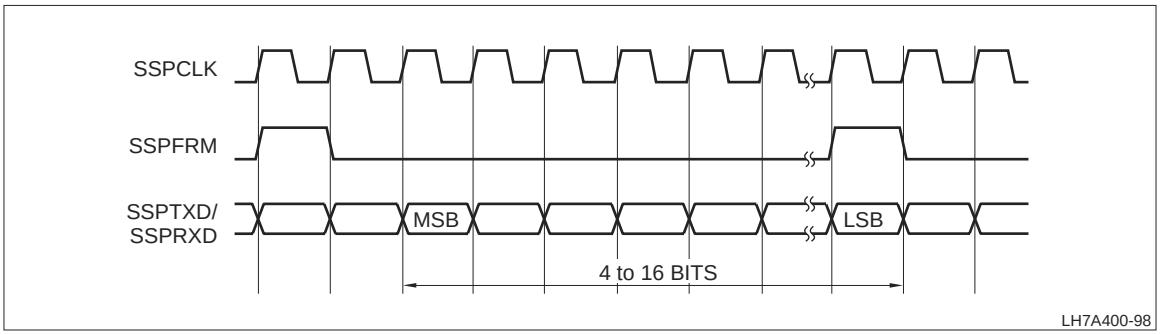



**Figure 17. Texas Instruments Synchronous Serial Frame Format (Continuous Transfer)**

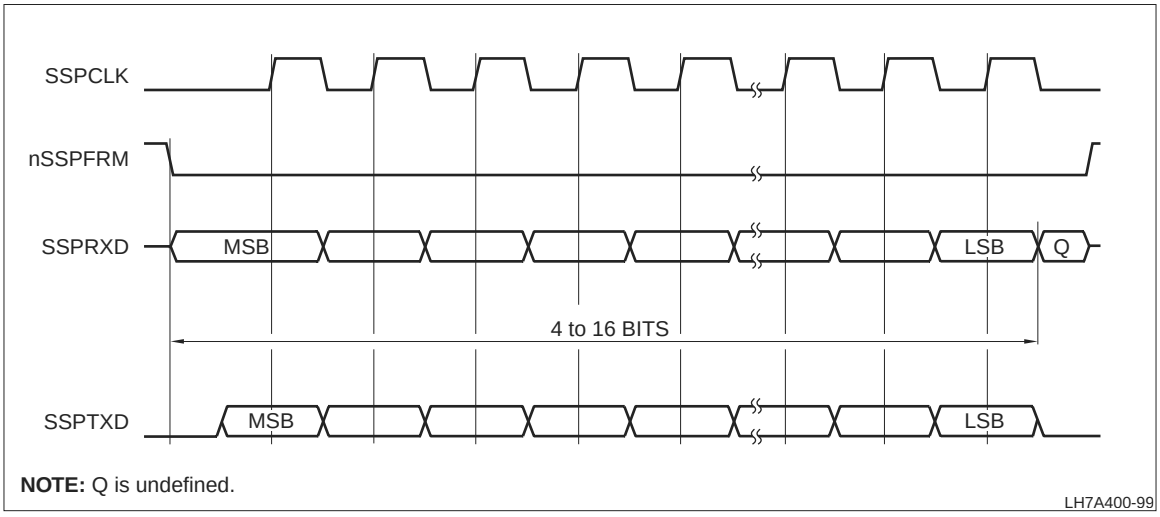
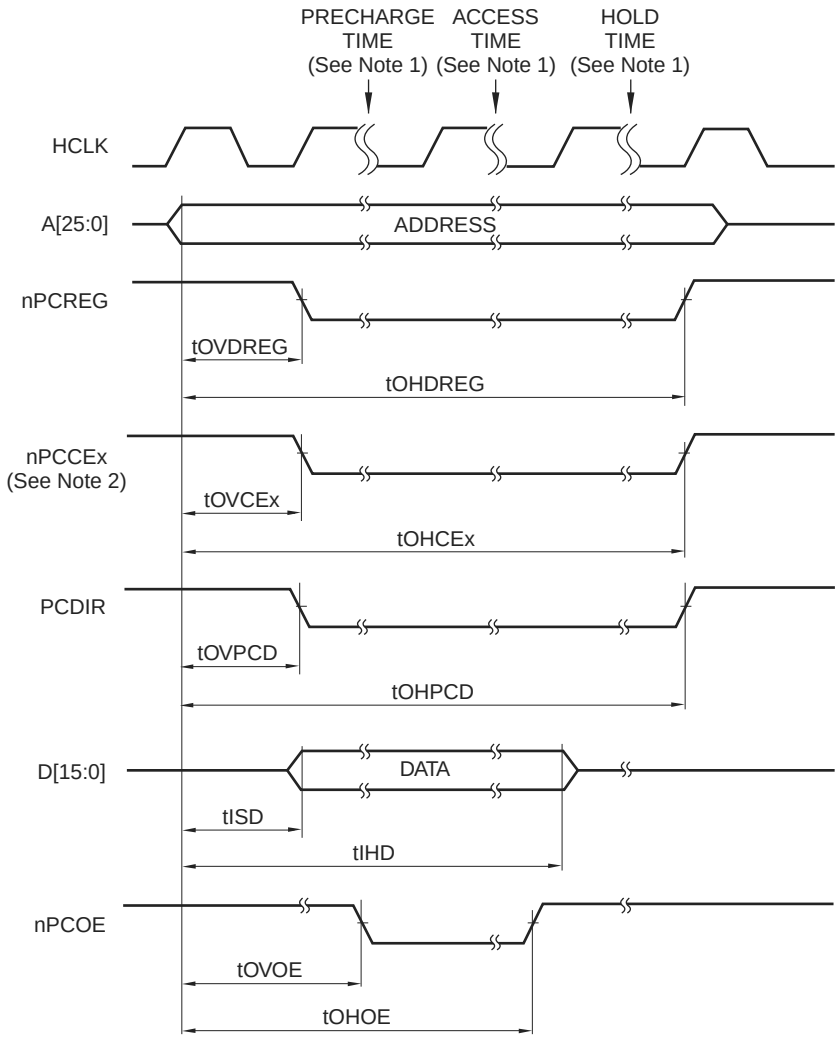



**Figure 18. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 0**

## PC Card (PCMCIA) Waveforms

Figure 28 shows the waveforms and timing for a PCMCIA Read Transfer, Figure 29 shows the waveforms and timing for a PCMCIA Write Transfer.




**NOTES:**

1. Precharge time, access time, and hold time are programmable wait-state times.
2. 

| nPCCE1 | nPCCE2 | TRANSFER TYPE |
|---|---|---|
| 0 | 0 | Common Memory |
| 0 | 1 | Attribute Memory |
| 1 | 0 | I/O |
| 1 | 1 | None |

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**Figure 28. PCMCIA Read Transfer**

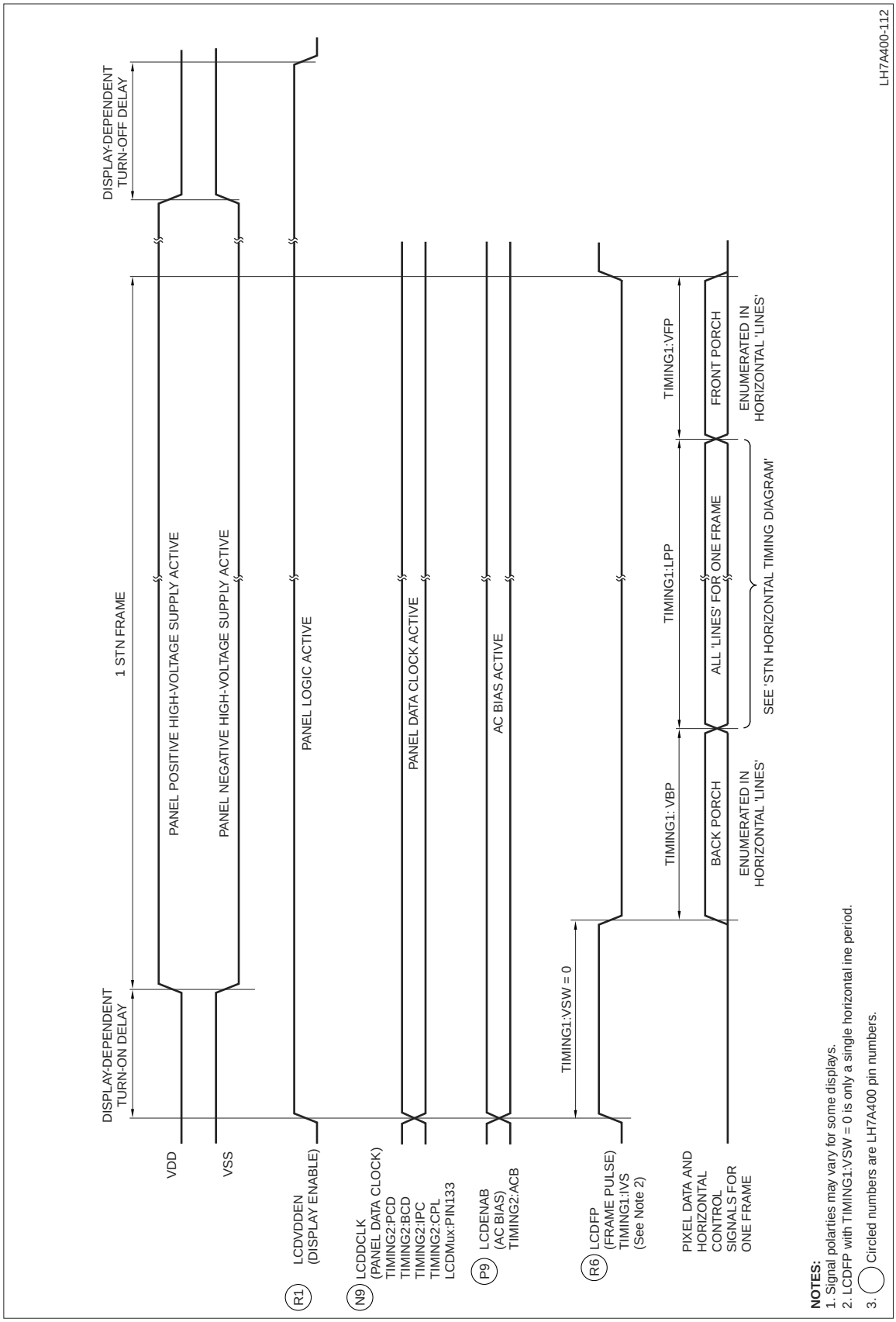
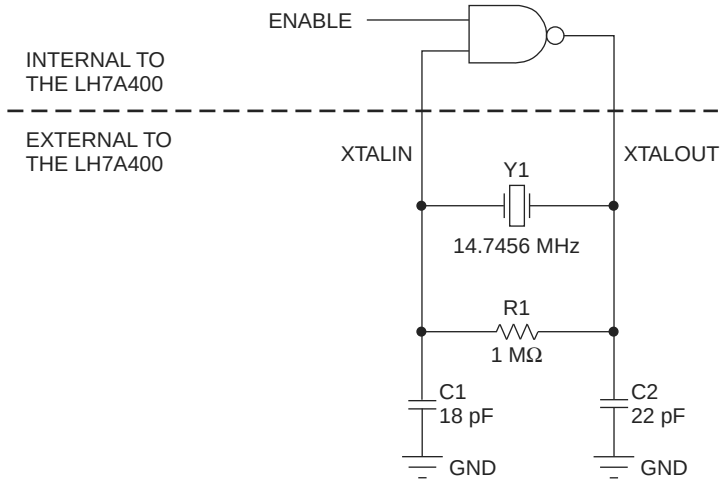



**Figure 37. STN Vertical Timing Diagram**




**NOTES:**
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

**RECOMMENDED CRYSTAL SPECIFICATIONS**

| PARAMETER | DESCRIPTION |
|---|---|
| 14.7456 MHz Crystal | (AT-Cut) Parallel Mode |
| Tolerance | ±50 ppm |
| Stability | ±100 ppm |
| Aging | ±5 ppm |
| Load Capacitance | 18 pF |
| ESR (MAX.) | 40 Ω |
| Drive Level | 100 µW (MAX.) |
| Recommended Part | MTRON SX2050 or equivalent |

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**Figure 46. 14.7456 MHz External Oscillator Components and Schematic**

## Operating Temperature and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

NXP recommends that users implementing a system to meet industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (i.e., noise immunity of the clock input to the SoC).

## Printed Circuit Board Layout Practices

### LH7A400 POWER SUPPLY DECOUPLING

The LH7A400 has separate power and ground pins for different internal circuitry sections. The VDD and VSS pins supply power to I/O buffers, while VDDC and VSSC supply power to the core logic, and VDDA/VSSA supply analog power to the PLLs.

Each of the VDD and VDDC pins must be provided with a low impedance path to the corresponding board power supply. Likewise, the VSS, VSSA, and VSSC pins must be provided with a low impedance path to the board ground.

Each power supply must be decoupled to ground using at least one 0.1 μF high frequency capacitor located as close as possible to a VDDx, VSSx pin pair on each of the four sides of the chip. If room on the circuit board allows, add one 0.01 μF high frequency capacitor near each VDDx, VSSx pair on the chip.

To be effective, the capacitor leads and associated circuit board traces connecting to the chip VDDx, VSSx pins must be kept to less than half an inch (12.7 mm) per capacitor lead. There must be one bulk 10 μF capacitor for each power supply placed near one side of the chip.

### RECOMMENDED PLL, VDDA, VSSA FILTER

The VDDA pins supply power to the chip PLL circuitry. VSSA is the ground return path for the PLL circuit. NXP recommends a low-pass filter attached as shown in Figure 47. The values of the inductor and capacitors are not critical. The low-pass filter prevents high frequency noise from adversely affecting the PLL circuits. The distance from the IC pin to the high frequency capacitor should be as short as possible.

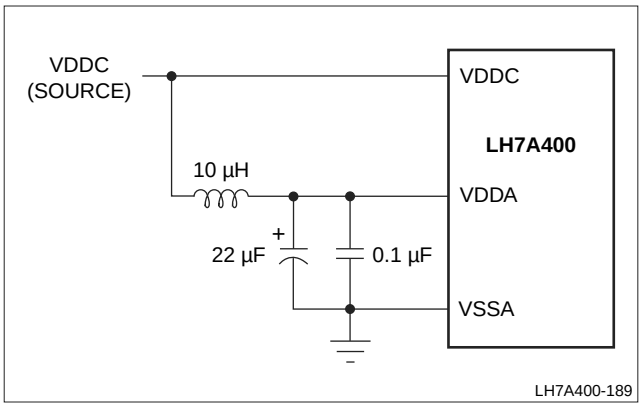


**Figure 47. VDDA, VSSA Filter Circuit**

### UNUSED INPUT SIGNAL CONDITIONING

Floating input signals can cause excessive power consumption. Unused inputs without internal pull-up or pull-down resistors should be pulled up or down externally (NXP recommends tying HIGH), to tie the signal to its inactive state. 33 KΩ or less is recommended.

Some GPIO signals default to inputs. If the pins that carry these signals are unused, software can program these signals as outputs, eliminating the need for pull-ups or pull-downs. Power consumption may be higher than expected until software completes programming the GPIO. Some LH7A400 inputs have internal pull-ups or pull-downs. If unused, these inputs do not require external conditioning.

### OTHER CIRCUIT BOARD LAYOUT PRACTICES

All outputs have fast rise and fall times. Printed circuit trace interconnection length must therefore be reduced to minimize overshoot, undershoot and reflections caused by transmission line effects of these fast output switching times. This recommendation particularly applies to the address and data buses.

When considering capacitance, calculations must consider all device loads and capacitances due to the circuit board traces. Capacitance due to the traces will depend upon a number of factors, including the trace width, dielectric material the circuit board is made from and proximity to ground and power planes.

Attention to power supply decoupling and printed circuit board layout becomes more critical in systems with higher capacitive loads. As these capacitive loads increase, transient currents in the power supply and ground return paths also increase.

## REVISION HISTORY

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LH7A400_N_2 | 20090319 | Product data sheet | - | LH7A400_N_1 |
| Modifications:<br>• Changed document status to “Product data sheet”. | | | | |
| LH7A400_N_1 | 20070716 | Preliminary data sheet | - | FAST LH7A400 v1-5 5-9-07 |