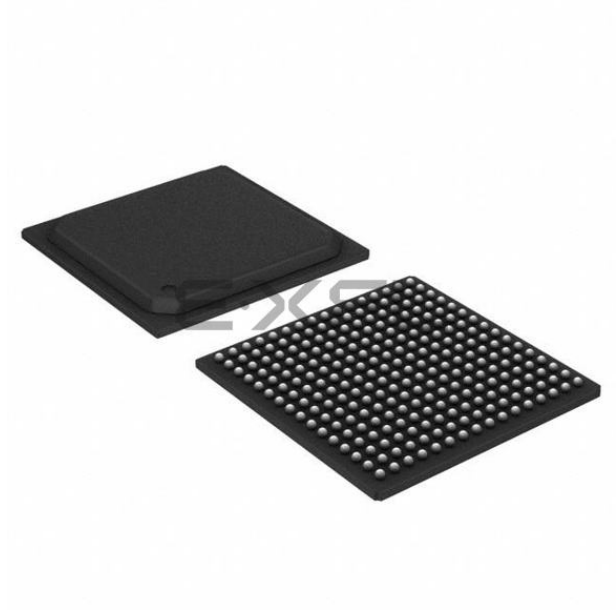

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, IrDA, Microwire, Memory Card, SmartCard, SPI, SSI, SSP, UART/USART, USB
Peripherals	AC'97, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lh7a400n0g000b5-55

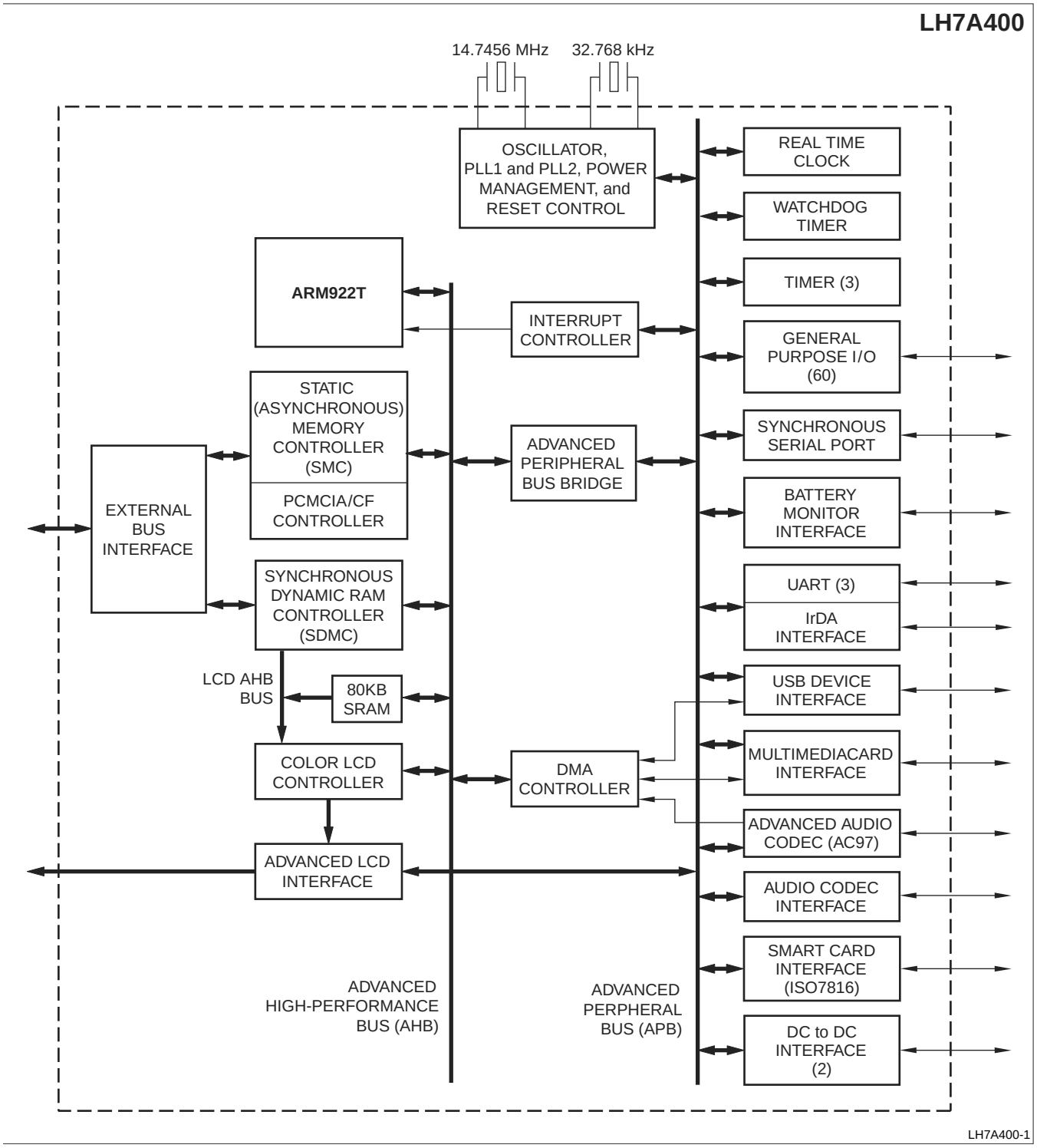


Figure 1. LH7A400 block diagram

Table 3. Functional Pin List

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
G7	C10	VDD	I/O Ring Power					
F1	F9							
K7	F11							
M1	F14							
M5	G8							
T6	H13							
R14	J9							
M14	K15							
J11	L7							
J12	N6							
F13	N8							
B14	N12							
E10	N13							
B8	P11							
H7	B8	VSS	I/O Ring Ground					
G3	C6							
K4	D5							
N5	D13							
P6	E8							
T14	F7							
R16	G13							
N16	H9							
K13	J14							
H9	K7							
C15	L8							
A11	L10							
E8	L12							
A5	M11							
F7	M14							
E1	C4	VDDC	Core Power					
J4	D7							
P3	D10							
T8	F4							
K9	F10							
L13	J4							
E15	J8							
D12	K8							
A7	L6							
H5	G7	VSSC	Core Ground					
M3	H4							
L9	H8							
T10	L4							
N15	L9							
H12	N3							
B15	N7							
C9	N10							
G6	R5							

Table 3. Functional Pin List (Cont'd)

BGA PIN	LFBGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
L6	P4	PG2/ nPCIOR	• GPIO Port G • I/O Read Strobe for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG2	No Change	8 mA	I/O	
M6	R3	PG3/ nPCIOW	• GPIO Port G • I/O Write Strobe for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG3	No Change	8 mA	I/O	
N6	T2	PG4/nPCREG	• GPIO Port G • Register Memory Access for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG4	No Change	8 mA	I/O	
M7	P5	PG5/nPCCE1	• GPIO Port G • Card Enable 1 for PC Card (PCMCIA or CF) in single or dual card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	LOW: PG5	No Change	8 mA	I/O	
M8	R4	PG6/nPCCE2	• GPIO Port G • Card Enable 2 for PC Card (PCMCIA or CF) in single or dual card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	LOW: PG6	No Change	8 mA	I/O	
N4	T3	PG7/PCDIR	• GPIO Port G • Direction for PC Card (PCMCIA or CF) in single or dual card mode	LOW: PG7	No Change	8 mA	I/O	
P4	P6	PH0/ PCRESET1	• GPIO Port H • Reset Card 1 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PH0	No Change	8 mA	I/O	
R4	T4	PH1/CFA8/ PCRESET2	• GPIO Port H • Address Bit 8 for PC Card (CF) in single card mode • Reset Card 2 for PC Card (PCMCIA or CF) in dual card mode	Input: PH1	No Change	8 mA	I/O	
T4	M7	PH2/ nPCSLOTE1	• GPIO Port H • Enable Card 1 for PC Card (PCMCIA or CF) in single or dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH2	No Change	8 mA	I/O	
N7	T5	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	• GPIO Port H • Address Bit 9 for PC Card (CF) in single card mode • Address Bit 25 for PC Card (PCMCIA) in single card mode • Enable Card 2 for PC Card (PCMCIA or CF) in dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH3	No Change	8 mA	I/O	
P8	R6	PH4/ nPCWAIT1	• GPIO Port H • WAIT Signal for Card 1 for PC Card (PCMCIA or CF) in single or dual card mode	Input: PH4	No Change	8 mA	I/O	
P5	R7	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	• GPIO Port H • Address Bit 10 for PC Card (CF) in single card mode • Address Bit 24 for PC Card (PCMCIA) in single card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or F) in dual card mode	Input: PH5	No Change	8 mA	I/O	
R5	P7	PH6/ nAC97RESET	• GPIO Port H • Audio Codec (AC97) Reset	Input: PH6	No Change	8 mA	I/O	
T5	T6	PH7/ nPCSTATRE	• GPIO Port H • Status Read Enable for PC Card (PCMCIA or F) in single or dual card mode	Input: PH7	No Change	8 mA	I/O	
R6	T7	LCDFP	LCD Frame Synchronization pulse	LOW	LOW	12 mA	O	
R8	R9	LCDLP	LCD Line Synchronization pulse	LOW	LOW	12 mA	O	

Table 6. 256-Ball BGA Package Numerical Pin List

BGA PIN	SIGNAL
A1	TDI
A2	MMCDATA/MMSPIDOUT
A3	MMCCLK/MMSPICLK
A4	ACIN
A5	VSS
A6	PF0/INT0
A7	VDDC
A8	A27/SCRST
A9	DQM0
A10	SCLK
A11	VSS
A12	nSCS3
A13	A24
A14	D24
A15	A23
A16	D23
B1	TCK
B2	TDO
B3	MMCCMD/MMSPIDIN
B4	ACSYNC
B5	PF4/INT4/SCVCCEN
B6	PF1/INT1
B7	PWM1
B8	VDD
B9	DQM1
B10	CS6/SCKE1_2
B11	D30
B12	D29
B13	D25
B14	VDD
B15	VSSC
B16	A22
C1	TMS
C2	nEXTPWR
C3	MEDCHG
C4	ACBITCLK
C5	PF7/INT7/PCRDY2
C6	PF2/INT2
C7	PWM0
C8	nWE0
C9	VSSC
C10	CS7/SCKE0
C11	nCAS
C12	nSWE
C13	D26

Table 6. 256-Ball BGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL
C14	nSCS0
C15	VSS
C16	A21
D1	BATOK
D2	nBATCHG
D3	nPOR
D4	WAKEUP
D5	ACOUT
D6	PF5/INT5/SCDETECT
D7	nPWME1
D8	nOE
D9	DQM2
D10	nWE3
D11	D31
D12	VDDC
D13	nSCS1
D14	D21
D15	A20
D16	D19
E1	VDDC
E2	UARTCTS2
E3	UARTDCD2
E4	nPWRFL
E5	UARTDSR2
E6	PF6/INT6/PCRDY1
E7	nPWME0
E8	VSS
E9	DQM3
E10	VDD
E11	nSCS2
E12	D27
E13	A18
E14	D18
E15	VDDC
E16	A17/SB1
F1	VDD
F2	UARTIRTX1
F3	UARTIRRX1
F4	UARTTX2
F5	COL1
F6	COL0
F7	VSS
F8	A26/SCCLK
F9	nRAS
F10	D22

AMBA APB BUS

The AMBA APB bus is a lower-speed 32-bit-wide peripheral data bus. The speed of this bus is selectable to be a divide-by-2, divide-by-4 or divide-by-8 of the speed of the AHB bus.

EXTERNAL BUS INTERFACE

The External Bus Interface (EBI) provides a 32-bit wide, high speed gateway to external memory devices. The memory devices supported include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous memory controller or Synchronous memory controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

LCD AHB BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

DMA BUSES

The LH7A400 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core. The DMA engine does not support memory to memory transfers.

Memory Map

The LH7A400 system has a 32-bit-wide address bus. This allows it to address up to 4GB of memory. This memory space is subdivided into a number of memory banks; see Figure 6. Four of these banks (each of 256MB) are allocated to the Synchronous memory controller. Eight of the banks (again, each 256MB) are allocated to the Asynchronous memory controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest is unused.

The LH7A400 can boot from either synchronous or asynchronous ROM/Flash. The selection is determined by the value of the MEDCHG pin at Power On Reset as shown in Table 8. When booting from synchronous memory, then synchronous bank 4 (nSCS3) is mapped into memory location zero. When booting from asynchronous memory, asynchronous memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 6 shows the memory map of the LH7A400 system for the two boot modes.

Once the LH7A400 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

Table 8. Boot Modes

BOOT MODE	LATCHED BOOT-WIDTH1	LATCHED BOOT-WIDTH0	LATCHED MEDCHG
8-bit ROM	0	0	0
16-bit ROM	0	1	0
32-bit ROM	1	0	0
32-bit ROM	1	1	0
16-bit SFlash (Initializes Mode Register)	0	0	1
16-bit SROM (Initializes Mode Register)	0	1	1
32-bit SFlash (Initializes Mode Register)	1	0	1
32-bit SROM (Initializes Mode Register)	1	1	1

Interrupt Controller

The LH7A400 interrupt controller is designed to control the interrupts from 28 different sources. Four interrupt sources are mapped to the FIQ input of the ARM922T and 24 are mapped to the IRQ input. FIQs have a higher priority than the IRQs. If two interrupts with the same priority become active at the same time, the priority must be resolved in software.

When an interrupt becomes active, the interrupt controller generates an FIQ or IRQ if the corresponding mask bit is set. No latching of interrupts takes place in the controller. After a Power On Reset all mask register bits are cleared, therefore masking all interrupts. Hence, enabling of the mask register must be done by software after a power-on-reset.

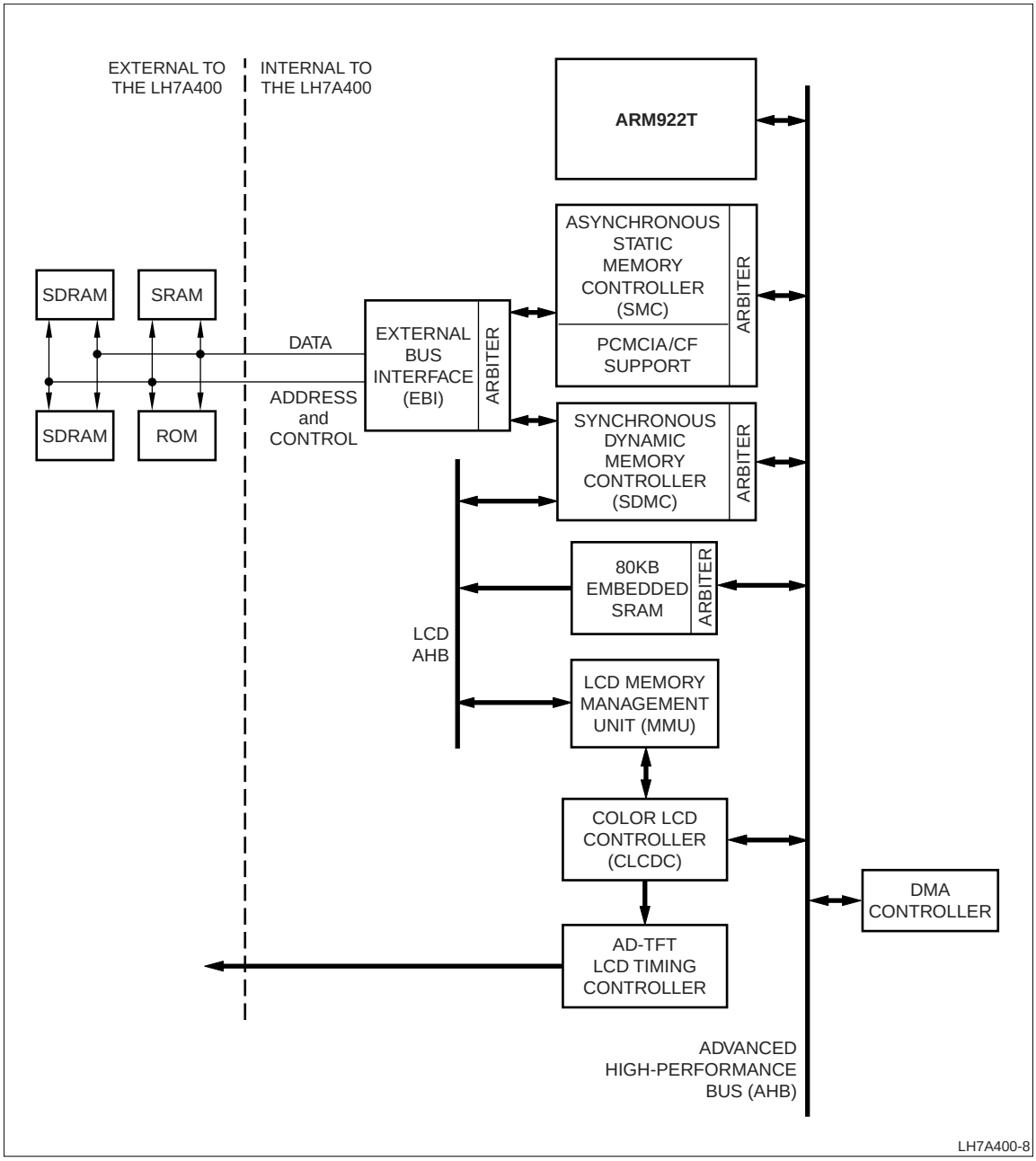


Figure 7. External Bus Interface Block Diagram

Direct Memory Access Controller (DMA)

The DMA Controller interfaces streams from the following three peripherals to the system memory:

- USB (1 Tx and 1 Rx DMA Channel)
- MMC (1 Tx and 1 Rx DMA Channel)
- AC97 (3 Tx and 3 Rx DMA Channels).

Each has its own bi-directional peripheral DMA bus capable of transferring data in both directions simultaneously. All memory transfers take place via the main system AHB bus.

DMA Specific features are:

- Independent DMA channels for Tx and Rx
- Two Buffer Descriptors per channel to avoid potential data under/over-flows due to software introduced latency
- No Buffer wrapping
- Buffer size may be equal to, greater than, or less than the packet size. Transfers can automatically switch between buffers.
- Maskable interrupt generation
- Internal arbitration between DMA Channels and external bus arbiter.
- For DMA Data transfer sizes, byte, word and quadword data transfers are supported.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. A system interrupt is generated when any or all of the DMA channels wish to inform the processor that a new buffer needs to be allocated. The DMA controller services three peripherals using ten DMA channels, each with its own peripheral DMA bus capable of transferring data in both directions simultaneously.

The MMC and USB peripherals each use two DMA channels, one for transmit and one for receive. The AC97 peripheral uses six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overheads. The DMA Controller does not support memory to memory transfers.

USB Device

The features of the USB are:

- Fully compliant to USB 1.1 specification
- Provides a high level interface that shields the firmware from USB protocol details
- Compatible with both OpenHCI and Intel's UHCI standards
- Supports full-speed (12 Mbps) functions
- Supports Suspend and Resume signalling.

Color LCD Controller

The LH7A400's LCD Controller is programmable to support up to 1,024 × 768, 16-bit color LCD panels. It interfaces directly to STN, color STN, TFT, AD-TFT, and HR-TFT panels. Unlike other LCD controllers, the LH7A400's LCD Controller incorporates the timing conversion logic from TFT to HR- and AD-TFT, allowing a direct interface to these panels and minimizing external chip count.

The Color LCD Controller features support for:

- Up to 1,024 × 768 Resolution
- 16-bit Video Bus
- STN, Color STN, AD-TFT, HR-TFT, TFT panels
- Single and Dual Scan STN panels
- Up to 15 Gray Shades
- Up to 64,000 Colors

AC97 Advanced Audio Codec Interface

The AC97 Advanced Audio Codec controller includes a 5-pin serial interface to an external audio codec. The AC97 LINK is a bi-directional, fixed rate, serial Pulse Code Modulation (PCM) digital stream, dividing each audio frame into 12 outgoing and 12 incoming data streams (slots), each with 20-bit sample resolution.

The AC97 controller contains logic that controls the AC97 link to the Audio Codec and an interface to the AMBA APB.

Its main features include:

- Serial-to-parallel conversion for data received from the external codec
- Parallel-to-serial conversion for data transmitted to the external codec
- Reception/Transmission of control and status information via the AMBA APB interface
- Supports up to 4 different codec sampling rates at a time with its 4 transmit and 4 receive channels. The transmit and receive paths are buffered with internal FIFO memories, allowing data to be stored independently in both transmit and receive modes. The outgoing data for the FIFOs can be written via either the APB interface or with DMA channels 1 - 3.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	MINIMUM	MAXIMUM
DC Core Supply Voltage (VDDC)	–0.3 V	2.4 V
DC I/O Supply Voltage (VDD)	–0.3 V	4.6 V
DC Analog Supply Voltage (VDDA)	–0.3 V	2.4 V
5 V Tolerant Digital Input Pin Voltage	–0.5 V	5.5 V
ESD, Human Body Model (Analog pins AN0 - AN9 rated at 500 V)		2 kV
ESD, Charged Device Model		1 kV
Storage Temperature	–55°C	125°C

NOTE: Except for Storage Temperature, these ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Recommended Operating Conditions

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	1.71 V	1.8 V	1.89 V	1, 4
DC Core Supply Voltage (VDDC)	2.0 V	2.1 V	2.2 V	1, 5
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	2, 6
DC I/O Supply Voltage (VDD)	3.14 V	3.3 V	3.6 V	2, 7
DC Analog Supply Voltage for PLLs (VDDA)	1.71 V	1.8 V	1.89 V	
Clock Frequency (0°C to +70°C)	10 MHz		200 MHz	3, 4, 6
Clock Frequency (–40°C to +85°C)	10 MHz		195 MHz	3, 4, 6
Bus Clock Frequency (–40°C to +85°C)			100 MHz	3, 4, 6
Clock Frequency (0°C to +70°C)	10 MHz		250 MHz	3, 5, 7
Clock Frequency (–40°C to +85°C)	10 MHz		245 MHz	3, 5, 7
Bus Clock Frequency (–40°C to +85°C)			125 MHz	3, 5, 7
External Clock Input (XTALIN)	14 MHz	14.7456 MHz	20 MHz	8
External Clock Input (XTALIN) Voltage	1.71 V	1.8 V	1.89 V	
Operating Temperature	–40°C	25°C	+85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 33
2. USB is not functional below 3.0 V
3. Using 14.7456 MHz Main Oscillator Crystal and 32.768 kHz RTC Oscillator Crystal
4. VDDC = 1.71 V to 1.89 V (LH7A400N0G000xx)
5. VDDC = 2.1 V ± 5 % (LH7A400N0G076xx only)
6. VDD = 3.0 V to 3.6 V (LH7A400N0G000xx)
7. VDD = 3.14V to 3.60 V (LH7A400N0G076xx only)
8. IMPORTANT: Most peripherals will NOT function with crystals other than 14.7456 MHz.

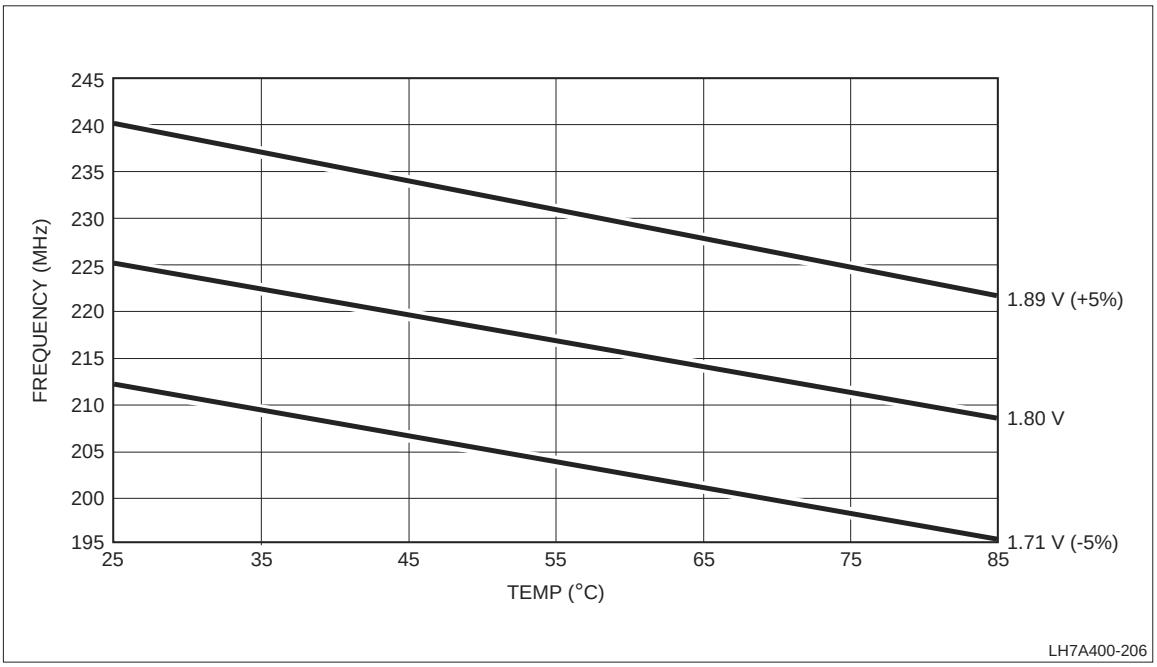


Figure 8. Temperature/Voltage/Speed Chart (For LH7A400N0G000xx)

Table 9. Clock Frequency vs. Voltages (VDDC) vs. Temperature

PARAMETER		1.71 V	1.8 V	1.89 V
25°C	Clock Frequency (FCLK)	211 MHz	225 MHz	240 MHz
	Clock Period (FCLK)	4.74 ns	4.44 ns	4.17 ns
70°C	Clock Frequency (FCLK)	200 MHz	212 MHz	227 MHz
	Clock Period (FCLK)	5.00 ns	4.72 ns	4.41 ns
85°C	Clock Frequency (FCLK)	195 MHz	208 MHz	222 MHz
	Clock Period (FCLK)	5.13 ns	4.81 ns	4.50 ns

NOTES:
1. Table 9 is representative of a typical wafer process. Guaranteed values are in the Recommended Operating Conditions table.
2. LH7A400N0G000xx

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 10 were derived under the conditions presented here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All voltages at maximum specified values
- Maximum specified ambient temperature (tAMB).

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- LINUX operating system running from SDRAM
- UART and AC97 peripherals operating; all other peripherals as needed by the OS
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate, data in SDRAM
- I/O loads at nominal
- Cache enabled
- FCLK = 200 MHz or 250 MHz; HCLK = 100 MHz or 125 MHz; PCLK = 50 MHz or 62.5 MHz
- All voltages at typical values
- Nominal case temperature (tAMB).

Table 10. Current Consumption by Mode

SYMBOL	PARAMETER	LH7A400N0G000xx (FCLK = 200 MHz)		LH7A400N0G076xx (FCLK = 250 MHz)	
		TYP.	MAX.	TYP.	UNITS
ACTIVE MODE					
ICORE	Core Current	110	135	250	mA
IIO	I/ O Current	15	45		mA
HALT MODE (ALL PERIPHERALS DISABLED)					
ICORE	Core Current	24	39	50	mA
IIO	I/ O Current	1	2		mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)					
ICORE	Core Current	40		125	μA
IIO	I/ O Current	2		4	μA

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 11 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the CPU clock running at 200 MHz, typical conditions, and no I/O loads. This current is supplied by the 1.8 VDDC power supply.

Table 11. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
AC97	1.3	mA
UART (Each)	1.0	mA
RTC	0.005	mA
Timers (Each)	0.1	mA
LCD (+I/O)	5.4 (1.0)	mA
MMC	0.6	mA
SCI	23	mA
PWM (each)	< 0.1	mA
BMI-SWI	1.0	mA
BMI-SBus	1.0	mA
SDRAM (+I/O)	1.5 (14.8)	mA
USB (+PLL)	5.6 (3.3)	mA
ACI	0.8	mA

Table 12. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
MMC INTERFACE SIGNALS						
MMCCMD	Output	100 pF	tOS	5 ns		MMC Command Setup
			tOH	5 ns		MMC Command Hold
MMCDATA	Output	100 pF	tOS	5 ns		MMC Data Setup
			tOH	5 ns		MMC Data Hold
MMCDATA	Input		tIS	3 ns		MMC Data Setup
			tIH	3 ns		MMC Data Hold
MMCCMD	Input		tIS	3 ns		MMC Command Setup
			tIH	3 ns		MMC Command Hold
AC97 INTERFACE SIGNALS						
ACOUT/ACSYNC	Output	30 pF	tOVAC97		15 ns	AC97 Output Valid/Sync Valid
			tOHAC97	10 ns		AC97 Output Hold/Sync Hold
ACIN	Input		tISAC97	10 ns		AC97 Input Setup
			tIHAC97	2.5 ns		AC97 Input Hold
ACBITCLK	Input		tACBITCLK	72 ns	90 ns	AC97 Clock Period
SYNCHRONOUS SERIAL PORT (SSP)						
SSPFRM	Output		tOVSSPFRM		10 ns	SSPFRM Valid
			tOHSSPFRM	5 ns		SSPFRM Hold
SSPTX	Output	50 pF	tOVSSPOUT		10 ns	SSP Transmit Valid
			tOHSSPOUT	5 ns		SSP Transmit Hold
SSPRX	Input		tISSSPIN	14 ns		SSP Receive Setup
SSPCLK	Output		tSSPCLK	8.819 ms	271 ns	SSP Clock Period
AUDIO CODEC INTERFACE (ACI)						
ACOUT	Output	30 pF	tOVD		15 ns	ACOUT delay from rising clock edge
			tOHD	10 ns		ACOUT Hold
ACIN	Input		tIS	10 ns		ACIN Setup
			tIH	2.5 ns		ACIN Hold
COLOR LCD CONTROLLER						
LCDVD [17:0]	Output	30 pF	tOV	—	3 ns	LCD Data Clock to Data Valid

NOTES:
1. Register BCRx:WST1 = 0b000
2. For Output Drive strength specifications, refer to Table 3
3. LH7A400N0G076xx only
4. LH7A400N0G000xx only

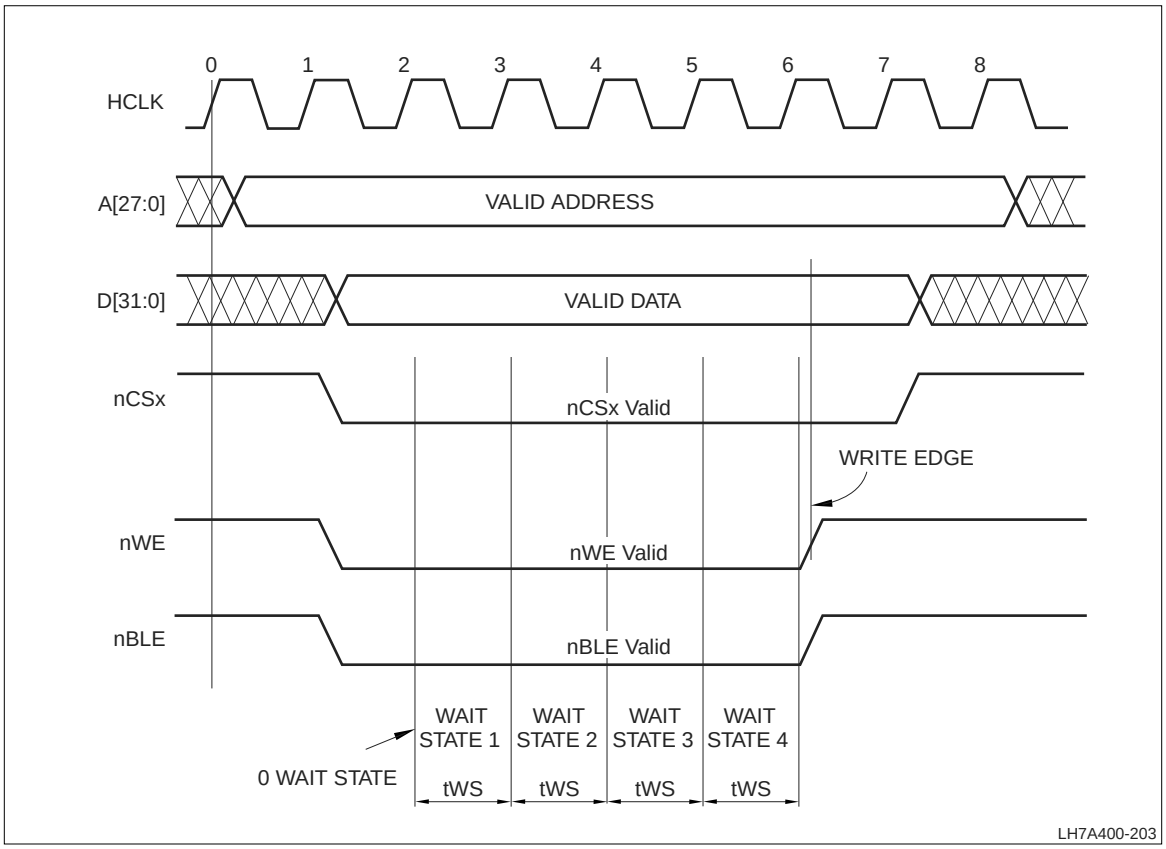


Figure 11. External Asynchronous Memory Write with 4 Wait States (BCRx:WST1 = 0b100)

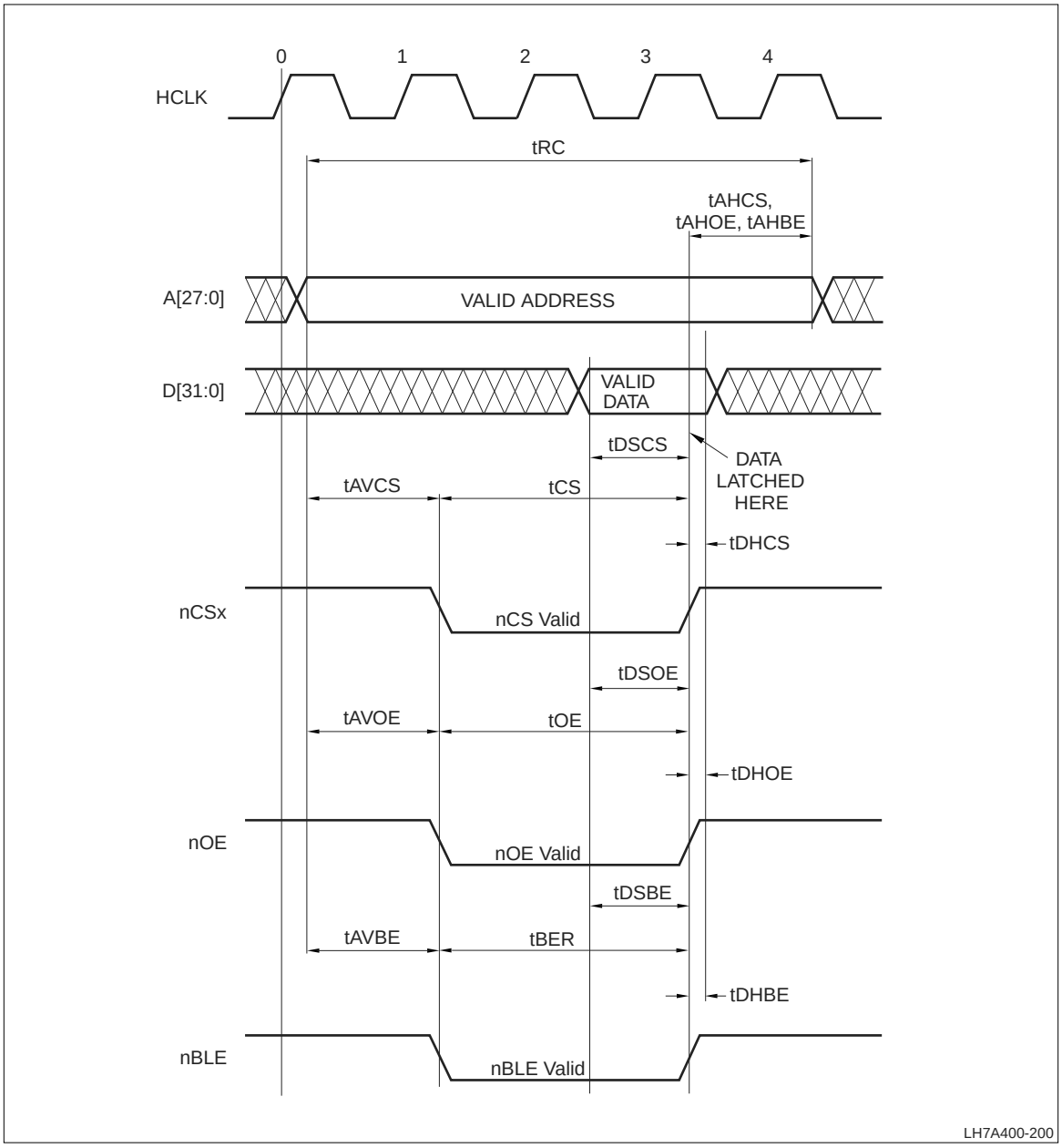


Figure 12. External Asynchronous Memory Read with 0 Wait States (BCRx:WST1 = 0b000)

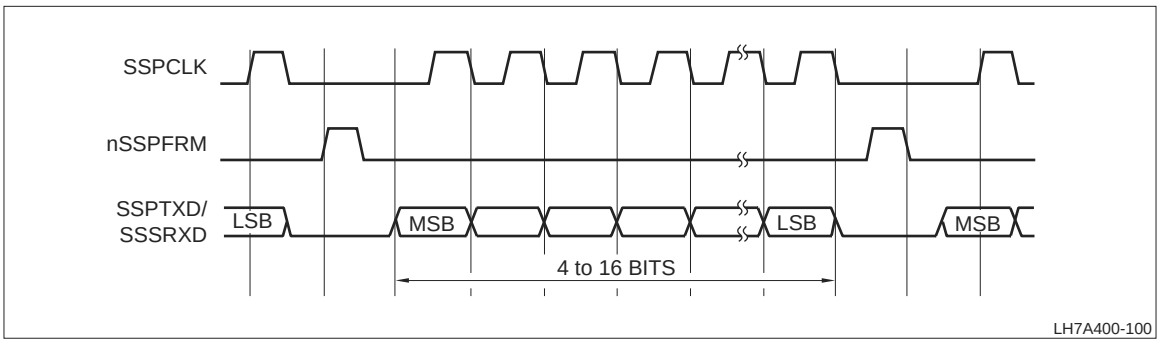


Figure 19. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 0

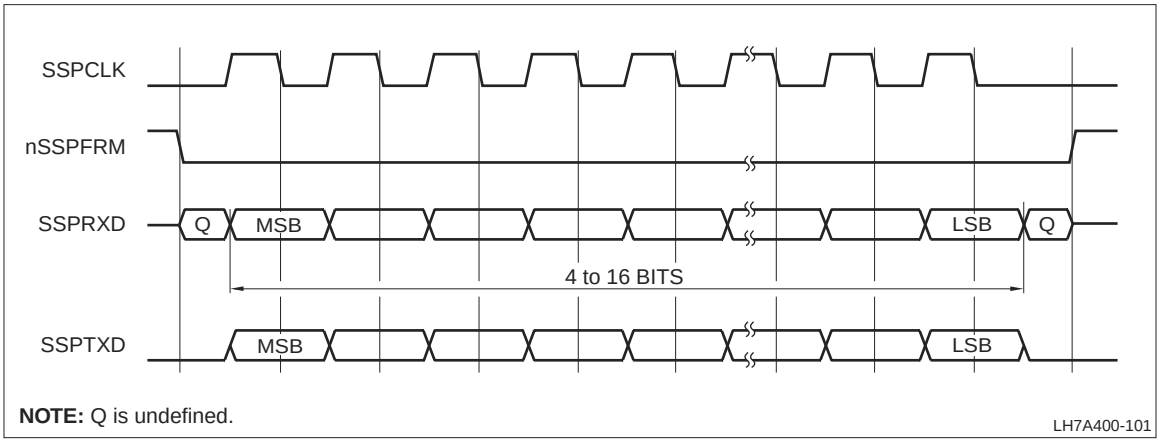


Figure 20. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 1

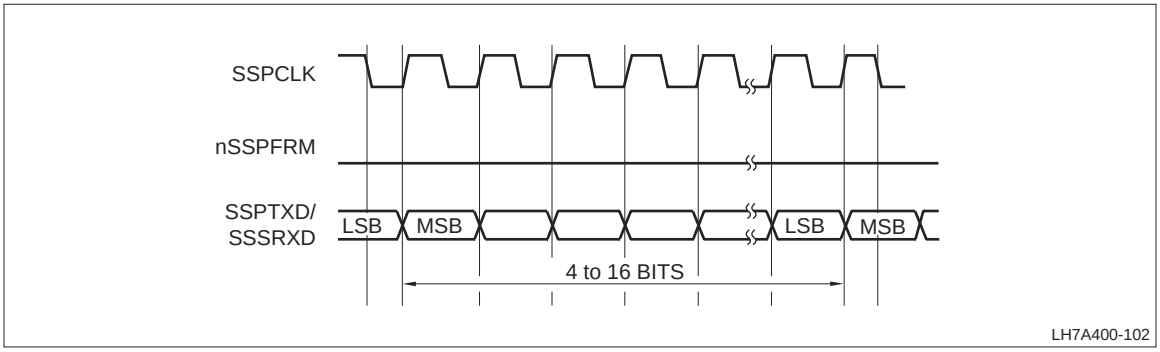


Figure 21. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 1

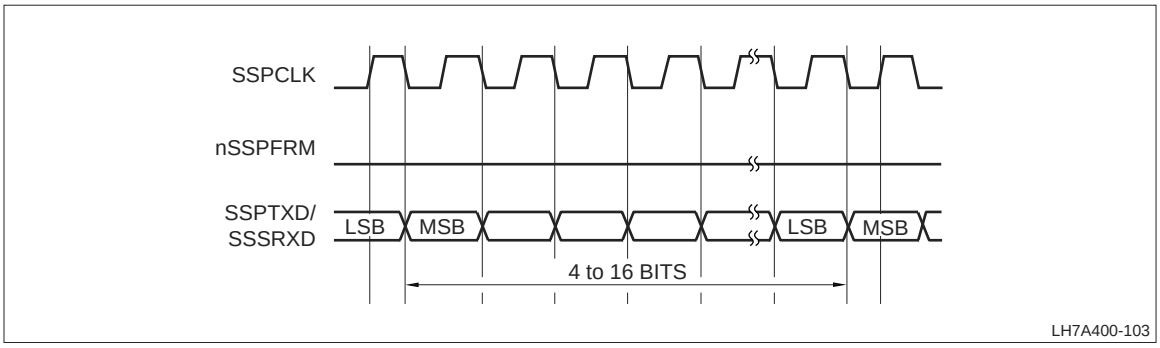
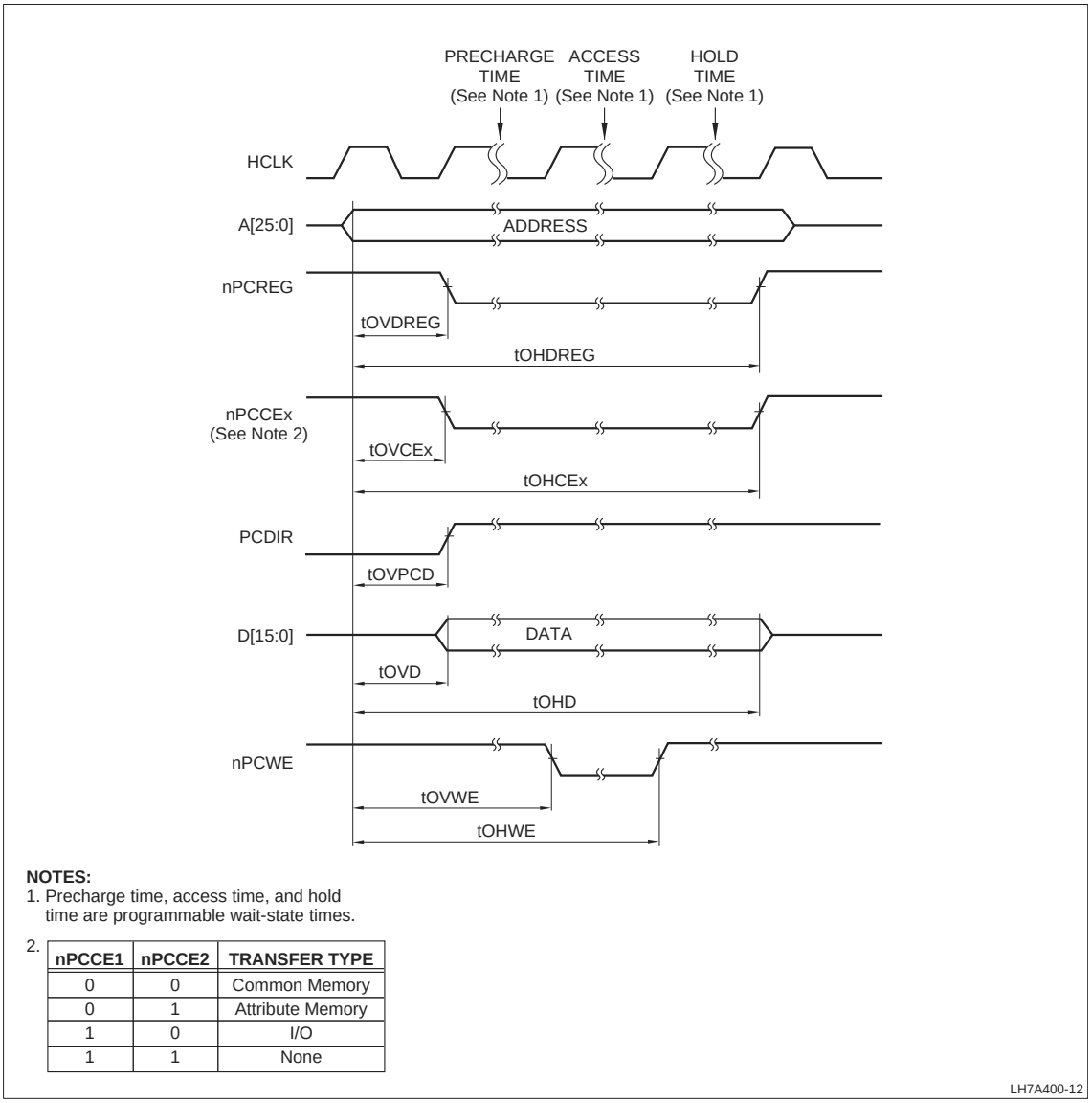


Figure 22. Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 1



NOTES:
1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

Figure 29. PCMCIA Write Transfer

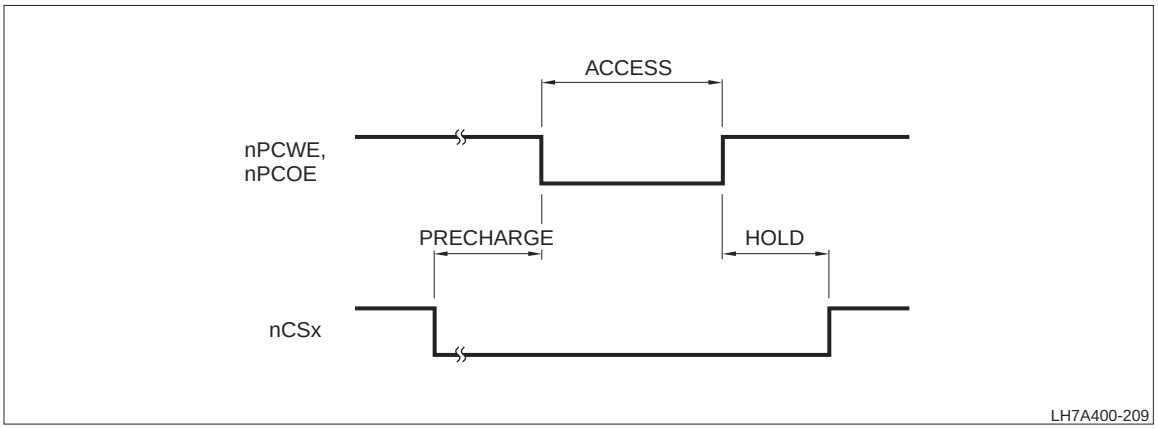


Figure 30. PCMCIA Precharge, Access, and Hold Waveform

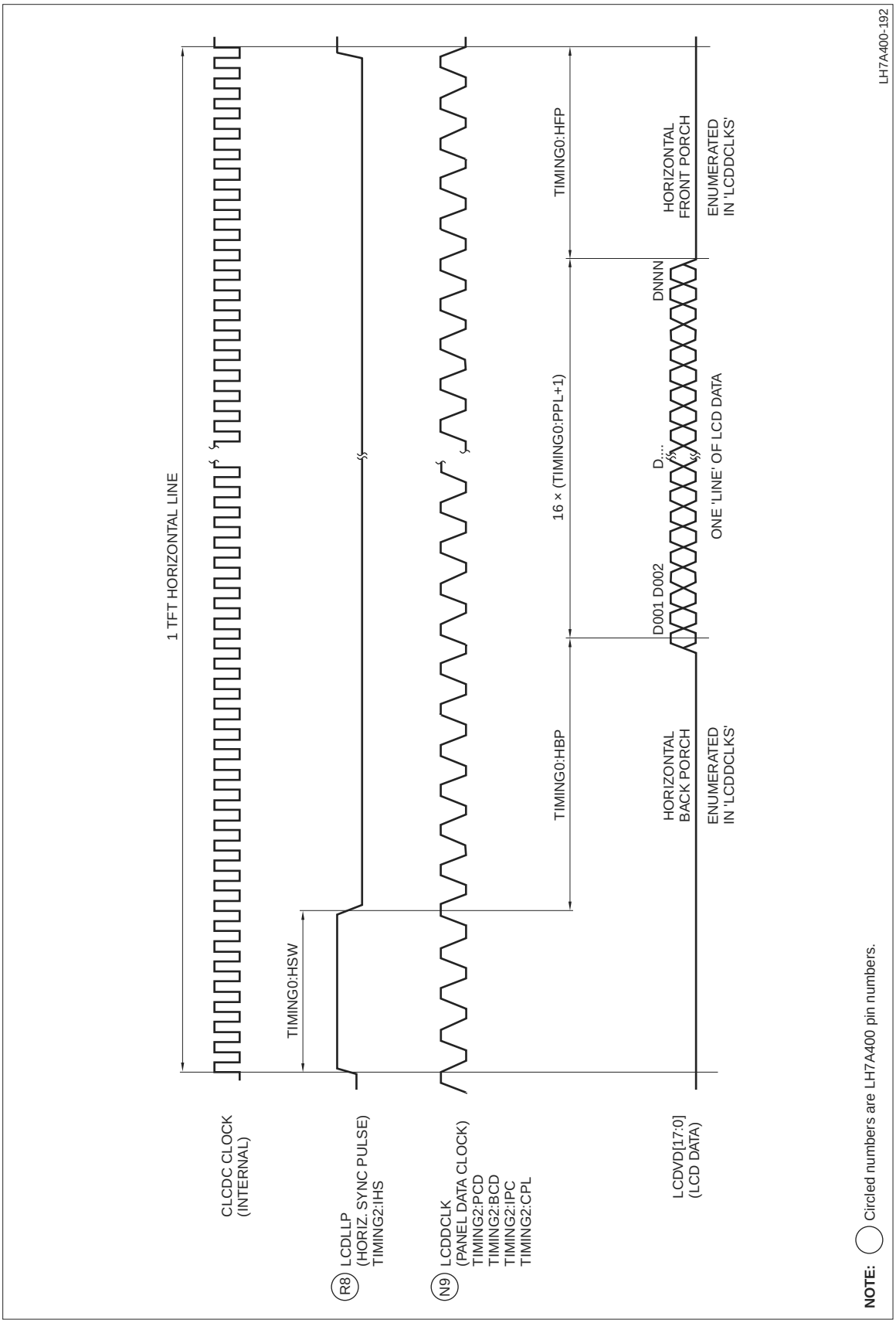


Figure 38. TFT Horizontal Timing Diagram

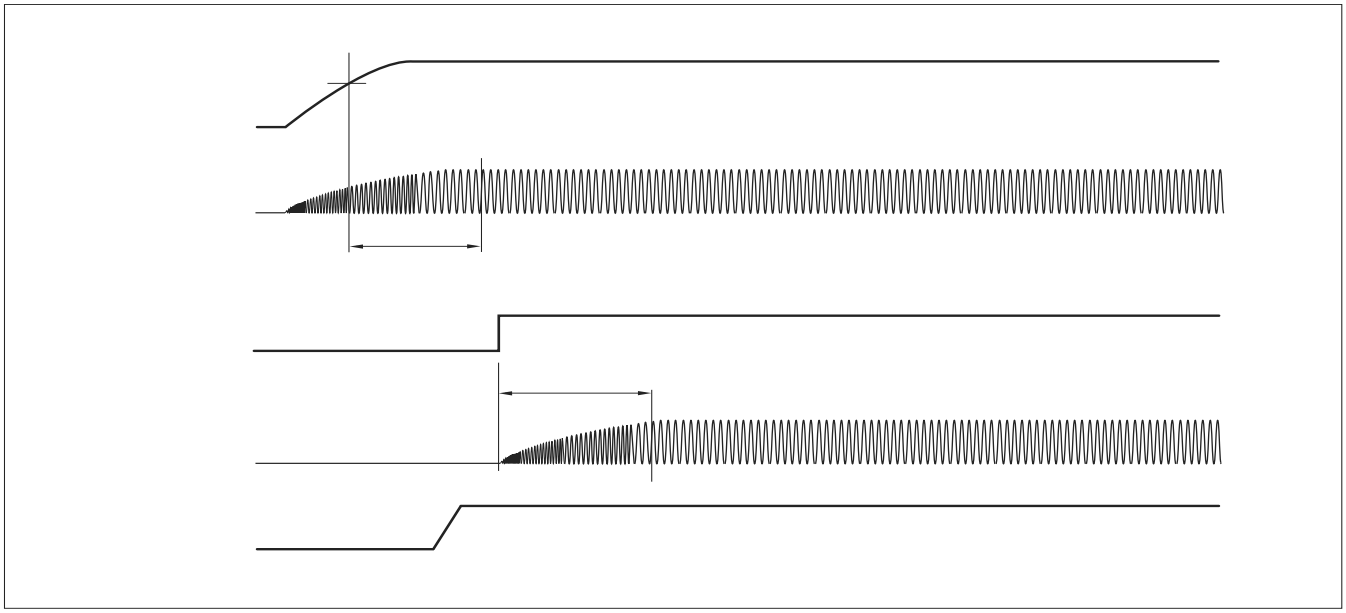


Figure 42. Oscillator Start-up

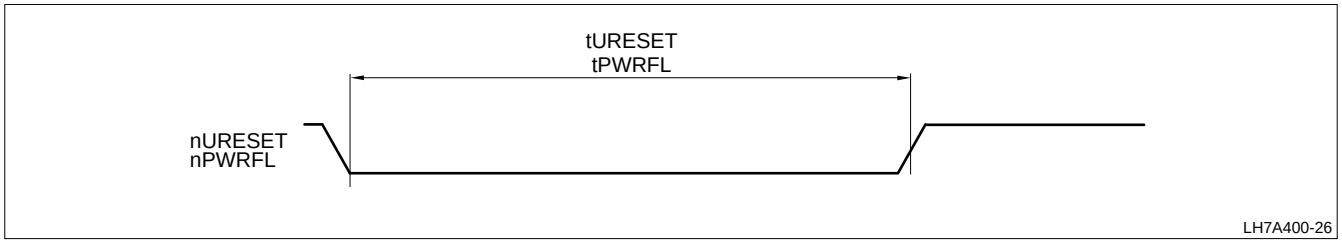


Figure 43. External Reset

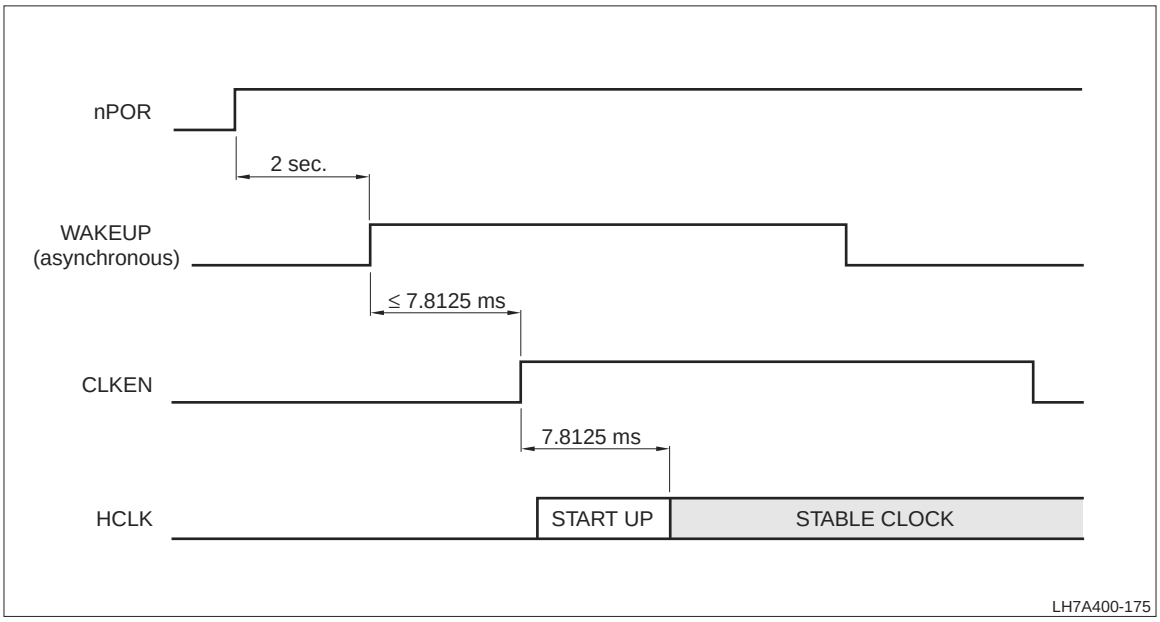


Figure 44. Signal Timing After Reset

Operating Temperature and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

NXP recommends that users implementing a system to meet industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (i.e., noise immunity of the clock input to the SoC).

Printed Circuit Board Layout Practices

LH7A400 POWER SUPPLY DECOUPLING

The LH7A400 has separate power and ground pins for different internal circuitry sections. The VDD and VSS pins supply power to I/O buffers, while VDDC and VSSC supply power to the core logic, and VDDA/VSSA supply analog power to the PLLs.

Each of the VDD and VDDC pins must be provided with a low impedance path to the corresponding board power supply. Likewise, the VSS, VSSA, and VSSC pins must be provided with a low impedance path to the board ground.

Each power supply must be decoupled to ground using at least one 0.1 μF high frequency capacitor located as close as possible to a VDDx, VSSx pin pair on each of the four sides of the chip. If room on the circuit board allows, add one 0.01 μF high frequency capacitor near each VDDx, VSSx pair on the chip.

To be effective, the capacitor leads and associated circuit board traces connecting to the chip VDDx, VSSx pins must be kept to less than half an inch (12.7 mm) per capacitor lead. There must be one bulk 10 μF capacitor for each power supply placed near one side of the chip.

RECOMMENDED PLL, VDDA, VSSA FILTER

The VDDA pins supply power to the chip PLL circuitry. VSSA is the ground return path for the PLL circuit. NXP recommends a low-pass filter attached as shown in Figure 47. The values of the inductor and capacitors are not critical. The low-pass filter prevents high frequency noise from adversely affecting the PLL circuits. The distance from the IC pin to the high frequency capacitor should be as short as possible.

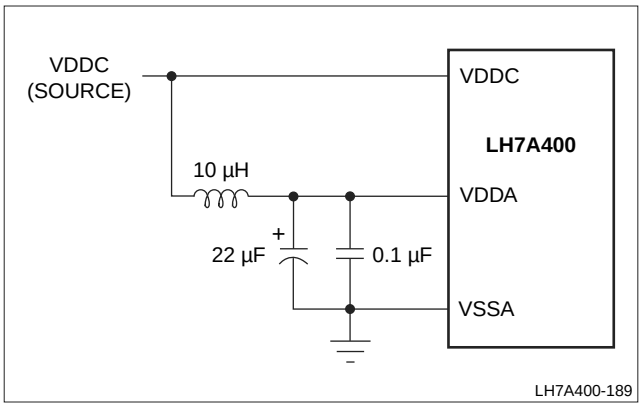


Figure 47. VDDA, VSSA Filter Circuit

UNUSED INPUT SIGNAL CONDITIONING

Floating input signals can cause excessive power consumption. Unused inputs without internal pull-up or pull-down resistors should be pulled up or down externally (NXP recommends tying HIGH), to tie the signal to its inactive state. 33 KΩ or less is recommended.

Some GPIO signals default to inputs. If the pins that carry these signals are unused, software can program these signals as outputs, eliminating the need for pull-ups or pull-downs. Power consumption may be higher than expected until software completes programming the GPIO. Some LH7A400 inputs have internal pull-ups or pull-downs. If unused, these inputs do not require external conditioning.

OTHER CIRCUIT BOARD LAYOUT PRACTICES

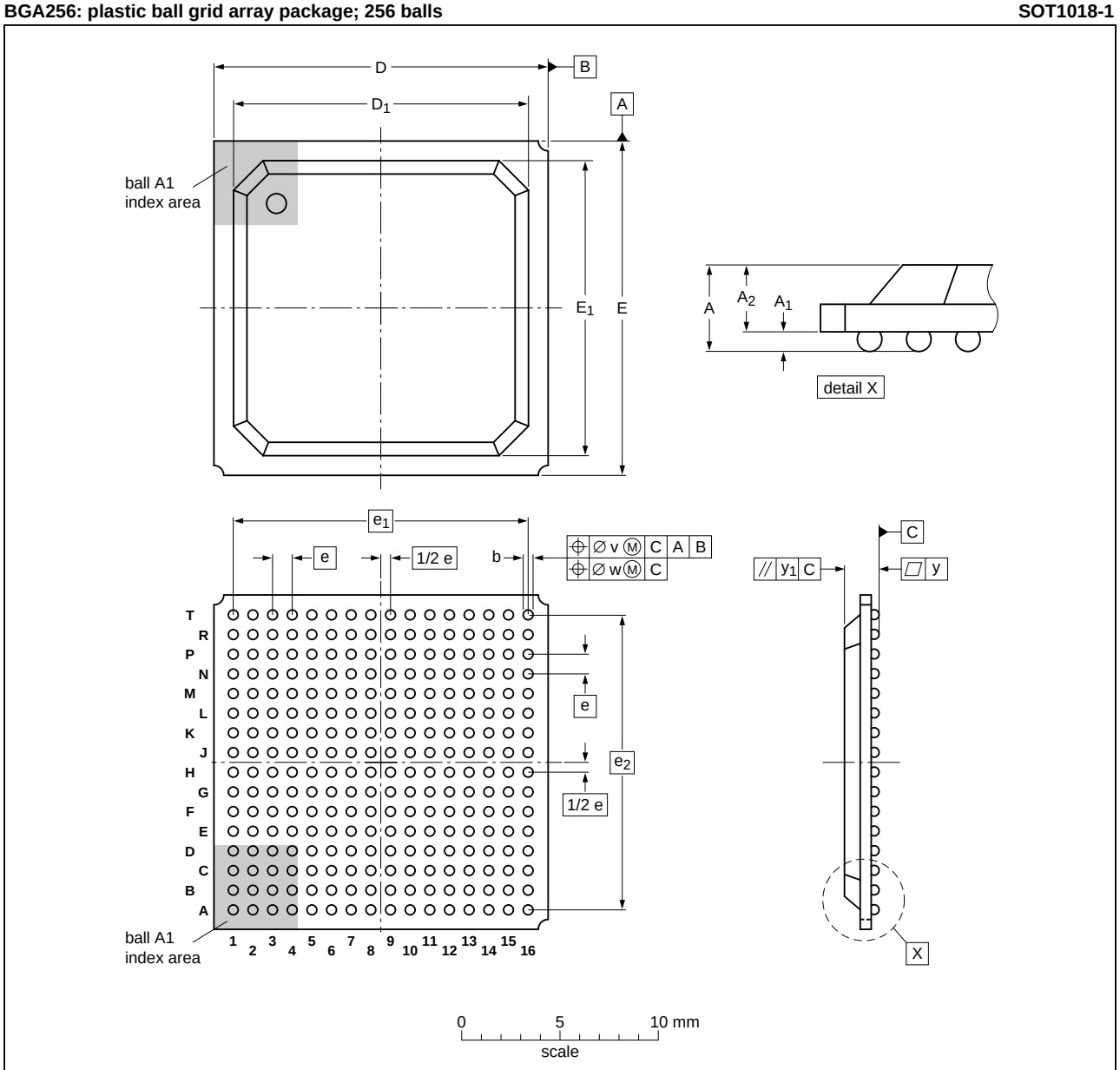
All outputs have fast rise and fall times. Printed circuit trace interconnection length must therefore be reduced to minimize overshoot, undershoot and reflections caused by transmission line effects of these fast output switching times. This recommendation particularly applies to the address and data buses.

When considering capacitance, calculations must consider all device loads and capacitances due to the circuit board traces. Capacitance due to the traces will depend upon a number of factors, including the trace width, dielectric material the circuit board is made from and proximity to ground and power planes.

Attention to power supply decoupling and printed circuit board layout becomes more critical in systems with higher capacitive loads. As these capacitive loads increase, transient currents in the power supply and ground return paths also increase.

PACKAGE SPECIFICATIONS

BGA256: plastic ball grid array package; 256 balls **SOT1018-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	D_1	E	E_1	e	e_1	e_2	v	w	y	y_1
mm	1.95	0.5 0.3	1.45 1.25	0.55 0.45	17.2 16.8	15.75 14.75	17.2 16.8	15.75 14.75	1	15	15	0.25	0.1	0.15	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1018-1						

Figure 48. Package outline SOT1018-1 (BGA256)

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