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Details

Product Status	Active
Core Processor	e200z4d, e200z0h
Core Size	32-Bit Dual-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644cf0vlu8

3 Package pinouts and signal descriptions

The available LQFP pinouts and the MAPBGA ballmaps are provided in the following figures. For functional port pin description, see Table 4.

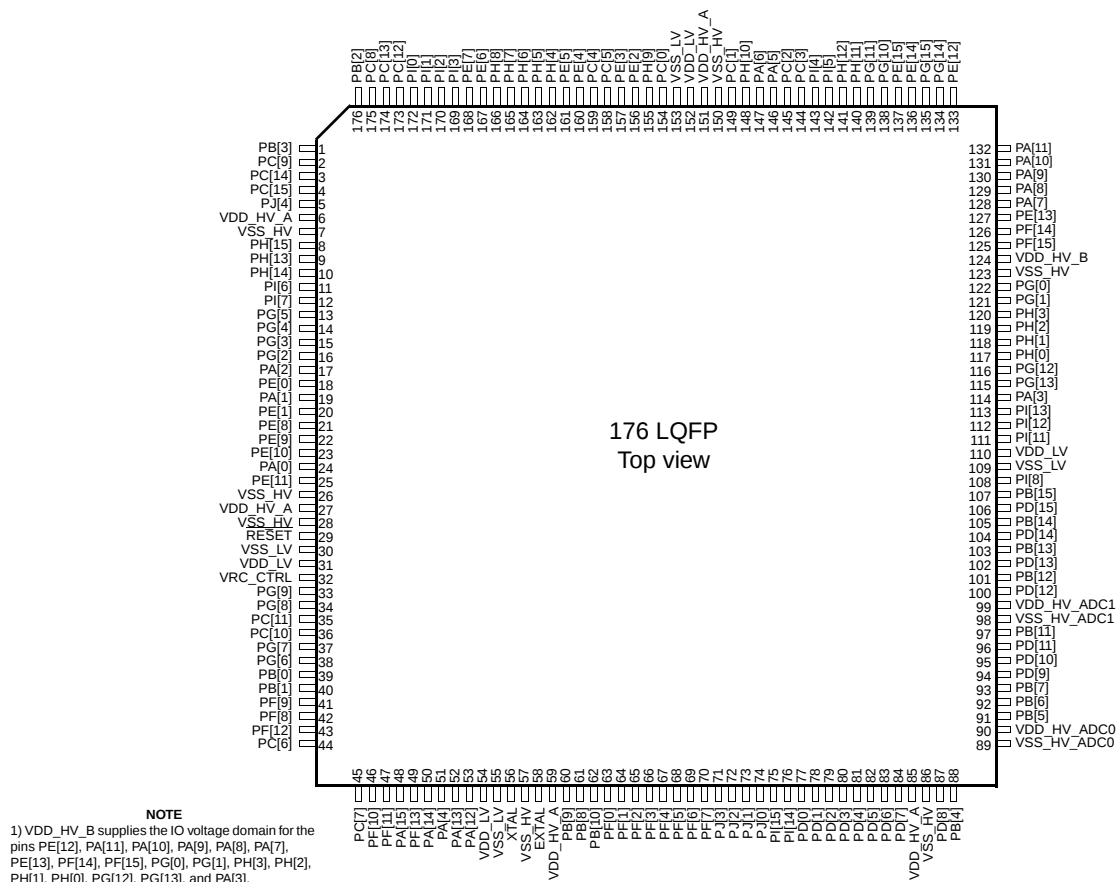
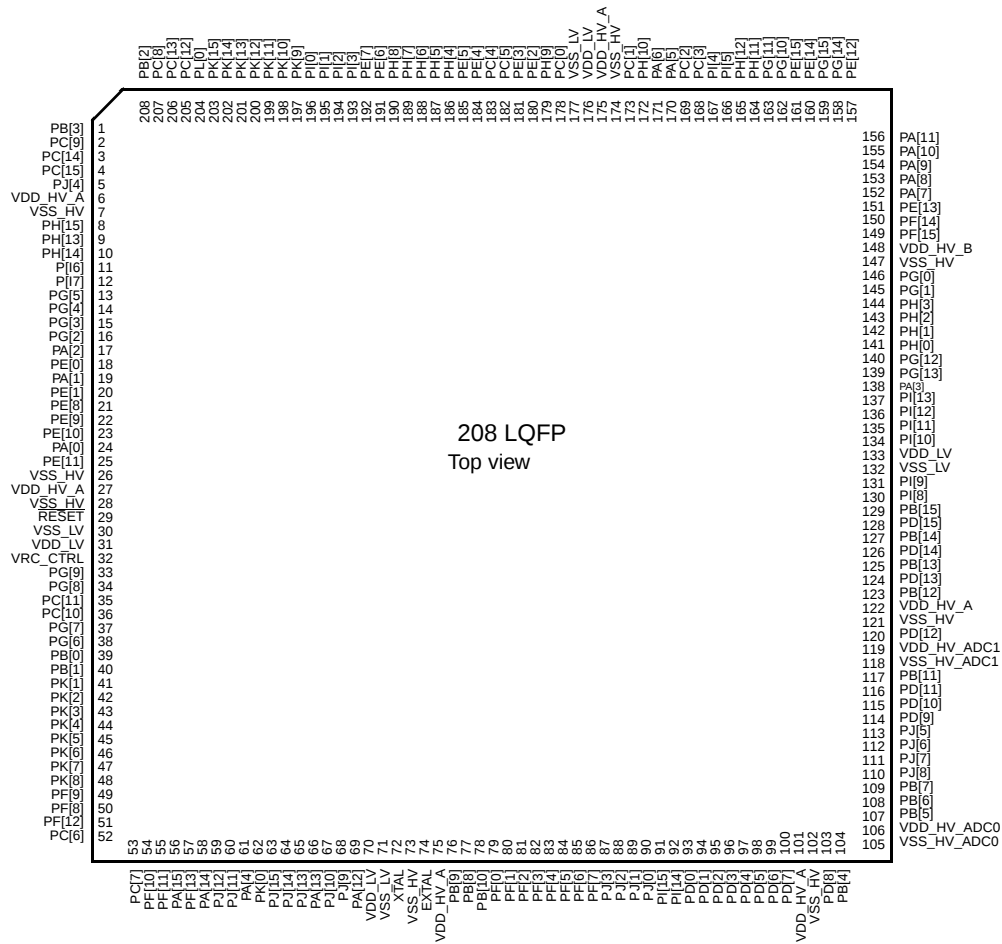


Figure 2. 176-pin LQFP configuration



NOTE

- 1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
- 2) Availability of port pin alternate functions depends on product selection.

Figure 3. 208-pin LQFP configuration

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[63] CS2_1 E0UC[27] — FR_DBG[1] ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	106	128	J13
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX WKPU[6]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	18	18	G2
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M/S	Tristate	20	20	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[66] E0UC[18] — — FR_A_TX_EN SIN_1 EIRQ[21]	SIUL eMIOS_0 — — Flexray DSPI_1 SIUL	I/O I/O — — O I I	M/S	Tristate	156	180	A7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3 — —	GPIO[67] E0UC[19] SOUT_1 — FR_A_RX WKPU[29]	SIUL eMIOS_0 DSPI_1 — Flexray WKPU	I/O I/O O — I I	M/S	Tristate	157	181	A10
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[68] E0UC[20] SCK_1 — FR_B_TX EIRQ[9]	SIUL eMIOS_0 DSPI_1 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	160	184	A8
PE[5]	PCR[69]	AF0 AF1 AF2 AF3 — —	GPIO[69] E0UC[21] CS0_1 MA[2] FR_B_RX WKPU[30]	SIUL eMIOS_0 DSPI_1 ADC_0 Flexray WKPU	I/O I/O I/O O I I	M/S	Tristate	161	185	B8

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PG[5]	PCR[101]	AF0	GPIO[101]	SIUL	I/O	S	Tristate	13	13	D1
		AF1	E1UC[14]	eMIOS_1	I/O					
		AF2	—	—	—					
		AF3	—	—	—					
		—	WKPU[18]	WKPU	I					
		—	SIN_3	DSPI_3	I					
PG[6]	PCR[102]	AF0	GPIO[102]	SIUL	I/O	M/S	Tristate	38	38	M1
		AF1	E1UC[15]	eMIOS_1	I/O					
		AF2	LIN6TX	LINFlexD_6	O					
		AF3	—	—	—					
PG[7]	PCR[103]	AF0	GPIO[103]	SIUL	I/O	S	Tristate	37	37	L2
		AF1	E1UC[16]	eMIOS_1	I/O					
		AF2	E1UC[30]	eMIOS_1	I/O					
		AF3	—	—	—					
		—	LIN6RX	LINFlexD_6	I					
		—	WKPU[20]	WKPU	I					
PG[8]	PCR[104]	AF0	GPIO[104]	SIUL	I/O	S	Tristate	34	34	K3
		AF1	E1UC[17]	eMIOS_1	I/O					
		AF2	LIN7TX	LINFlexD_7	O					
		AF3	CS0_2	DSPI_2	I/O					
		—	EIRQ[15]	SIUL	I					
PG[9]	PCR[105]	AF0	GPIO[105]	SIUL	I/O	S	Tristate	33	33	J4
		AF1	E1UC[18]	eMIOS_1	I/O					
		AF2	—	—	—					
		AF3	SCK_2	DSPI_2	I/O					
		—	LIN7RX	LINFlexD_7	I					
		—	WKPU[21]	WKPU	I					
PG[10]	PCR[106]	AF0	GPIO[106]	SIUL	I/O	S	Tristate	138	162	B13
		AF1	E0UC[24]	eMIOS_0	I/O					
		AF2	E1UC[31]	eMIOS_1	I/O					
		AF3	—	—	—					
		—	SIN_4	DSPI_4	I					
PG[11]	PCR[107]	AF0	GPIO[107]	SIUL	I/O	M/S	Tristate	139	163	A16
		AF1	E0UC[25]	eMIOS_0	I/O					
		AF2	CS0_4	DSPI_4	I/O					
		AF3	CS0_6	DSPI_6	I/O					
PG[12]	PCR[108]	AF0	GPIO[108]	SIUL	I/O	M/S	Tristate	116	140	F15
		AF1	E0UC[26]	eMIOS_0	I/O					
		AF2	SOUT_4	DSPI_4	O					
		AF3	—	—	—					
		ALT4	TXD[2]	FEC	O					

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PG[13]	PCR[109]	AF0 AF1 AF2 AF3 ALT4	GPIO[109] E0UC[27] SCK_4 — TXD[3]	SIUL eMIOS_0 DSPI_4 — FEC	I/O I/O I/O — O	M/S	Tristate	115	139	F16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3 —	GPIO[110] E1UC[0] LIN8TX — SIN_6	SIUL eMIOS_1 LINFlexD_8 — DSPI_6	I/O I/O O — I	S	Tristate	134	158	C13
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] SOUT_6 — LIN8RX	SIUL eMIOS_1 DSPI_6 — LINFlexD_8	I/O I/O O — I	M/S	Tristate	135	159	D13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[112] E1UC[2] — — TXD[1] SIN_1	SIUL eMIOS_1 — — FEC DSPI_1	I/O I/O — — O I	M/S	Tristate	117	141	E15
PH[1]	PCR[113]	AF0 AF1 AF2 AF3 ALT4	GPIO[113] E1UC[3] SOUT_1 — TXD[0]	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O O — O	M/S	Tristate	118	142	F13
PH[2]	PCR[114]	AF0 AF1 AF2 AF3 ALT4	GPIO[114] E1UC[4] SCK_1 — TX_EN	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	119	143	D16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3 ALT4	GPIO[115] E1UC[5] CS0_1 — TX_ER	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	120	144	F14
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] SOUT_7 —	SIUL eMIOS_1 DSPI_7 —	I/O I/O O —	M/S	Tristate	162	186	D7

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PJ[15]	PCR[159]	AF0 AF1 AF2 AF3 —	GPIO[159] — CS1_6 — CAN1RX	SIUL — DSPI_6 — FlexCAN_1	I/O — O — I	M/S	Tristate	—	63	R4
PK[0]	PCR[160]	AF0 AF1 AF2 AF3	GPIO[160] CAN1TX CS2_6 —	SIUL FlexCAN_1 DSPI_6 —	I/O O O —	M/S	Tristate	—	62	T3
PK[1]	PCR[161]	AF0 AF1 AF2 AF3 —	GPIO[161] CS3_6 — — CAN4RX	SIUL DSPI_6 — — FlexCAN_4	I/O O — — I	M/S	Tristate	—	41	H4
PK[2]	PCR[162]	AF0 AF1 AF2 AF3	GPIO[162] CAN4TX — —	SIUL FlexCAN_4 — —	I/O O — —	M/S	Tristate	—	42	L4
PK[3]	PCR[163]	AF0 AF1 AF2 AF3 — —	GPIO[163] E1UC[0] — — CAN5RX LIN8RX	SIUL eMIOS_1 — — FlexCAN_5 LINFlexD_8	I/O I/O — — I I	M/S	Tristate	—	43	N1
PK[4]	PCR[164]	AF0 AF1 AF2 AF3	GPIO[164] LIN8TX CAN5TX E1UC[1]	SIUL LINFlexD_8 FlexCAN_5 eMIOS_1	I/O O O I/O	M/S	Tristate	—	44	M3
PK[5]	PCR[165]	AF0 AF1 AF2 AF3 — —	GPIO[165] — — — CAN2RX LIN2RX	SIUL — — — FlexCAN_2 LINFlexD_2	I/O — — — I I	M/S	Tristate	—	45	M5
PK[6]	PCR[166]	AF0 AF1 AF2 AF3	GPIO[166] CAN2TX LIN2TX —	SIUL FlexCAN_2 LINFlexD_2 —	I/O O O —	M/S	Tristate	—	46	M6

4 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 5 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see MPC5646C Reference Manual.

Electrical Characteristics

- ² V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$. All values need to be confirmed during device validation.
- ³ Analog filters are available on all wakeup lines.
- ⁴ The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions ^{1,2}		Value			Unit
						Min	Typ	Max	
I _{WPU}	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}, V_{DD} = 5.0 \text{ V} \pm 10\%$	PAD3V5V = 0	10	—	150	μA
		C			PAD3V5V = 1 ³	10	—	250	
		P		$V_{IN} = V_{IL}, V_{DD} = 3.3 \text{ V} \pm 10\%$	PAD3V5V = 1	10	—	150	
I _{WPD}	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}, V_{DD} = 5.0 \text{ V} \pm 10\%$	PAD3V5V = 0	10	—	150	μA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}, V_{DD} = 3.3 \text{ V} \pm 10\%$	PAD3V5V = 1	10	—	150	

NOTES:

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified.

² V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$.

³ The configuration PAD3V5 = 1 when $V_{DD} = 5 \text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. SLOW configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ^{1,2}		Value			Unit
					Min	Typ	Max	
V _{OH}	CC	Output high level SLOW configuration	Push Pull	$I_{OH} = -3 \text{ mA}, V_{DD} = 5.0 \text{ V} \pm 10\%, \text{PAD3V5V} = 0$	$0.8V_{DD}$	—	—	V
				$I_{OH} = -3 \text{ mA}, V_{DD} = 5.0 \text{ V} \pm 10\%, \text{PAD3V5V} = 1^3$	$0.8V_{DD}$	—	—	
				$I_{OH} = -1.5 \text{ mA}, V_{DD} = 3.3 \text{ V} \pm 10\%, \text{PAD3V5V} = 1$	$V_{DD} - 0.8$	—	—	

Table 20. I/O consumption (continued)

Symbol		C	Parameter	Conditions ^{1,2}	Value ³			Unit
					Min	Typ	Max	
I _{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
				V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65 ⁴	

- NOTES:
- ¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.
 - ² V_{DD} as mentioned in the table is V_{DD_HV_A}/V_{DD_HV_B}.
 - ³ All values need to be confirmed during device validation.
 - ⁴ Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

4.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

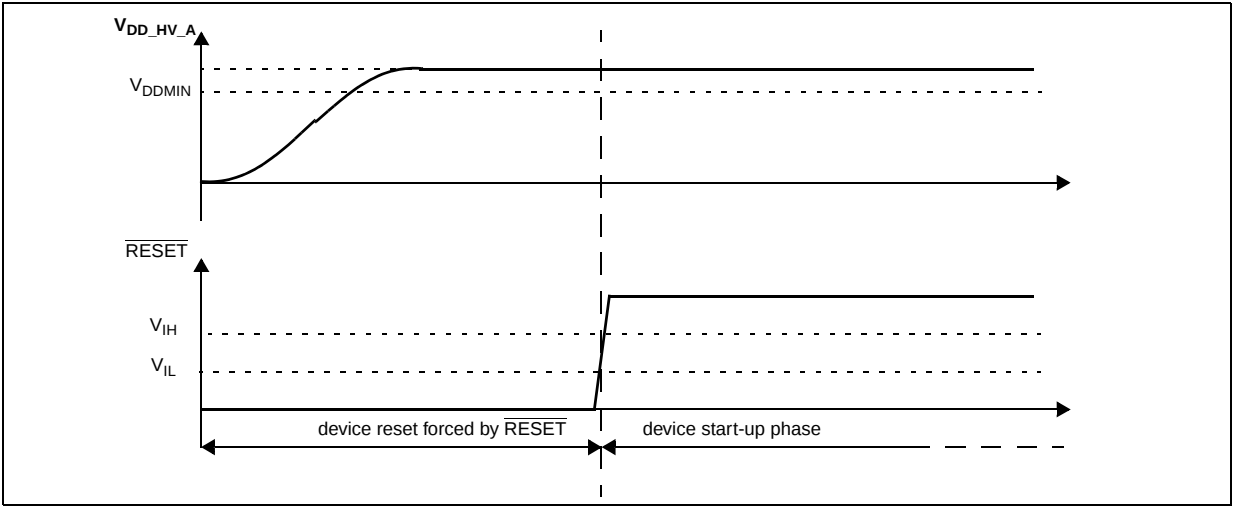


Figure 6. Start-up reset requirements

Table 22. Voltage regulator electrical characteristics (continued)

Symbol	C	D	Parameter	Conditions ¹	Value ²			Unit
					Min	Typ	Max	
I _{LPREGINT}	CC	D	Low power regulator module current consumption	I _{LPREG} = 15 mA; T _A = 55 °C	—	—	600	μA
		—		I _{LPREG} = 0 mA; T _A = 55 °C	—	20	—	
I _{VREGREF}	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T _A = 55 °C	—	2	—	μA
I _{VREDLVD12}	CC	D	Main LVD current consumption (switch-off during standby)	T _A = 55 °C	—	1	—	μA
I _{DD_HV_A}	CC	D	In-rush current on V _{DD_BV} during power-up	—	—	—	600 ³	mA

NOTES:

¹ V_{DD_HV_A} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

³ Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

4.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the V_{DD_HV_A} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD_HV_A} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD_HV_A} to ensure device is reset below minimum functional supply
- LVDHV5 monitors V_{DD_HV_A} when application uses device in the 5.0 V±10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

NOTE

When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

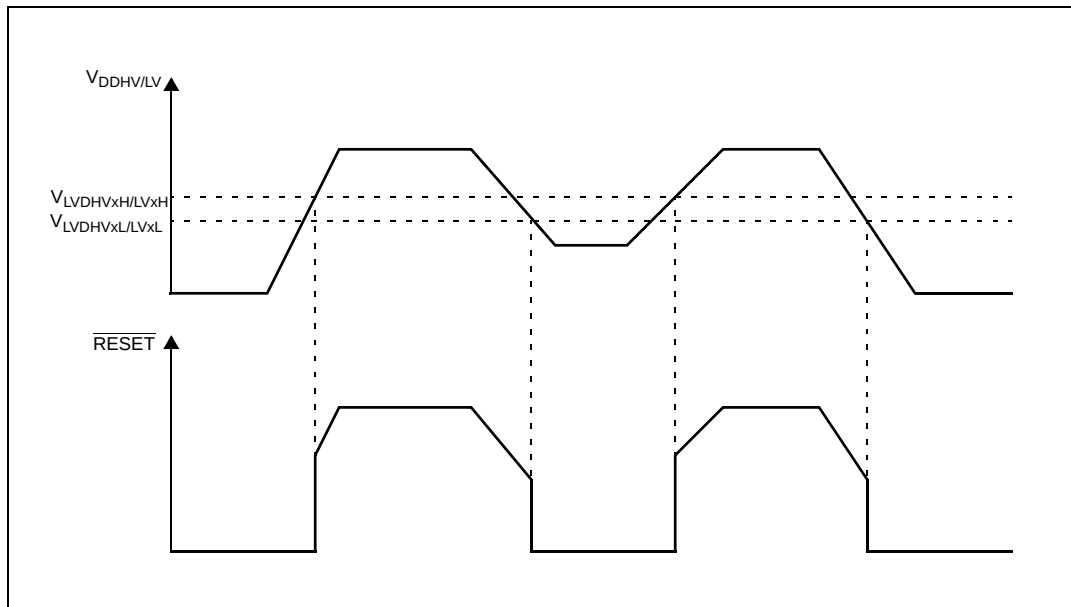


Figure 9. Low voltage monitor vs. Reset

Table 23. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value ²			Unit
				Min	Typ	Max	
V _{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5
V _{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6
V _{LVDHV3H}	CC	T	LVDHV3 low voltage detector high threshold	—	2.7	—	2.85
V _{LVDHV3L}	CC	T	LVDHV3 low voltage detector low threshold	—	2.6	—	2.74
V _{LVDHV5H}	CC	T	LVDHV5 low voltage detector high threshold	—	4.3	—	4.5
V _{LVDHV5L}	CC	T	LVDHV5 low voltage detector low threshold	—	4.2	—	4.4
V _{LVDLVCORL}	CC	P	LVDLVCOR low voltage detector low threshold	T _A = 25 °C, after trimming	1.12	1.145	1.17
V _{LVDLVBKPL}	CC	P	LVDLVBKP low voltage detector low threshold		1.12	1.145	1.17

NOTES:

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

4.9 Low voltage domain power consumption

Table 24 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 28. Flash memory read access timing¹

Symbol		C	Parameter	Conditions ²		Frequency range	Unit
				Code flash memory	Data flash memory		
f _{READ}	CC	P	Maximum frequency for Flash reading	5 wait states	13 wait states	120 —100	MHz
		C		4 wait states	11 wait states	100—80	
		D		3 wait states	9 wait states	80—64	
		C		2 wait states	7 wait states	64—40	
		C		1 wait states	4 wait states	40—20	
		C		0 wait states	2 wait states	20—0	

NOTES:

¹ Max speed is the maximum speed allowed including PLL frequency modulation (FM).

² V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

4.10.2 Flash memory power supply DC characteristics

Table 29 shows the flash memory power supply DC characteristics on external supply.

Table 29. Flash memory power supply DC electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value ²			Unit
				Min	Typ	Max	
I _{CFREAD} ⁽³⁾	CC	Sum of the current consumption on V _{DD_HV_A} on read access	Flash memory module read f _{CPU} = 120 MHz + 2% ⁽⁴⁾			33	mA
I _{DFREAD} ⁽³⁾						13	
I _{CFMOD} ⁽³⁾	CC	Sum of the current consumption on V _{DD_HV_A} (program/erase)	Program/Erase on-going while reading flash memory registers f _{CPU} = 120 MHz + 2% ⁽⁴⁾			52	mA
I _{DFMOD} ⁽³⁾						13	
I _{CFLPW} ⁽³⁾	CC	Sum of the current consumption on V _{DD_HV_A} during flash memory low power mode				1.1	mA
I _{CFPWD} ⁽³⁾	CC	Sum of the current consumption on V _{DD_HV_A} during flash memory power down mode				150	µA
I _{DFPWD} ⁽³⁾						150	

NOTES:

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol		C	Parameter	Conditions ¹	Value ²			Unit
					Min	Typ	Max	
V _{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	0.65V _{DD_HV_A}	—	V _{DD_HV_A} + 0.4	V
V _{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	−0.3	—	0.35V _{DD_HV_A}	V

- NOTES:
- ¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.
 - ² All values need to be confirmed during device validation.
 - ³ Based on ATE Cz
 - ⁴ Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

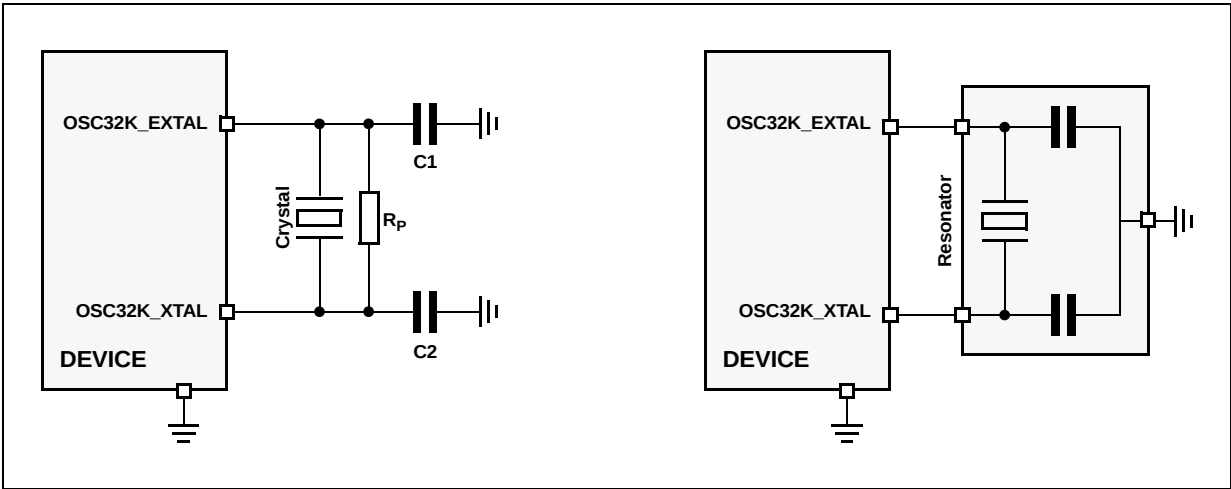


Figure 12. Crystal oscillator and resonator connection scheme

NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions ¹	Value ²			Unit
					Min	Typ	Max	
T _{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T _A = 25 °C, V _{DD} = 5.0 V ± 10%	—	8	12	μs
Δ _{SIRCPRE}	CC	C	Slow internal RC oscillator precision after software trimming of f _{SIRC}	T _A = 25 °C	−2	—	+2	%
Δ _{SIRCTRM}	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
Δ _{SIRCVAR}	CC	C	Variation in f _{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	−10	—	+10	%

NOTES:

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

³ This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

Table 48. On-chip peripherals current consumption¹

Symbol		C	Parameter	Conditions		Value ²	Unit
						Typ	
IDD_HV_ADC1	CC	D	ADC_1 supply current on V _{DD_HV_ADC1}	V _{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f _{periph}	μA
				V _{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
I _{DD_HV(FLASH)}	CC	D	CFlash + DFlash supply current on V _{DD_HV_ADC}	V _{DD} = 5.5 V	—	13.25	mA
I _{DD_HV(PLL)}	CC	D	PLL supply current on V _{DD_HV}	V _{DD} = 5.5 V	—	0.0031 × f _{periph}	

NOTES:

¹ Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.

² f_{periph} is in absolute value.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol			Unit
			Min	Max	
1	DSPI Cycle Time	t_{SCK}	Refer note ¹	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay ²	t_{CSC}	7	—	ns
3	After SCK Delay ³	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid) ⁴	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

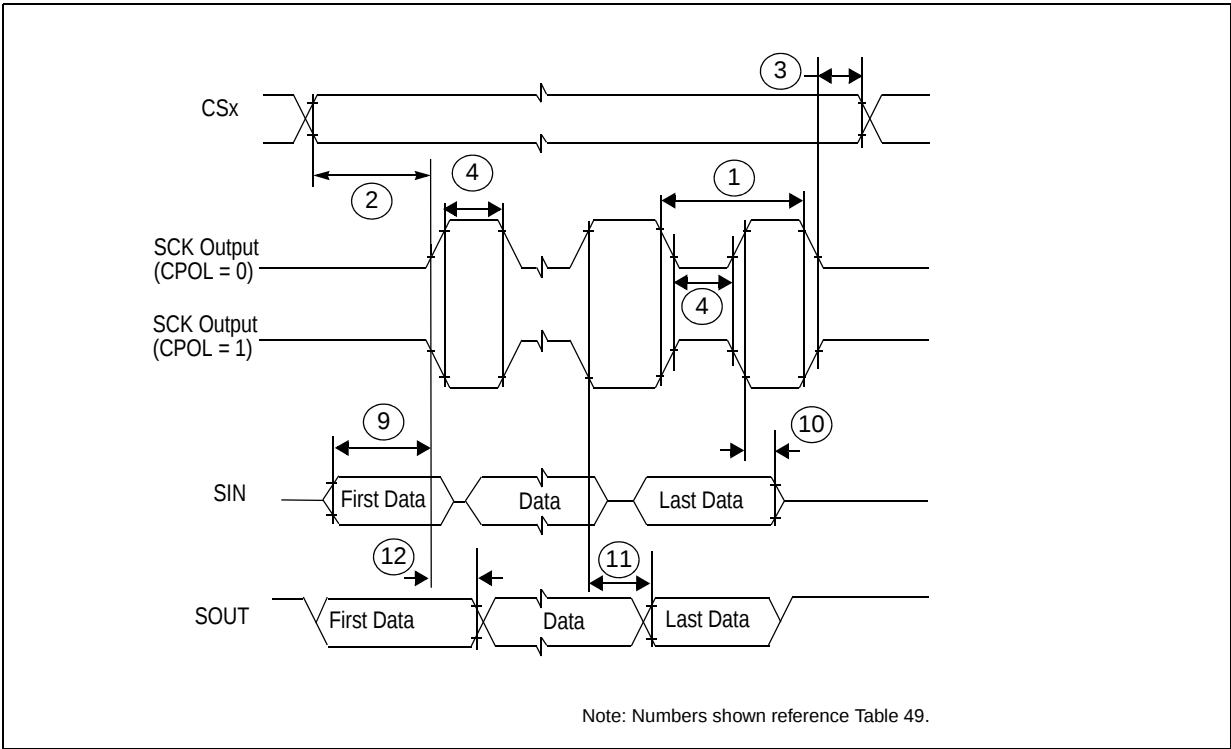
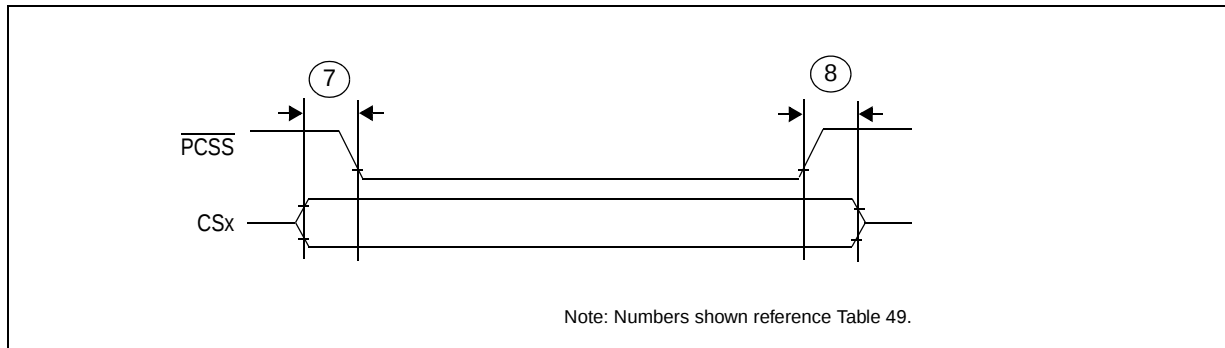


Figure 29. DSPI modified transfer format timing-master, CPHA = 0


Figure 33. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4.19.3 Nexus characteristics

Table 50. Nexus debug port timing¹

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time ²	t_{MCKC}	16.3	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVT0}}$ Data Valid ³	t_{MDOV}	−0.1	0.25	t_{MCKC}
4	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCKC}
5	$\overline{\text{EVT0}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCKC}
6	TCK Cycle Time ⁴	t_{TCKC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	$t_{\text{NTDIS}}, t_{\text{NTMSS}}$	8	—	ns
9	TDI, TMS Data Hold Time	$t_{\text{NTDIH}}, t_{\text{NTMSH}}$	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

NOTES:

¹ JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{\text{DDE}} = 4.0 - 5.5 \text{ V}$, $T_{\text{A}} = T_{\text{L}}$ to T_{H} , and $C_{\text{L}} = 30 \text{ pF}$ with $\text{SRC} = 0b11$.

² MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.

³ MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVT0}}$ data is held valid until next MCKO low cycle.

⁴ The system clock frequency needs to be three times faster than the TCK frequency.

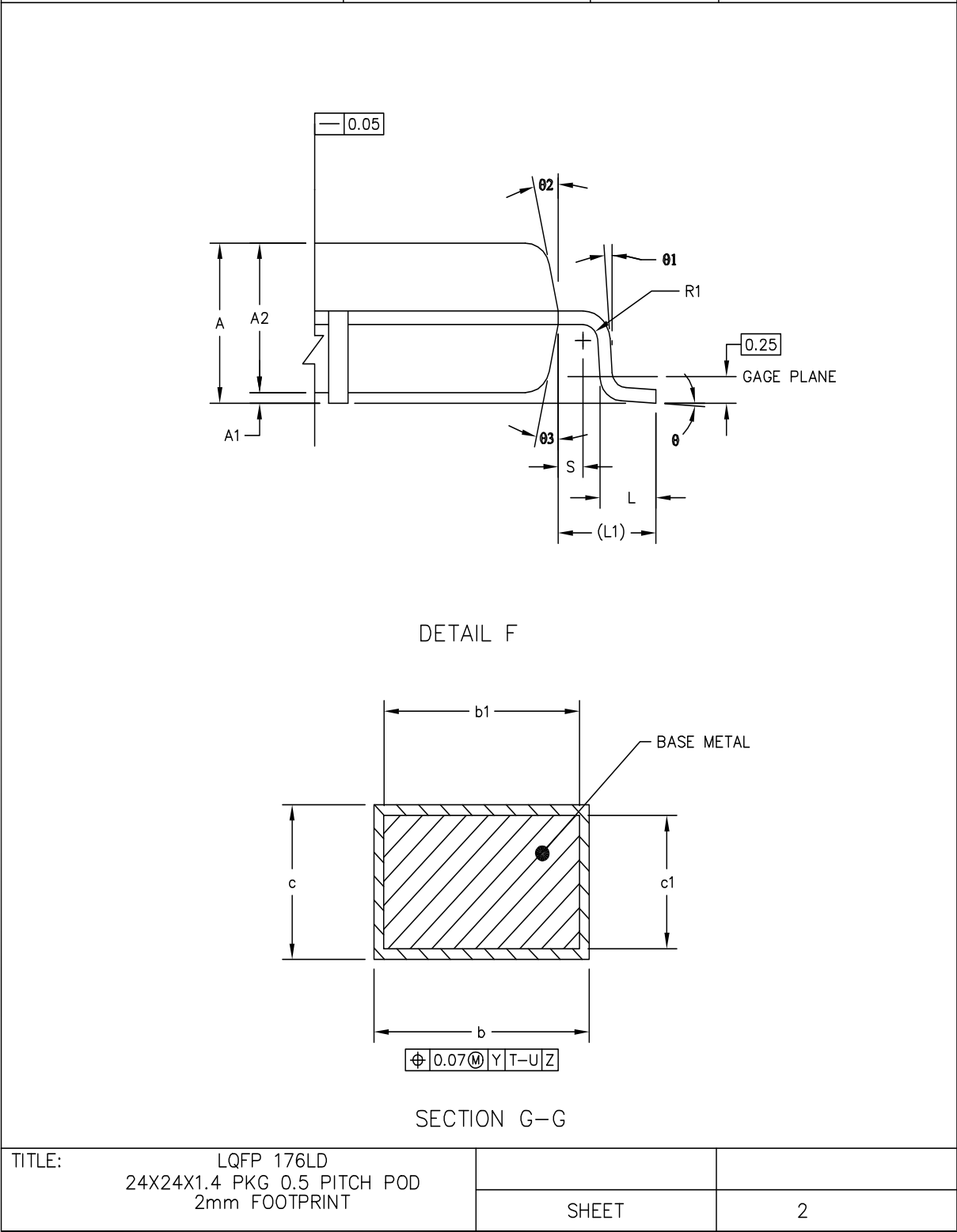


Figure 38. 176 LQFP mechanical drawing (Part 2 of 3)