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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 46x10b, 24x12b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5645bf0mlu1

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Other Features

- System clocks sources
  - 4–40 MHz external crystal oscillator
  - 16 MHz internal RC oscillator
  - FMPLL
  - Additionally, there are two low power oscillators: 128 kHz internal RC oscillator, 32 kHz external crystal oscillator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillators or external 4–40 MHz crystal
  - Supports autonomous wake-up with 1 ms resolution with max timeout of 2 seconds
  - Optional support from external 32 kHz crystal oscillator, supporting wake-up with 1 second resolution and max timeout of 1 hour
- 1 Real Time Interrupt (RTI) with 32-bit counter resolution
- 1 Safety Enhanced Software Watchdog Timer (SWT) that supports keyed functionality
- 1 dual-channel FlexRay Controller with 128 message buffers
- 1 Fast Ethernet Controller (FEC)
- On-chip voltage regulator (VREG)
- Cryptographic Services Engine (CSE)
- Offered in the following standard package types:
  - 176-pin LQFP, 24 × 24 mm, 0.5 mm Lead Pitch
  - 208-pin LQFP, 28 × 28 mm, 0.5 mm Lead Pitch
  - 256-ball MAPBGA, 17 × 17mm, 1.0 mm Lead Pitch

Table 1. MPC5646C family comparison[1] (continued)

Feature	MPC5644B		MPC5644C			MPC5645B		MPC5645C			MPC5646B		MPC5646C		
Package	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO[12]	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

NOTES:
1 Feature set dependent on selected peripheral multiplexing; table shows example.
2 Based on 125 °C ambient operating temperature and subject to full device characterisation.
3 The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4 DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5 Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6 There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7 16x precision channels (ANP) and 3x standard (ANS).
8 Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9 As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10 CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11 STCU controls MBIST activation and reporting.
12 Estimated I/O count for proposed packages based on multiplexing with peripherals.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]									PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]									PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]			VSS_LV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTRL	VDD_LV	PG[9]			VSS_LV	VSS_LV	VSS_HV	VSS_HV			PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]			VSS_LV	VSS_LV	VSS_LV	VDD_LV			PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]									PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]									PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3
PF[14]	PCR[94]	AF0 AF1 AF2 AF3 ALT4	GPIO[94] CAN4TX E1UC[27] CAN1TX MDIO	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1 FEC	I/O O I/O O I/O	M/S	Tristate	126	150	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — — —	GPIO[95] E1UC[4] — — RX_DV CAN1RX CAN4RX EIRQ[13]	SIUL eMIOS_1 — — FEC FlexCAN_1 FlexCAN_4 SIUL	I/O I/O — — I I I I	M/S	Tristate	125	149	D15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3 ALT4	GPIO[96] CAN5TX E1UC[23] — MDC	SIUL FlexCAN_5 eMIOS_1 — FEC	I/O O I/O — O	F	Tristate	122	146	E13
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — — —	GPIO[97] — E1UC[24] — TX_CLK CAN5RX EIRQ[14]	SIUL — eMIOS_1 — FEC FlexCAN_5 SIUL	I/O — I/O — I I I	M	Tristate	121	145	E14
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M/S	Tristate	16	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	15	15	E1
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M/S	Tristate	14	14	F2

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PL[10]	PCR[186]	AF0 AF1 AF2 AF3	GPIO[186] — MCKO —	SIUL — Nexus —	I/O — O —	F/S	Tristate	—	—	M11
PL[11]	PCR[187]	AF0 AF1 AF2 AF3	GPIO[187] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	M12
PL[12]	PCR[188]	AF0 AF1 AF2 AF3	GPIO[188] — EVTO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F11
PL[13]	PCR[189]	AF0 AF1 AF2 AF3	GPIO[189] — MDO6 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F10
PL[14]	PCR[190]	AF0 AF1 AF2 AF3	GPIO[190] — MDO7 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E12
PL[15]	PCR[191]	AF0 AF1 AF2 AF3	GPIO[191] — MDO8 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E11
PM[0]	PCR[192]	AF0 AF1 AF2 AF3	GPIO[192] — MDO9 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E10
PM[1]	PCR[193]	AF0 AF1 AF2 AF3	GPIO[193] — MDO10 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E9
PM[2]	PCR[194]	AF0 AF1 AF2 AF3	GPIO[194] — MDO11 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F12
PM[3]	PCR[195]	AF0 AF1 AF2 AF3	GPIO[195] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	K12

2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3 Analog filters are available on all wakeup lines.
4 The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

Table 15. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 16. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 38. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle(3)	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4 f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	100	nA
		D		T_A = 55 °C	—	—	200	nA
		D		T_A = 125 °C	—	—	1	µA

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

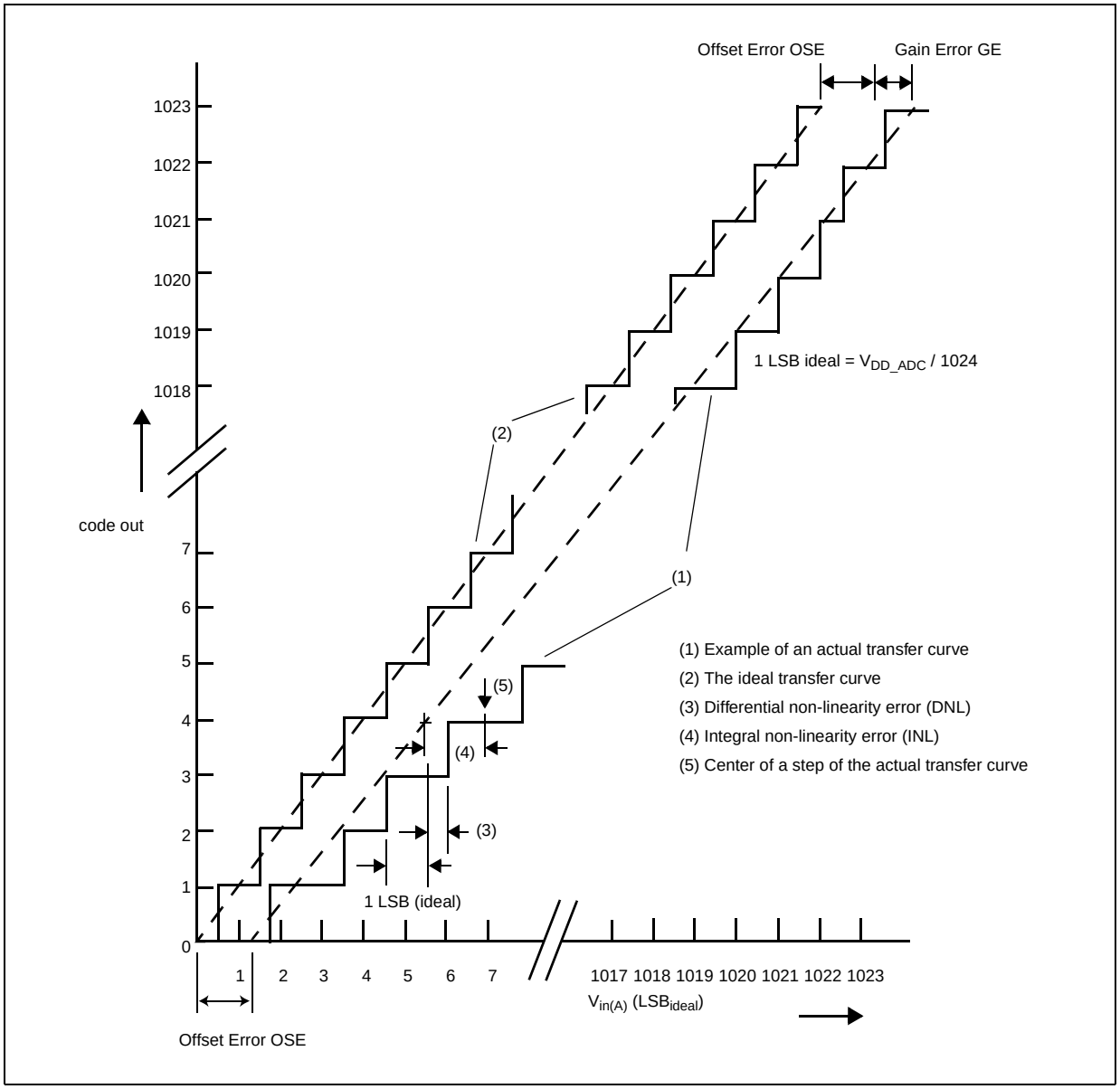


Figure 15. ADC_0 characteristic and error definitions

4.17.1.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device, can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source. A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

Table 43. Conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1		0.1	V
V_{DD_ADC1}[3]	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1		$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}[3,4]	SR	—	Analog input voltage[5]	—	V_{SS_ADC1} – 0.1		V_{DD_ADC1} + 0.1	V
f_{ADC1}	SR	—	ADC_1 analog frequency	—	8 + 2%		32 + 2%	MHz
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	1.5			µs
t_{ADC1_S}	CC	T	Sample time[6] VDD=5.0 V	—	440			ns
			Sample time(6) VDD=3.3 V	—	530			
t_{ADC1_C}	CC	P	Conversion time[7, 8] VDD=5.0 V	f_{ADC1} = 32 MHz	2			µs
			Conversion time(7), (6) VDD =5.0 V	$f_{ADC\ 1}$= 30 MHz	2.1			
			Conversion time(7), (6) VDD=3.3 V	$f_{ADC\ 1}$= 20 MHz	3			
			Conversion time(7), (6) VDD =3.3 V	f_{ADC1} = 15 MHz	3.01			
C_S	CC	D	ADC_1 input sampling capacitance	—	5			pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	3			pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	1			pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	1.5			pF
R_{SW1}	CC	D	Internal resistance of analog source	—			1	kΩ

7 Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.

8 Refer to ADC conversion table for detailed calculations.

9 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

Table 44. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

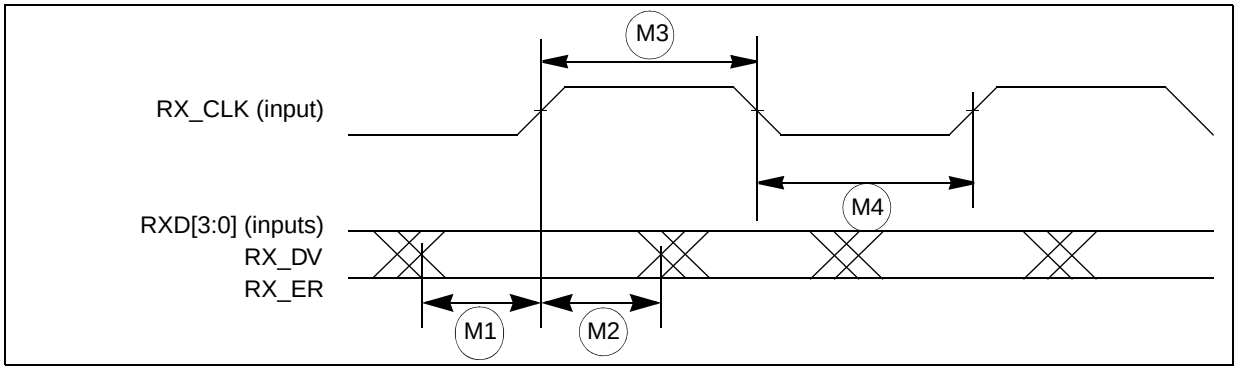


Figure 21. MII receive signal timing diagram

4.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

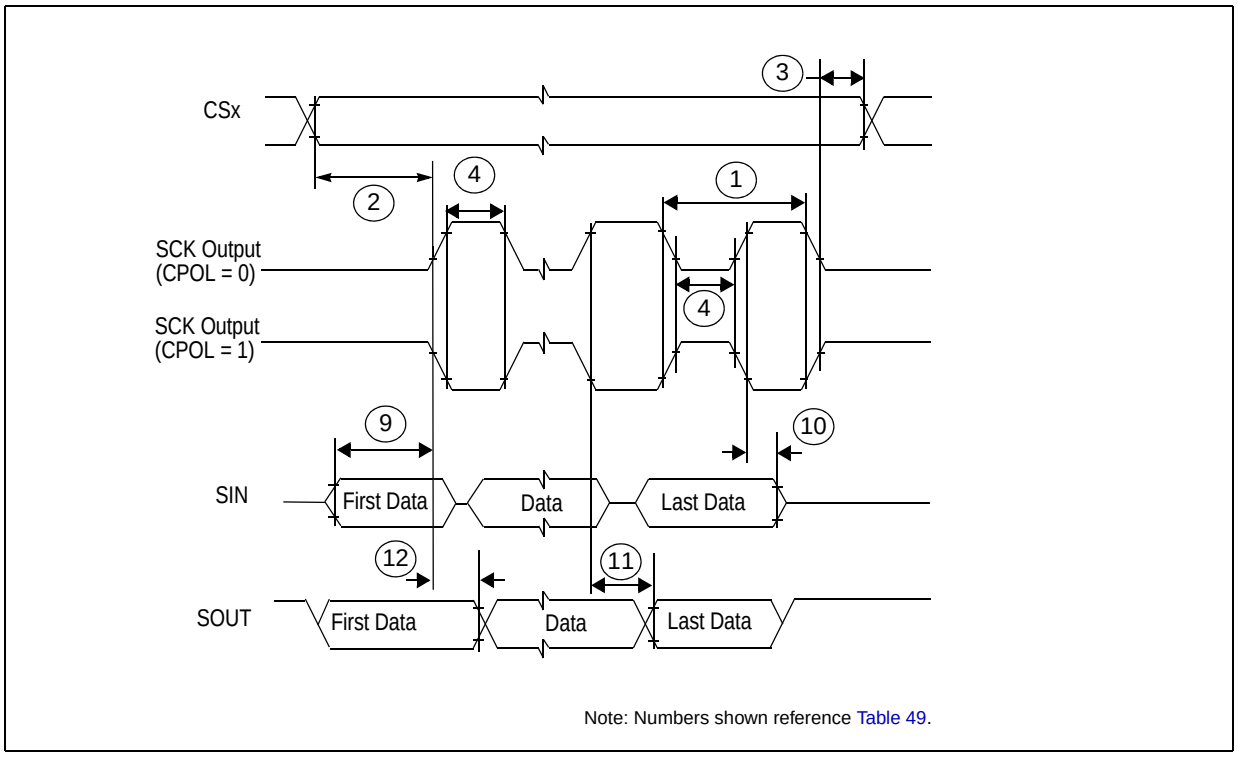


Figure 29. DSPI modified transfer format timing–master, CPHA = 0

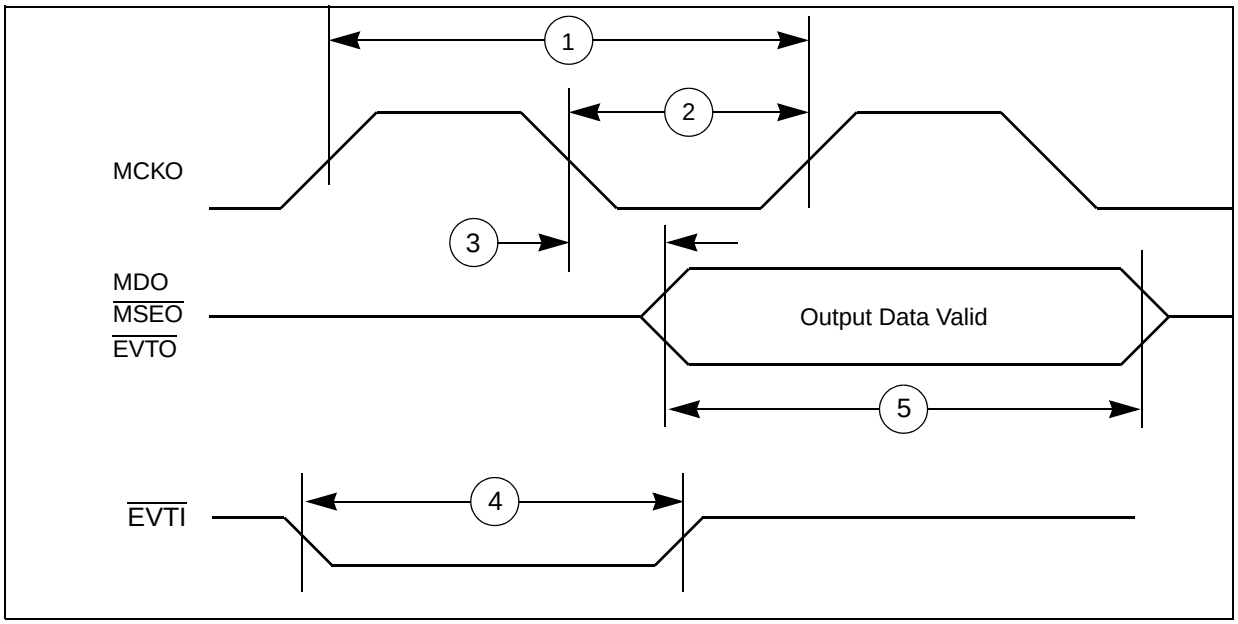
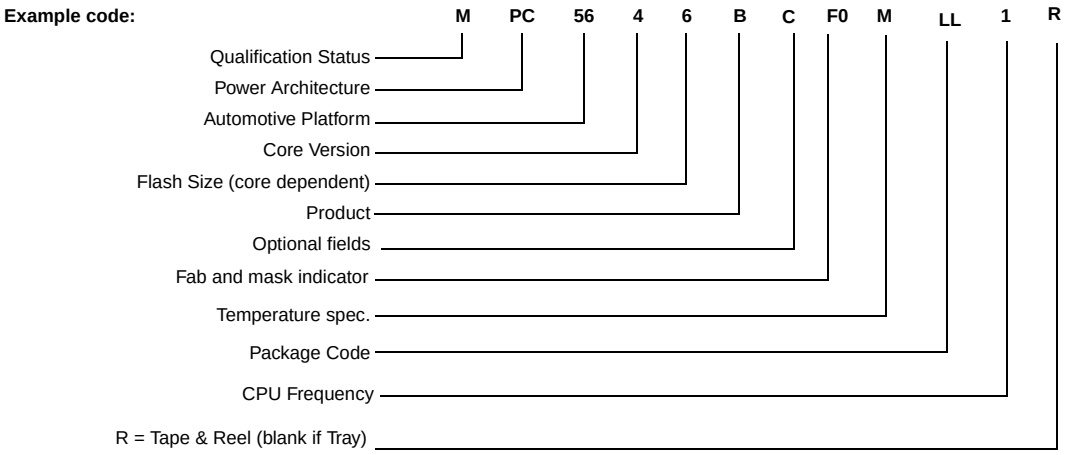


Figure 34. Nexus output timing

6 Ordering information



Qualification Status
M = MC status
S = Auto qualified
P = PC status

PC = Power Architecture

Automotive Platform
56 = Power Architecture in 90 nm

Core Version
4 = e200z4d core version (highest core version in the case of multiple cores)

Flash Memory Size
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

Product Version
B = Body
C = Gateway

Optional fields
C = CSE module available
Blank = none of these options available

Fab and mask version indicator
F = ATMC
0 = First version of the mask

Temperature spec.
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C

Package Code
LU = 176 LQFP
LT = 208 LQFP
MJ = 256 MAPBGA

CPU Frequency
1 = e200z4d operates up to 120 MHz
8 = e200z4d operates up to 80 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Note: Not all options are available on all devices. Refer to Table 1, which shows the orderable part numbers for MPC564xx.

Figure 45. Orderable parts

Table 52. Revision history (continued)

Revision	Date	Changes
3	28 April 2011	• Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics • Updated Crystal oscillator and resonator connection scheme figure • Specified NPN transistor as the recommended BCP68 transistor throughout the document • Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} • Revised the footnotes in the “Functional port pin descriptions” table. • In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. • Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] • ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. • Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classification from “C” to “D”. • Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. • Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. • Functional port pin description: Added a footnote at the PB [9] port pin. • Absolute maximum ratings table: Added footnote 1. • Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. • Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. • FMPLL electrical characteristics table: Updated Δt_{LTJIT}. • Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. • MII serial management channel timing table: Updated M12 • JTAG characteristics table: Updated t_{TDOV}. • Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. • DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. • IO consumption table: Updated all parameter values. • DSPI electricals: Updated Δt_{CSC} max to 115 ns. • Low voltage power domain electrical characteristics table: Added footnote 9. • ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.

Table 52. Revision history (continued)

Revision	Date	Changes
5	21 June 2012	• Updated the pins 23 and 24 of Figure 2.176-pin LQFP configuration • Updated unit of measure in Table 43 Conversion characteristics (12-bit ADC_1) • Modified the value to typical value in Table 48 On-chip peripherals current consumption • Added footnote to t_{ESRT} parameter in Table 25 Code flash memory—Program and erase specifications • Added footnote to t_{ESRT} parameter in Table 26 Data flash memory—Program and erase specifications • Updated Table 28 Flash memory read access timing. • Updated Notes 2 and Notes 3 of Table 9 Recommended operating conditions (3.3 V) and Table 10 Recommended operating conditions (5.0 V) respectively. • Updated the footnote1 of Table 9 Recommended operating conditions (3.3 V) and Table 10 Recommended operating conditions (5.0 V) • Updated $V_{DD\_HV\_A}$ to V_{DD_BV} for C_{DEC2} and $I_{DD\_HV\_A}$ in Table 22 Voltage regulator electrical characteristics and deleted footnote3 • Updated the dedicated number of channels for 12-bit ADC in family comparison tables • Updated the values of $f_{SIRC,}$ parameters and conditions of $\Delta_{SIRCVAR}$ in Table 40 Slow internal RC oscillator (128 kHz) electrical characteristics • Updated second footnote in Table 10, Recommended operating conditions (5.0 V) • Updated the value of t_{ADC0_PU} in Table 42, ADC conversion characteristics (10-bit ADC_0) • Updated the IDD values in Table 24, Low voltage power domain electrical characteristics • Added footnote to Table 24, Low voltage power domain electrical characteristics related to current drawn from $V_{DD\_HV\_A}$ and $V_{DD\_HV\_B}$ • Updated entire Section 4.17.1.1, ”Input impedance and ADC accuracy”- Updated the values of VLPREG in Table 22, Voltage regulator electrical characteristics. • Updated the values of V_{LPREG} in Table 22, Voltage regulator electrical characteristics. • Added T_A = 25 °C, min and max values of V_{MREG} in Table 22, Voltage regulator electrical characteristics • Added T_A = 25 °C, min and max values of V_{LPREG} in Table 22, Voltage regulator electrical characteristics • Updated the min, max and typical values of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in Table 23, Low voltage monitor electrical characteristics • Updated values of gmFXOSC in Table 35, Fast external crystal oscillator (4 to 40 MHz) electrical characteristicsUpdated values of gmSXOSC in Table 37, Slow external crystal oscillator (32 kHz) electrical characteristics • Updated the footnote 5 for T_{ADC0_C} in Table 42, ADC conversion characteristics (10-bit ADC_0) • Updated the footnotes of Table 24, Low voltage power domain electrical characteristics
5.1	15 Aug 2012	• Removed Footer: Preliminary tag