What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5645bf0vlt1r

1 Introduction

1.1 Document Overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the MPC5646C device. To ensure a complete understanding of the device functionality, refer also to the MPC5646C Reference Manual.

1.2 Description

The MPC5646C is a new family of next generation microcontrollers built on the Power Architecture embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5646C family expands the range of the MPC560xB microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the MPC5646C automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UISA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 2 summarizes the functions of the blocks present on the MPC5646C.

Table 2. MPC5646C series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Cryptographic Security Engine (CSE)	Supports the encoding and decoding of any kind of data
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width
DMA Channel Multiplexer (DMAMUX)	Allows to route DMA sources (called slots) to DMA channels
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Fast Ethernet Controller (FEC)	Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks
Internal multiplexer (IMUX) SIUL subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^{2}C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^{2}C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	S	Tristate	97	117	M13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	101	123	L14
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	103	125	L15
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/S	Input, weak pull-up	154	178	B10
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/M	Tristate	149	173	D9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/S	Tristate	145	169	B11

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[46] E0UC[14] SCK_2 — FR_DBG[2] EIRQ[8]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	3	3	B2
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 ALT4	GPIO[47] E0UC[15] CS0_2 — FR_DBG[3] EIRQ[20]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	4	4	A1
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPI[48] — — — ADC0_P[4] ADC1_P[4] WKPU[27]	SIUL — — — ADC_0 ADC_1 WKPU	I — — — I I I	I	Tristate	77	93	R12

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3
PF[14]	PCR[94]	AF0 AF1 AF2 AF3 ALT4	GPIO[94] CAN4TX E1UC[27] CAN1TX MDIO	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1 FEC	I/O O I/O O I/O	M/S	Tristate	126	150	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — — —	GPIO[95] E1UC[4] — — RX_DV CAN1RX CAN4RX EIRQ[13]	SIUL eMIOS_1 — — FEC FlexCAN_1 FlexCAN_4 SIUL	I/O I/O — — I I I I	M/S	Tristate	125	149	D15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3 ALT4	GPIO[96] CAN5TX E1UC[23] — MDC	SIUL FlexCAN_5 eMIOS_1 — FEC	I/O O I/O — O	F	Tristate	122	146	E13
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — — —	GPIO[97] — E1UC[24] — TX_CLK CAN5RX EIRQ[14]	SIUL — eMIOS_1 — FEC FlexCAN_5 SIUL	I/O — I/O — I I I	M	Tristate	121	145	E14
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M/S	Tristate	16	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	15	15	E1
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M/S	Tristate	14	14	F2

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKPU[18] SIN_3	SIUL eMIOS_1 — — WKPU DSPI_3	I/O I/O — — I I	S	Tristate	13	13	D1
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX —	SIUL eMIOS_1 LINFlexD_6 —	I/O I/O O —	M/S	Tristate	38	38	M1
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] — LIN6RX WKPU[20]	SIUL eMIOS_1 eMIOS_1 — LINFlexD_6 WKPU	I/O I/O I/O — I I	S	Tristate	37	37	L2
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15]	SIUL eMIOS_1 LINFlexD_7 DSPI_2 SIUL	I/O I/O O I/O I	S	Tristate	34	34	K3
PG[9]	PCR[105]	AF0 AF1 AF2 AF3 — —	GPIO[105] E1UC[18] — SCK_2 LIN7RX WKPU[21]	SIUL eMIOS_1 — DSPI_2 LINFlexD_7 WKPU	I/O I/O — I/O I I	S	Tristate	33	33	J4
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	138	162	B13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 CS0_6	SIUL eMIOS_0 DSPI_4 DSPI_6	I/O I/O I/O I/O	M/S	Tristate	139	163	A16
PG[12]	PCR[108]	AF0 AF1 AF2 AF3 ALT4	GPIO[108] E0UC[26] SOUT_4 — TXD[2]	SIUL eMIOS_0 DSPI_4 — FEC	I/O I/O O — O	M/S	Tristate	116	140	F15

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PM[4]	PCR[196]	AF0 AF1 AF2 AF3	GPIO[196] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	L12
PM[5]	PCR[197]	AF0 AF1 AF2 AF3	GPIO[197] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F9
PM[6]	PCR[198]	AF0 AF1 AF2 AF3	GPIO[198] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F6

NOTES:

[1] Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 000 → AF0; PCR.PA = 001 → AF1; PCR.PA = 010 → AF2; PCR.PA = 011 → AF3; PCR.PA = 100 → ALT4. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to ‘1’, regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as “—”.

[2] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[3] NMI[0] and NMI[1] have a higher priority than alternate functions. When NMI is selected, the PCR.PA field is ignored.

[4] SXOSC’s OSC32k_XTAL and OSC32k_EXTAL pins are shared with GPIO functionality. When used as crystal pins, other functionality of the pin cannot be used and it should be ensured that application never programs OBE and PUE bit of the corresponding PCR to "1".

[5] If you want to use OSC32K functionality through PB[8] and PB[9], you must ensure that PB[10] is static in nature as PB[10] can induce coupling on PB[9] and disturb oscillator frequency.

[6] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

[7] When MBIST is enabled to run (STCU Enable = 1), the application must not drive or tie PAD[178) (MDO[0]) to 0 V before the device exits reset (external reset is removed) as the pad is internally driven to 1 to indicate MBIST operation. When MBIST is not enabled (STCU Enable = 0), there are no restriction as the device does not internally drive the pad.

[8] These pins can be configured as Nexus pins during reset by the debugger writing to the Nexus Development Interface "Port Control Register" rather than the SIUL. Specifically, the debugger can enable the MDO[7:0], MSEO, and MCKO ports by programming NDI (PCR[MCKO_EN] or PCR[PSTAT_EN]). MDO[8:11] ports can be enabled by programming NDI ((PCR[MCKO_EN] and PCR[FPM]) or PCR[PSTAT_EN]).

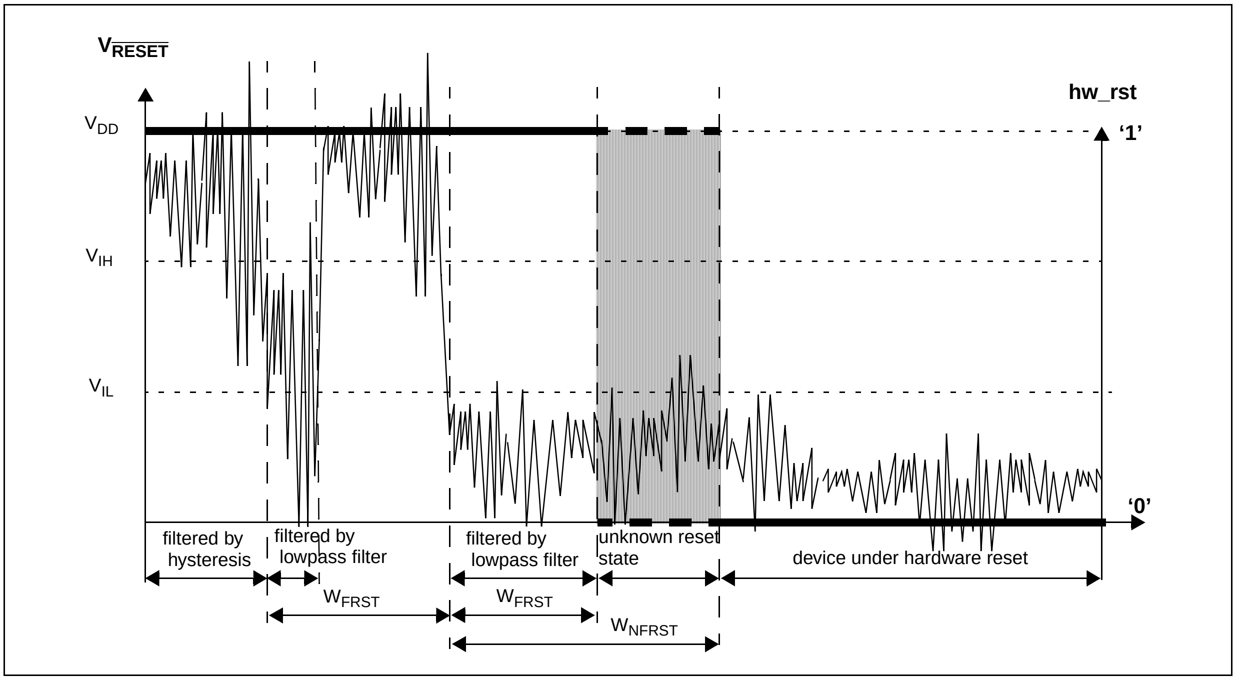


Figure 7. Noise filtering on reset signal

Table 21. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	−0.3	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 22. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600[3]	mA

NOTES:

[1] $V_{DD\_HV\_A}$ = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

[3] Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

4.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

NOTE

When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

Table 38. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle(3)	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

NOTES:

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

[2] All values need to be confirmed during device validation.

[3] PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

[4] f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3,]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	100	nA
		D		T_A = 55 °C	—	—	200	nA
		D		T_A = 125 °C	—	—	1	µA

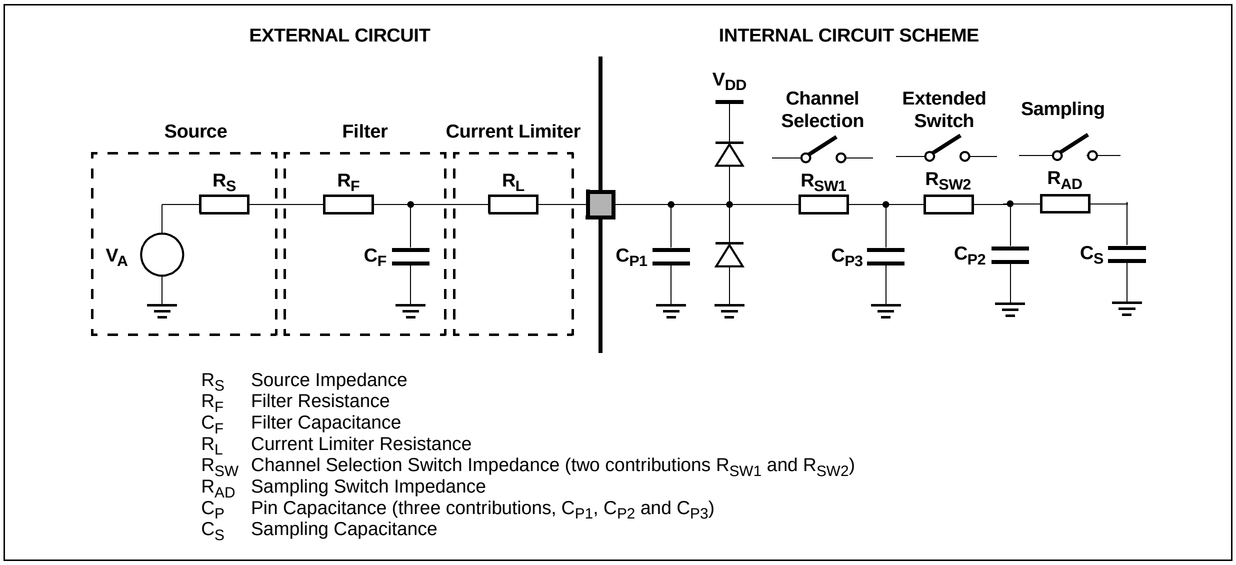


Figure 17. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 16): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

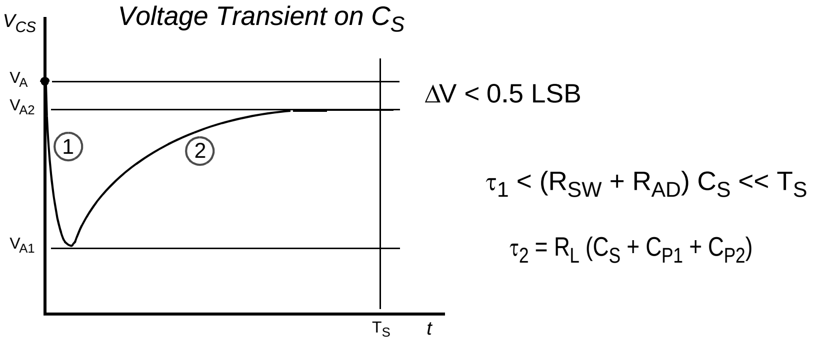


Figure 18. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

[7] Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.

[8] Refer to ADC conversion table for detailed calculations.

[9] Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

Table 44. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

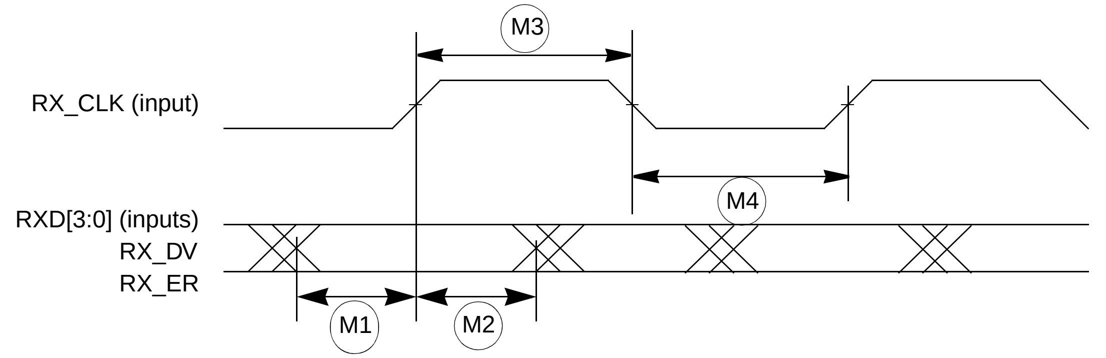


Figure 21. MII receive signal timing diagram

4.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

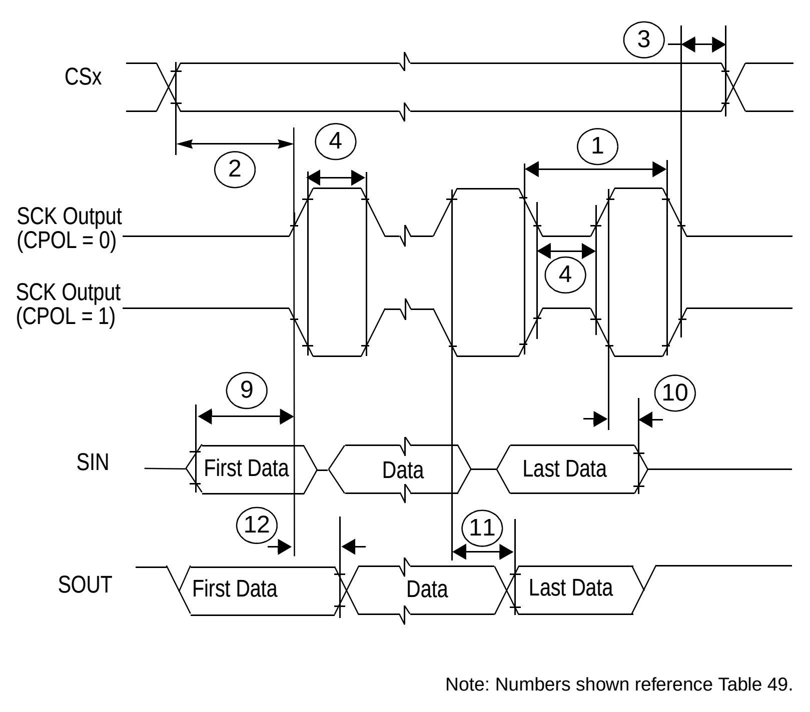


Figure 29. DSPI modified transfer format timing–master, CPHA = 0

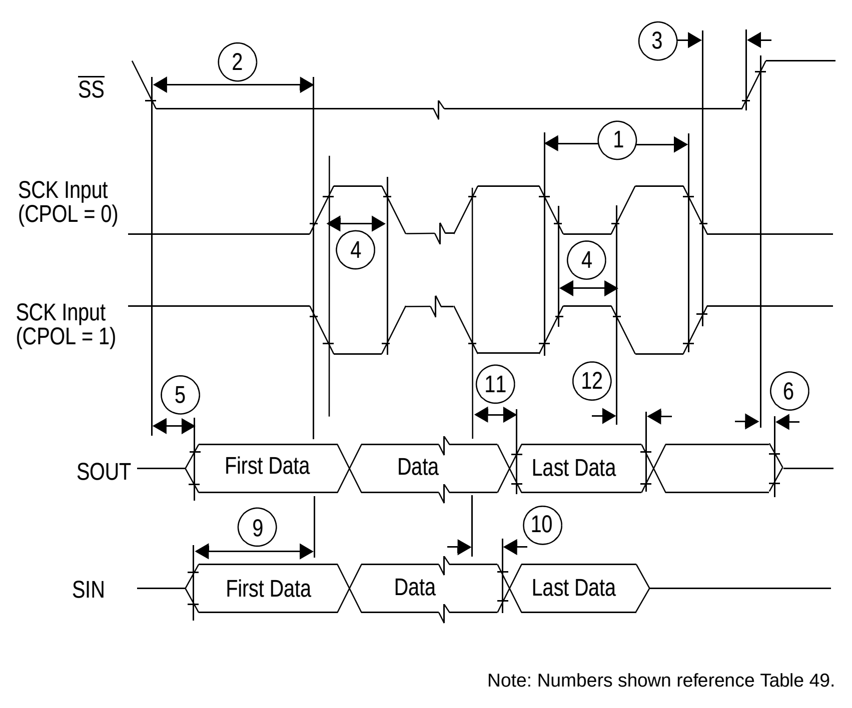


Figure 31. DSPI modified transfer format timing–slave, CPHA = 0

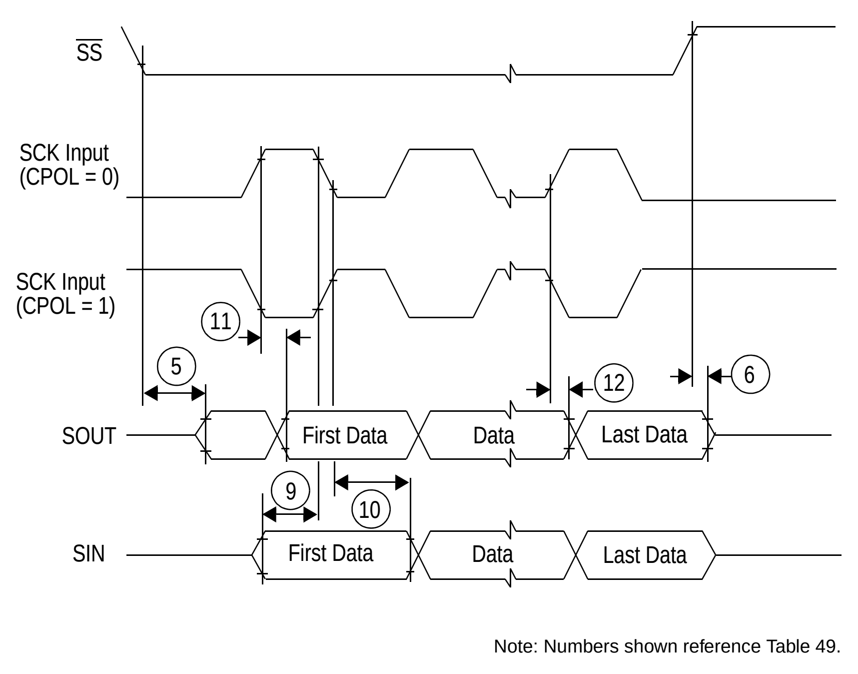
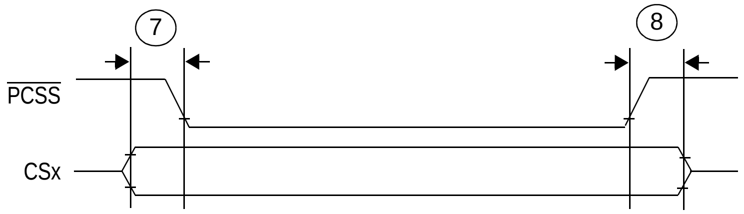


Figure 32. DSPI modified transfer format timing–slave, CPHA = 1



Note: Numbers shown reference Table 49.

Figure 33. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4.19.3 Nexus characteristics

Table 50. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time[2]	t_{MCYC}	16.3	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[3]	t_{MDOV}	–0.1	0.25	t_{MCYC}
4	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
5	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
6	TCK Cycle Time[4]	t_{TCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
9	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

NOTES:

[1] JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DDE} = 4.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

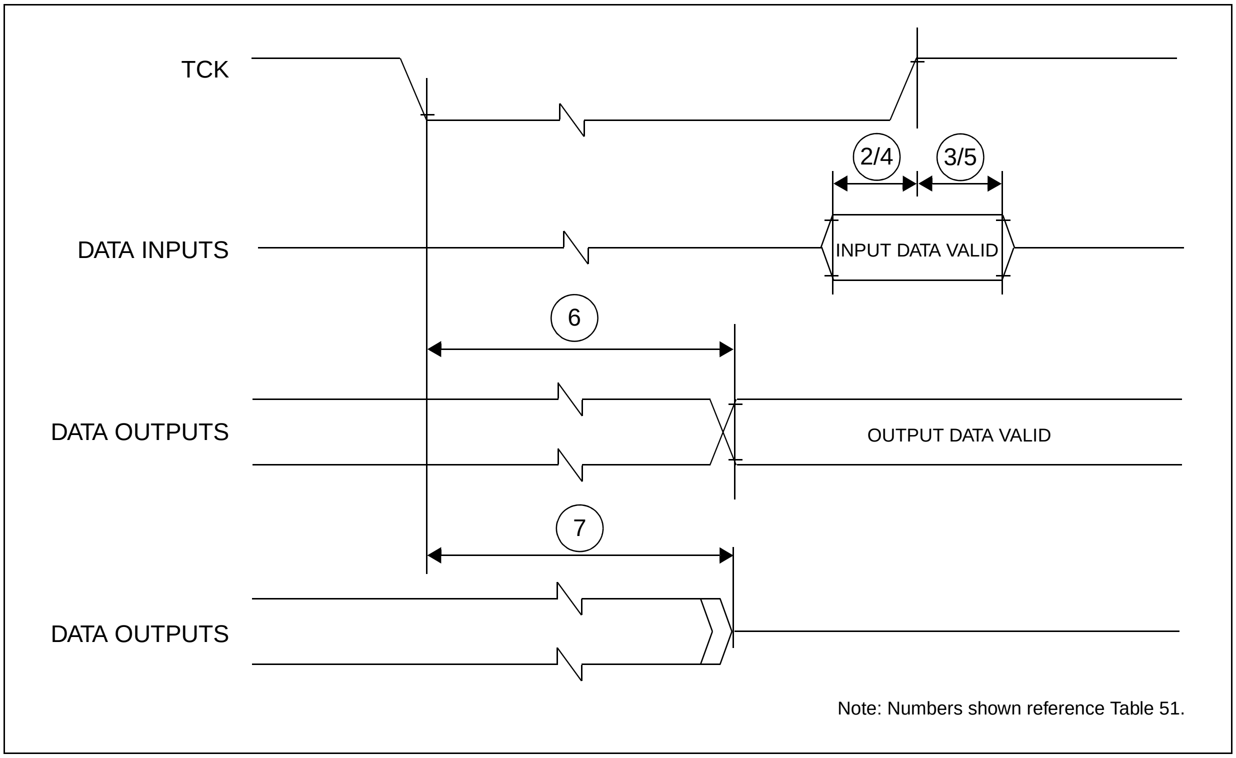
[2] MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.

[3] MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

[4] The system clock frequency needs to be three times faster than the TCK frequency.

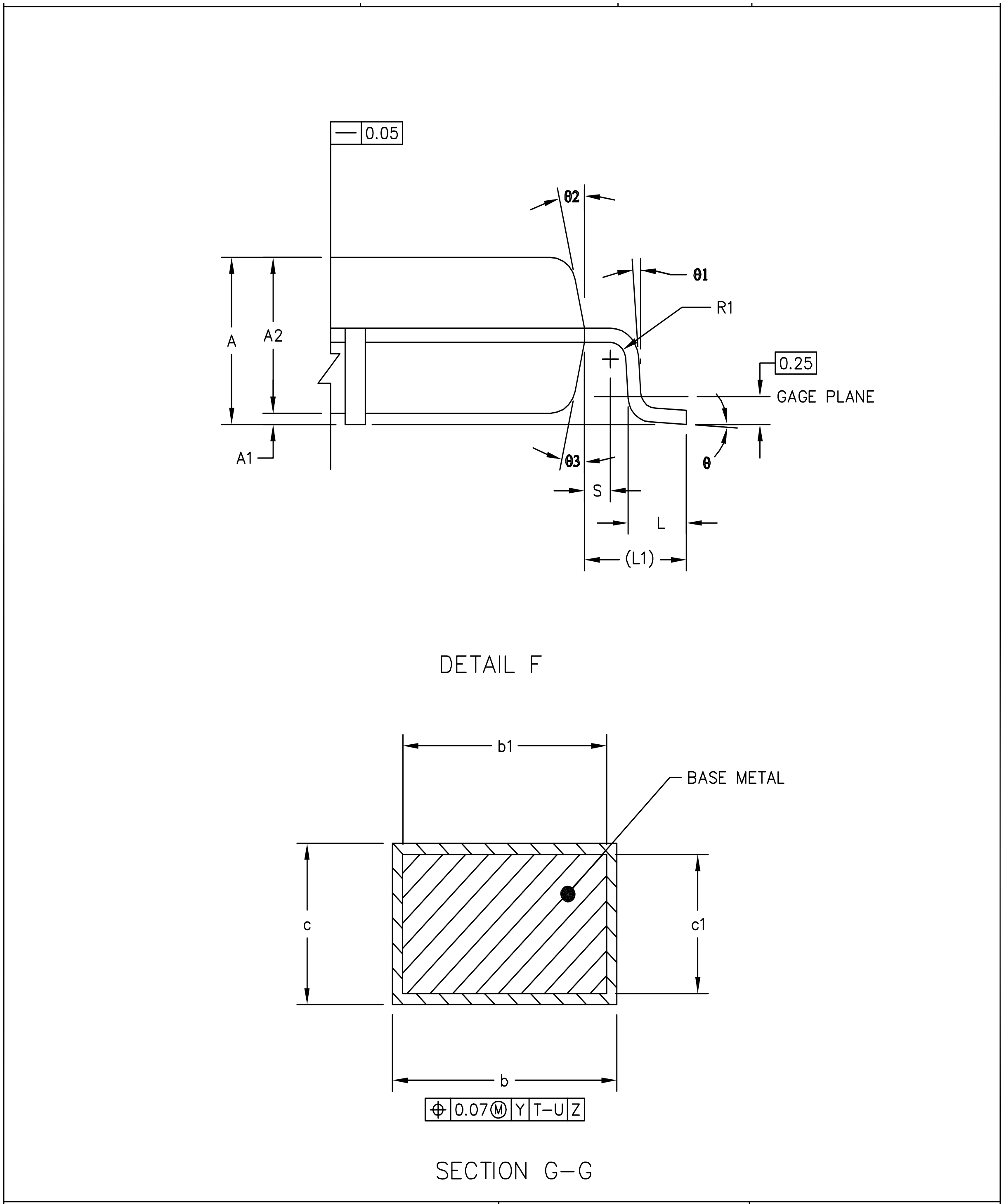
Table 51. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns



Note: Numbers shown reference Table 51.

Figure 36. Timing diagram - JTAG boundary scan



TITLE: LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	2

Figure 38. 176 LQFP mechanical drawing (Part 2 of 3)

NOTES

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS IN MILLIMETERS.

3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.

△4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM T.

△5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS INCLUDE MOLD MISMATCH.

△6. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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TITLE: 208 LD TQFP, 28 X 28 PKG, 0.50 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23458W	REV: C
	CASE NUMBER: 998-01	20 MAY 2005
	STANDARD: JEDEC MS-026 BJB	

Figure 42. 208 LQFP mechanical drawing (Part 3 of 3)

Appendix A Abbreviations

Table 53 lists abbreviations used but not defined elsewhere in this document.

Table 53. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select