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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646bcf0vlu8

Table of Contents

1 Introduction

1.1 Document Overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the MPC5646C device. To ensure a complete understanding of the device functionality, refer also to the MPC5646C Reference Manual.

1.2 Description

The MPC5646C is a new family of next generation microcontrollers built on the Power Architecture embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5646C family expands the range of the MPC560xB microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the MPC5646C automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UISA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5646C family comparison[1]

Feature	MPC5644B		MPC5644C			MPC5645B		MPC5645C			MPC5646B		MPC5646C		
Package	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA
CPU	e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed[2]	Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]		
Code flash memory	1.5 MB					2 MB					3 MB				
Data flash memory	4 x16 KB														
SRAM	128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU	16-entry														
eDMA[4]	32 ch														
10-bit ADC															
dedicated[5,6]	27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch	
shared with 12-bit ADC[7]	19 ch														
12-bit ADC															
dedicated[8]	5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch	
shared with 10-bit ADC[7]	19 ch														
CTU	64 ch														
Total timer I/O[9] eMIOS	64 ch, 16-bit														
SCI (LINFlexD)	10														
SPI (DSPI)	8														
CAN (FlexCAN)[10]	6														
FlexRay	Yes														
STCU[11]	Yes														

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[46] E0UC[14] SCK_2 — FR_DBG[2] EIRQ[8]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	3	3	B2
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 ALT4	GPIO[47] E0UC[15] CS0_2 — FR_DBG[3] EIRQ[20]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	4	4	A1
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPI[48] — — — ADC0_P[4] ADC1_P[4] WKPU[27]	SIUL — — — ADC_0 ADC_1 WKPU	I — — — I I I	I	Tristate	77	93	R12

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PG[13]	PCR[109]	AF0 AF1 AF2 AF3 ALT4	GPIO[109] E0UC[27] SCK_4 — TXD[3]	SIUL eMIOS_0 DSPI_4 — FEC	I/O I/O I/O — O	M/S	Tristate	115	139	F16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3 —	GPIO[110] E1UC[0] LIN8TX — SIN_6	SIUL eMIOS_1 LINFlexD_8 — DSPI_6	I/O I/O O — I	S	Tristate	134	158	C13
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] SOUT_6 — LIN8RX	SIUL eMIOS_1 DSPI_6 — LINFlexD_8	I/O I/O O — I	M/S	Tristate	135	159	D13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[112] E1UC[2] — — TXD[1] SIN_1	SIUL eMIOS_1 — — FEC DSPI_1	I/O I/O — — O I	M/S	Tristate	117	141	E15
PH[1]	PCR[113]	AF0 AF1 AF2 AF3 ALT4	GPIO[113] E1UC[3] SOUT_1 — TXD[0]	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O O — O	M/S	Tristate	118	142	F13
PH[2]	PCR[114]	AF0 AF1 AF2 AF3 ALT4	GPIO[114] E1UC[4] SCK_1 — TX_EN	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	119	143	D16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3 ALT4	GPIO[115] E1UC[5] CS0_1 — TX_ER	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	120	144	F14
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] SOUT_7 —	SIUL eMIOS_1 DSPI_7 —	I/O I/O O —	M/S	Tristate	162	186	D7

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PI[15]	PCR[143]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 CS2_2 — ADC0_S[23]	SIUL DSPI_4 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	75	91	P11
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 —	GPIO[144] CS1_4 CS3_2 — ADC0_S[24]	SIUL DSPI_4 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	74	90	R11
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — — — ADC0_S[25] SIN_5	SIUL — — —— ADC_0 DSPI_5	I/O — — — I I	S	Tristate	73	89	N10
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 CS0_6 CS0_7 ADC0_S[26]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O I/O I/O I/O I	S	Tristate	72	88	R10
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 CS1_6 CS1_7 ADC0_S[27]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O O O O I	S	Tristate	71	87	P10
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M/S	Tristate	5	5	D3
PJ[5]	PCR[149]	AF0 AF1 AF2 AF3 —	GPIO[149] — — — ADC0_S[28]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	113	N12
PJ[6]	PCR[150]	AF0 AF1 AF2 AF3 —	GPIO[150] — — — ADC0_S[29]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	112	N15

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PJ[15]	PCR[159]	AF0 AF1 AF2 AF3 —	GPIO[159] — CS1_6 — CAN1RX	SIUL — DSPI_6 — FlexCAN_1	I/O — O — I	M/S	Tristate	—	63	R4
PK[0]	PCR[160]	AF0 AF1 AF2 AF3	GPIO[160] CAN1TX CS2_6 —	SIUL FlexCAN_1 DSPI_6 —	I/O O O —	M/S	Tristate	—	62	T3
PK[1]	PCR[161]	AF0 AF1 AF2 AF3 —	GPIO[161] CS3_6 — — CAN4RX	SIUL DSPI_6 — — FlexCAN_4	I/O O — — I	M/S	Tristate	—	41	H4
PK[2]	PCR[162]	AF0 AF1 AF2 AF3	GPIO[162] CAN4TX — —	SIUL FlexCAN_4 — —	I/O O — —	M/S	Tristate	—	42	L4
PK[3]	PCR[163]	AF0 AF1 AF2 AF3 — —	GPIO[163] E1UC[0] — — CAN5RX LIN8RX	SIUL eMIOS_1 — — FlexCAN_5 LINFlexD_8	I/O I/O — — I I	M/S	Tristate	—	43	N1
PK[4]	PCR[164]	AF0 AF1 AF2 AF3	GPIO[164] LIN8TX CAN5TX E1UC[1]	SIUL LINFlexD_8 FlexCAN_5 eMIOS_1	I/O O O I/O	M/S	Tristate	—	44	M3
PK[5]	PCR[165]	AF0 AF1 AF2 AF3 — —	GPIO[165] — — — CAN2RX LIN2RX	SIUL — — — FlexCAN_2 LINFlexD_2	I/O — — — I I	M/S	Tristate	—	45	M5
PK[6]	PCR[166]	AF0 AF1 AF2 AF3	GPIO[166] CAN2TX LIN2TX —	SIUL FlexCAN_2 LINFlexD_2 —	I/O O O —	M/S	Tristate	—	46	M6

Table 8. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{RC_CTRL}[2]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$[3]	$V_{DD\_HV\_A}$ – 0.3	$V_{DD\_HV\_A}$+0.3	
$V_{DD\_HV\_ADC1}$[4]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$[2]	$V_{DD\_HV\_A}$–0.3	$V_{DD\_HV\_A}$+0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A/HV\_B}$	$V_{DD\_HV\_A/HV\_B}$ –0.3	$V_{DD\_HV\_A/HV\_B}$ +0.3	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}[5]	SR	Sum of all the static I/O current within a supply segment ($V_{DD\_HV\_A}$ or $V_{DD\_HV\_B}$)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	SR	Storage temperature	—	–55[6]	150	°C

NOTES:
1. $V_{DD\_HV\_B}$ can be independently controlled from $V_{DD\_HV\_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±300 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up[8]	—	—	0.5	V/µs
			—	0.5	—	V/min
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
$V_{DD\_HV\_B}$	SR	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in Section 3, "Package pinouts and signal descriptions" for the list of channels operating in $V_{DD\_HV\_B}$ domain)	—	3.0	3.6	V

2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3 Analog filters are available on all wakeup lines.
4 The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

Table 17. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	

Table 19. I/O supplies (continued)

Package	I/O Supplies							
176 LQFP	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$) pin28 (V_{SS_HV})	pin57 (V_{SS_HV}) pin59 ($V_{DD\_HV\_A}$)	pin85 ($V_{DD\_HV\_A}$) pin86 (V_{SS_HV})	pin123 (V_{SS_HV}) pin124 ($V_{DD\_HV\_B}$)	pin150 (V_{SS_HV}) pin151 ($V_{DD\_HV\_A}$)	—	—

Table 20. I/O consumption

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
I_{SWTSLW}[4]	CC	D	Peak I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	19.9	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	15.5	
I_{SWTMED}(4)	CC	D	Peak I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	28.8	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16.3	
I_{SWTFST}(4)	CC	D	Peak I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	113.5	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	52.1	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.22	mA
				C_L = 25 pF, 4 MHz		—	—	3.13	
				C_L = 100 pF, 2 MHz		—	—	6.54	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.51	
				C_L = 25 pF, 4 MHz		—	—	2.14	
				C_L = 100 pF, 2 MHz		—	—	4.33	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.5	mA
				C_L = 25 pF, 40 MHz		—	—	13.32	
				C_L = 100 pF, 13 MHz		—	—	18.26	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.91	
				C_L = 25 pF, 40 MHz		—	—	8.47	
				C_L = 100 pF, 13 MHz		—	—	10.94	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	21.05	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	55.77	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	34.89	

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

Table 43. Conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
R_{SW2}	CC	D	Internal resistance of analog source	—				2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—				0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	−5	—	5	mA
					V_{DD} = 5.0 V ± 10%	−5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload			1	3	LSB
INLS	CC	T	Absolute Integral non-linearity-Standard channels	No overload			1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	T	Absolute Offset error	—			2		LSB
GNE	CC	T	Absolute Gain error	—			2		LSB
TUEP[9]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		−6		6	LSB
		T		With current injection		−8		8	LSB
TUES[(9)]	CC	T	Total Unadjusted Error for standard channel	Without current injection		−10		10	LSB
		T		With current injection		−12		12	LSB

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} **must** be common (to be tied together externally).
3. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.
4. VDD_HV_ADC1 can operate at 5V condition while $V_{DD\_HV\_B}$ can operate at 3.3V provided that ADC_1 channels coming from $V_{DD\_HV\_B}$ domain are limited in max swing as $V_{DD\_HV\_B}$.
5. V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.
6. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.

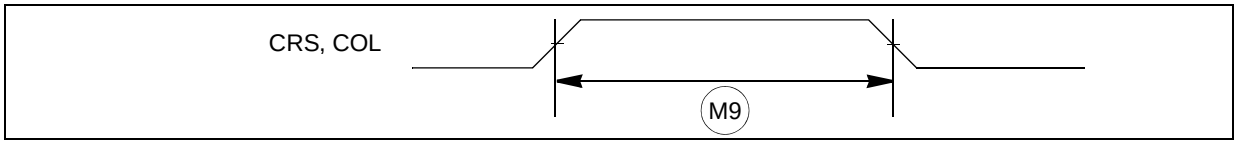

Figure 23. MII async inputs timing diagram

4.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 47. MII serial management channel timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

NOTES:
1 Output pads configured with SRE = 0b11.

Table 48. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2]	Unit
						Typ	
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

NOTES:
1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2 f_{periph} is in absolute value.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

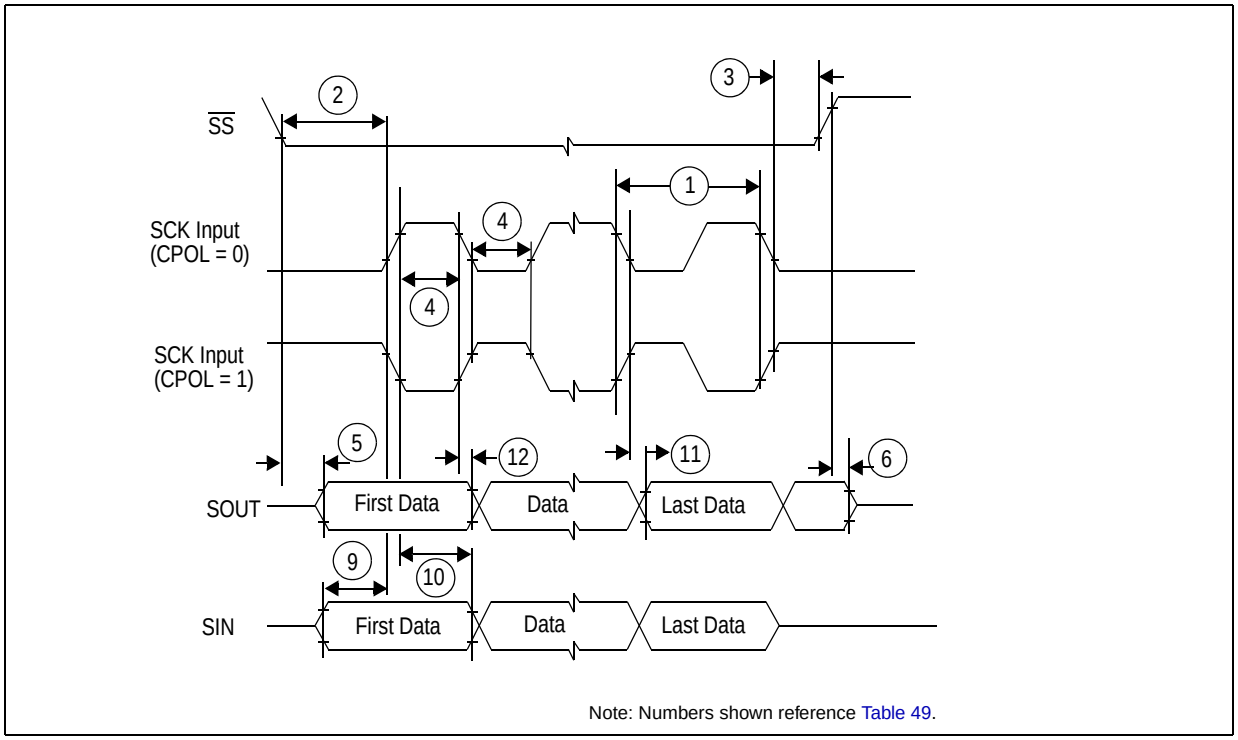

Figure 27. DSPI classic SPI timing–slave, CPHA = 0

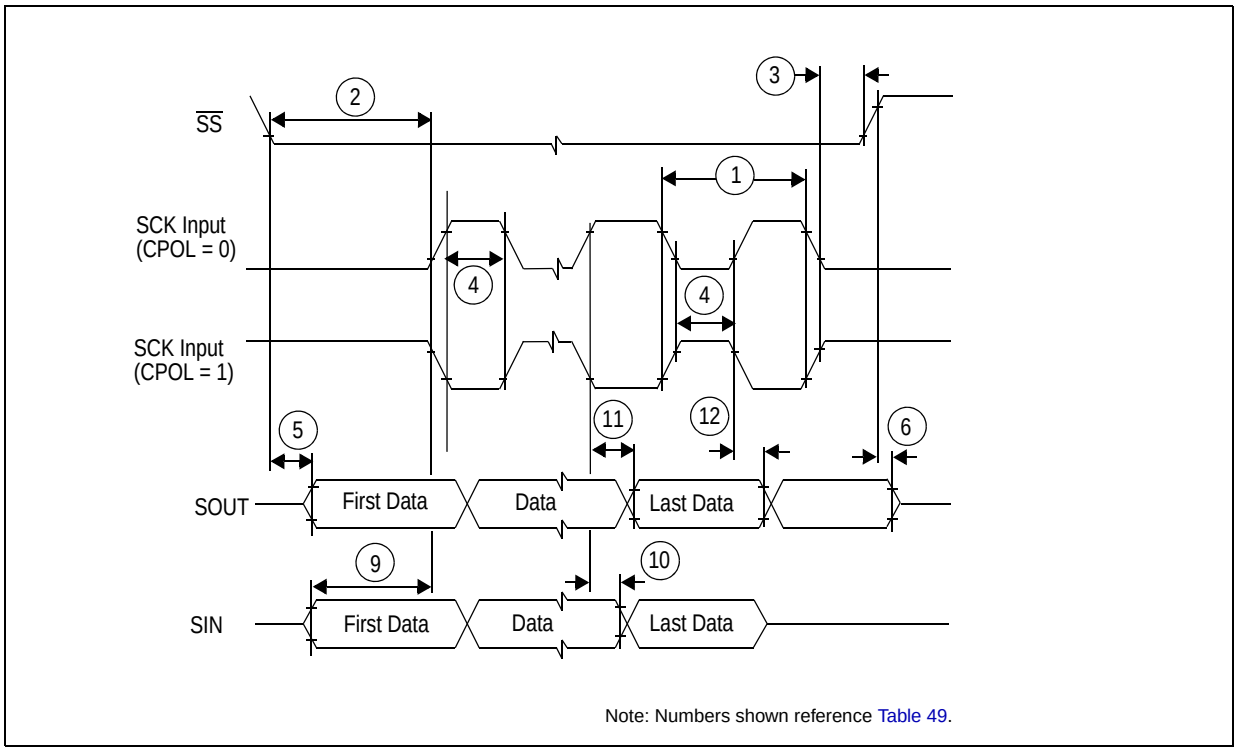

Figure 31. DSPI modified transfer format timing–slave, CPHA = 0

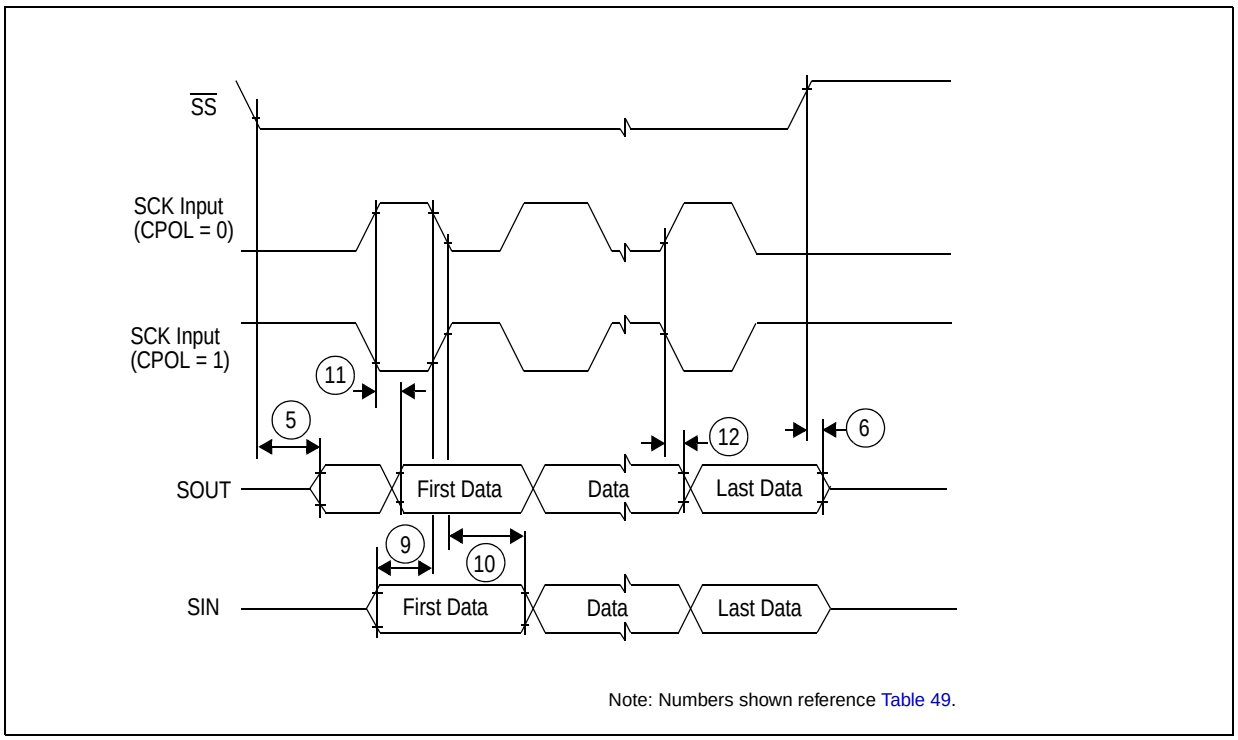

Figure 32. DSPI modified transfer format timing–slave, CPHA = 1

5.1.3 256 MAPBGA package mechanical drawing

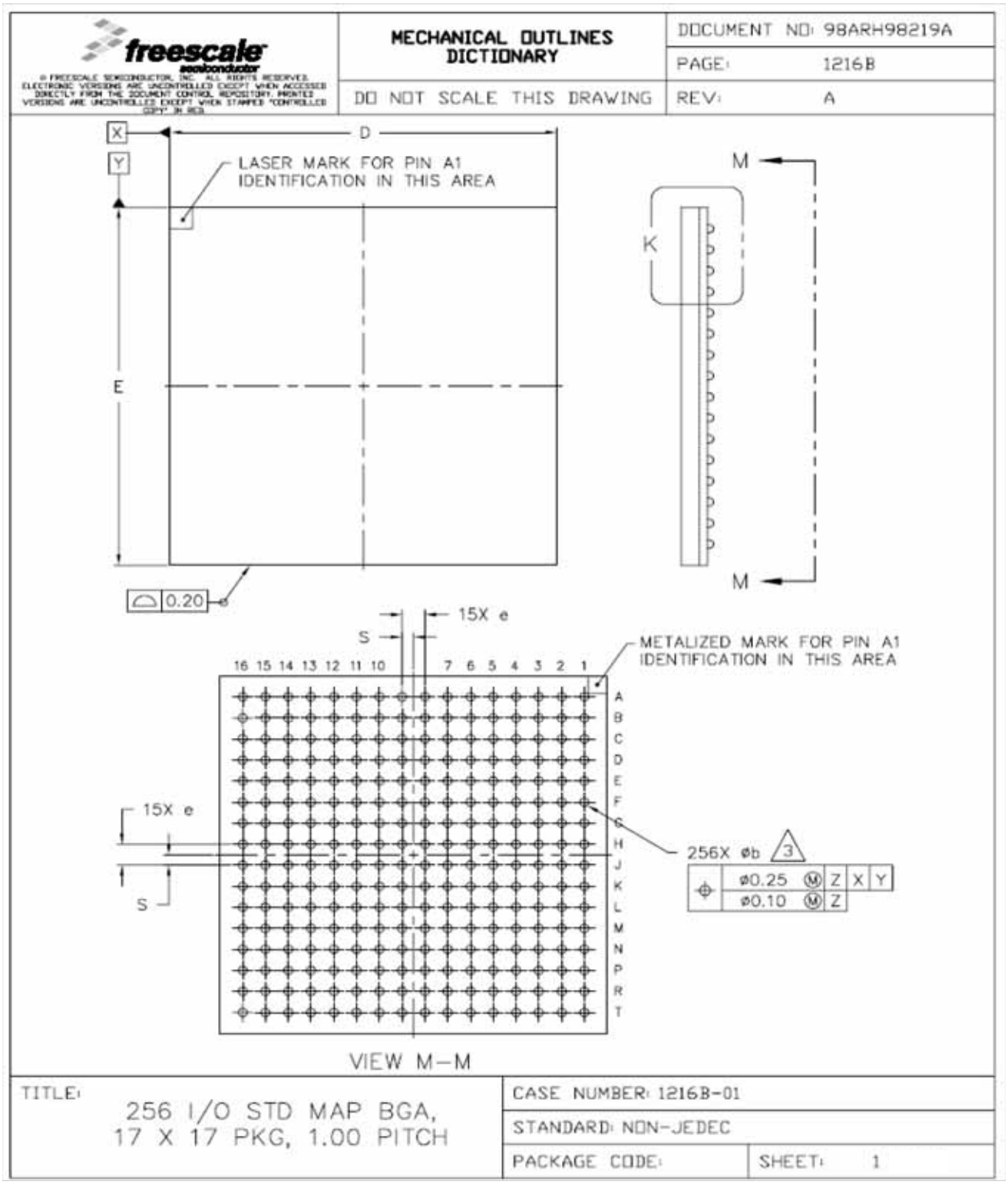

Figure 43. 256 MAPBGA mechanical drawing (Part 1 of 2)