Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

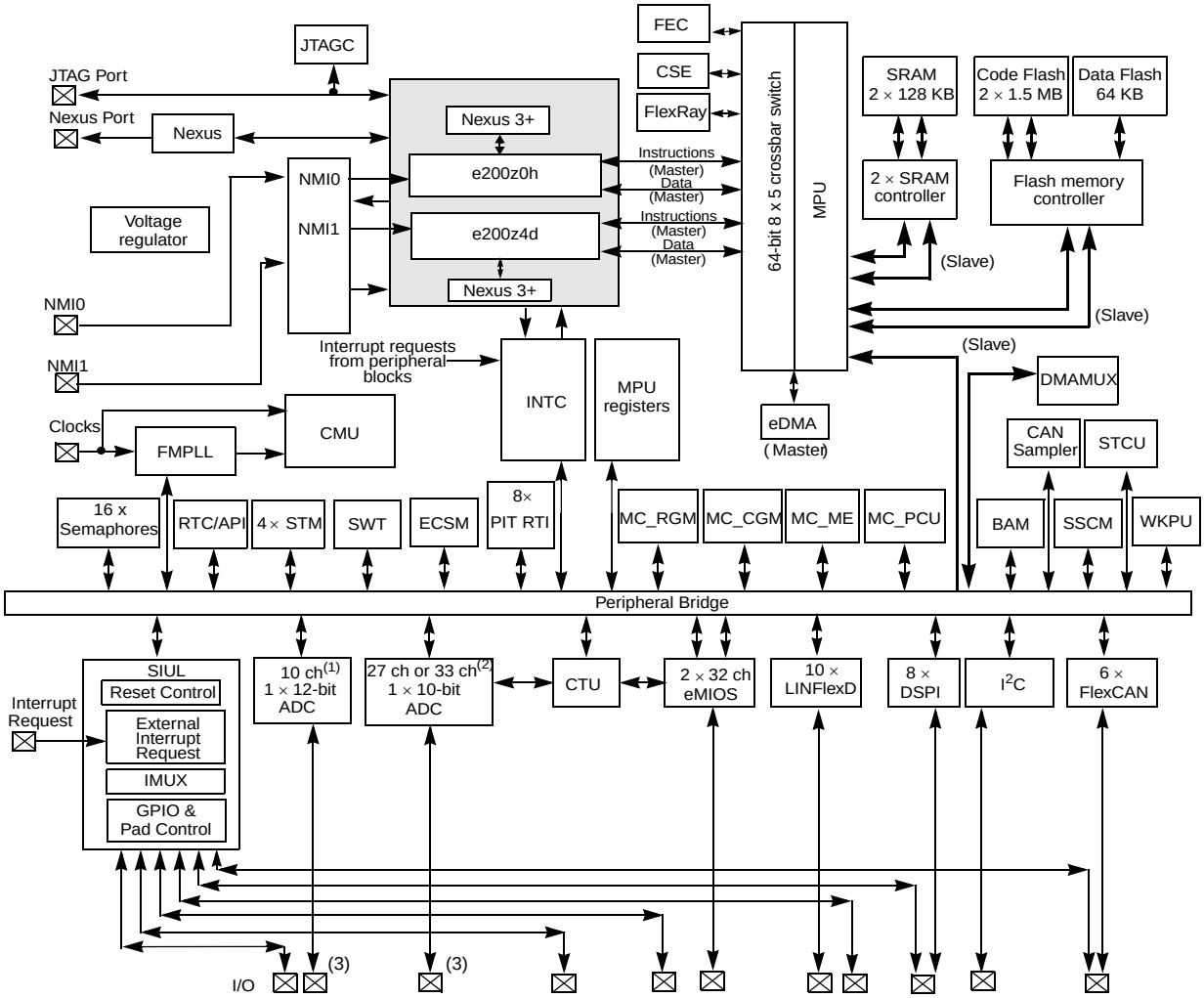
Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646bcf0vlu8r

Table of Contents

Introduction 4
1.1 Document Overview 4
1.2 Description 4
2 Block diagram 7
3 Package pinouts and signal descriptions 10
3.1 Pad types 13
3.2 System pins 14
3.3 Functional ports 14
4 Electrical Characteristics 41
4.1 Parameter classification 41
4.2 NVUSRO register 41
4.2.1 NVUSRO [PAD3V5V(0)] field description 42
4.2.2 NVUSRO [PAD3V5V(1)] field description 42
4.3 Absolute maximum ratings 42
4.4 Recommended operating conditions 44
4.5 Thermal characteristics 47
4.5.1 Package thermal characteristics 47
4.5.2 Power considerations 48
4.6 I/O pad electrical characteristics 48
4.6.1 I/O pad types 48
4.6.2 I/O input DC characteristics 49
4.6.3 I/O output DC characteristics 50
4.6.4 Output pin transition times 52
4.6.5 I/O pad current specification 53
4.7 RESET electrical characteristics 55
4.8 Power management electrical characteristics 57
4.8.1 Voltage regulator electrical characteristics 57
4.8.2 VDD_BV options 59
4.8.3 Voltage monitor electrical characteristics 60
4.9 Low voltage domain power consumption 61
4.10 Flash memory electrical characteristics 63
4.10.1 Program/Erase characteristics 63
4.10.2 Flash memory power supply DC characteristics 65
4.10.3 Flash memory start-up/switch-off timings 66
4.11 Electromagnetic compatibility (EMC) characteristics . . 66
4.11.1 Designing hardened software to avoid noise problems 66
4.11.2 Electromagnetic interference (EMI) 67
4.11.3 Absolute maximum ratings (electrical sensitivity) 67
4.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics 68
4.13 Slow external crystal oscillator (32 kHz) electrical characteristics 71
4.14 FMPLL electrical characteristics 73
4.15 Fast internal RC oscillator (16 MHz) electrical characteristics 74
4.16 Slow internal RC oscillator (128 kHz) electrical characteristics 75
4.17 ADC electrical characteristics 76
4.17.1 Introduction 76
4.18 Fast Ethernet Controller 87
4.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK) 87
4.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK) 87
4.18.3 MII Async Inputs Signal Timing (CRS and COL) 88
4.18.4 MII Serial Management Channel Timing (MDIO and MDC) 89
4.19 On-chip peripherals 91
4.19.1 Current consumption 91
4.19.2 DSPI characteristics 93
4.19.3 Nexus characteristics 101
4.19.4 JTAG characteristics 103
5 Package characteristics 105
5.1 Package mechanical data 105
5.1.1 176 LQFP package mechanical drawing 105
5.1.2 208 LQFP package mechanical drawing 108
5.1.3 256 MAPBGA package mechanical drawing . 113
6 Ordering information 115
7 Revision history 116

2 Block diagram

Figure 1 shows the detailed block diagram of the MPC5646C.

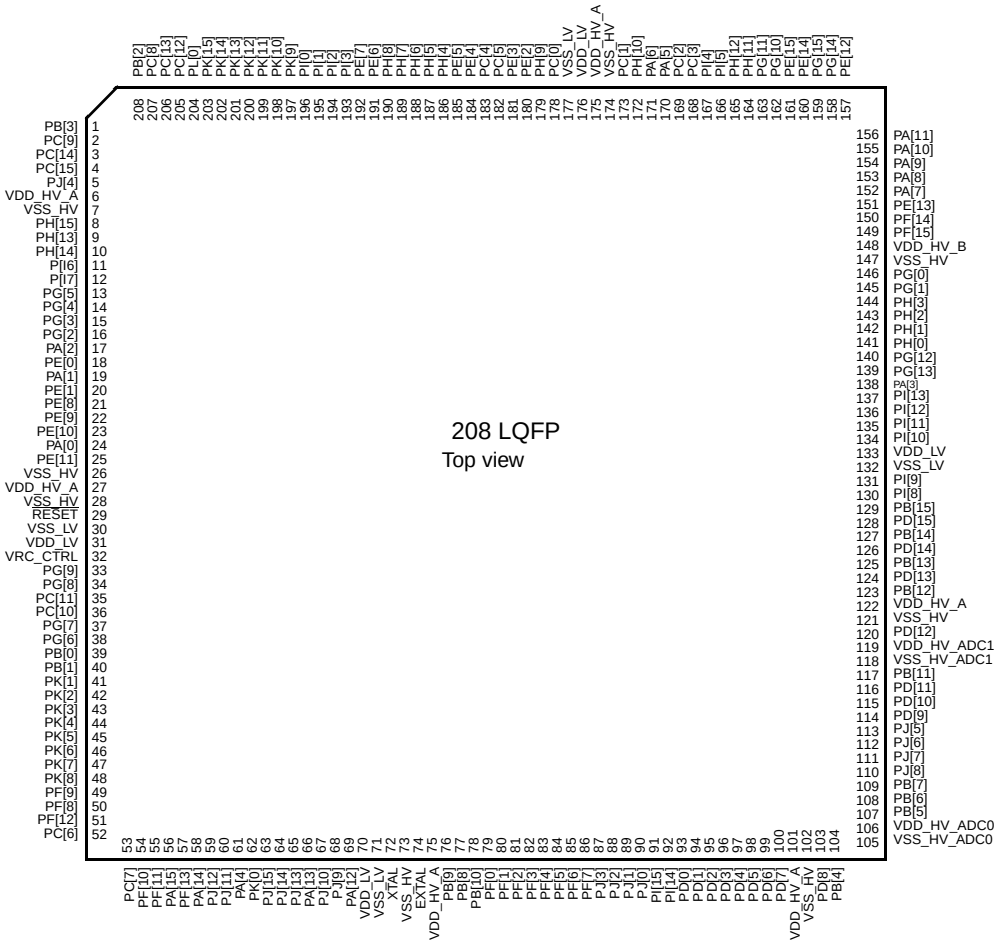


Legend:

ADC	Analog-to-Digital Converter	JTAGC	JTAG controller
BAM	Boot Assist Module	LINFlexD	Local Interconnect Network Flexible with DMA support
CSE	Cryptographic Services Engine	MC_ME	Mode Entry Module
CAN	Controller Area Network (FlexCAN)	MC_CGM	Clock Generation Module
CMU	Clock Monitor Unit	MC_PCU	Power Control Unit
CTU	Cross Triggering Unit	MC_RGM	Reset Generation Module
DMAMUX	DMA Channel Multiplexer	MPU	Memory Protection Unit
DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface
eDMA	enhanced Direct Memory Access	NMI	Non-Maskable Interrupt
FlexCAN	Controller Area Network controller modules	PIT_RTI	Periodic Interrupt Timer with Real-Time Interrupt
FEC	Fast Ethenet Controller	RTC/API	Real-Time Clock/ Autonomous Periodic Interrupt
eMIOS	Enhanced Modular Input Output System	SIUL	System Integration Unit Lite
ECSM	Error Correction Status Module	SRAM	Static Random-Access Memory
FMPLL	Frequency-Modulated Phase-Locked Loop	SSCM	System Status Configuration Module
FlexRay	FlexRay Communication Controller	STM	System Timer Module
I2C	Inter-integrated Circuit Bus	SWT	Software Watchdog Timer
IMUX	Internal Multiplexer	STCU	Self Test Control Unit
INTC	Interrupt Controller	WKPU	Wakeup Unit

Notes:
1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
3) 16 x precision channels (ANP) are mapped on input only I/O cells.

Figure 1. MPC5646C block diagram



NOTE
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

Figure 3. 208-pin LQFP configuration

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	108	130	J14
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	131	J15
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	134	J16
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	S	Tristate	111	135	H16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 CS0_2 — ADC0_S[20]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	112	136	G15
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 CS1_2 — ADC0_S[21]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	113	137	G14
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	S	Tristate	76	92	T12

4.2.1 NVUSRO [PAD3V5V(0)] field description

Table 6 shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD\_HV\_A}$ domain.

Table 6. PAD3V5V(0) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

4.2.2 NVUSRO [PAD3V5V(1)] field description

Table 7 shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD\_HV\_B}$ domain.

Table 7. PAD3V5V(1) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

4.3 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on VDD_HV_B pins with respect to common ground (V_{SS_HV})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD\_HV\_A/HV\_B}$ or $V_{IN} < V_{SS\_HV}$), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on $V_{DD\_HV\_A}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on $V_{DD\_HV\_B}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}[3]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$[4]	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	3.0[5]	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$[7]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	

Medium and fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.6.2 I/O input DC characteristics

Table 13 provides input DC electrical characteristics as described in Figure 5.

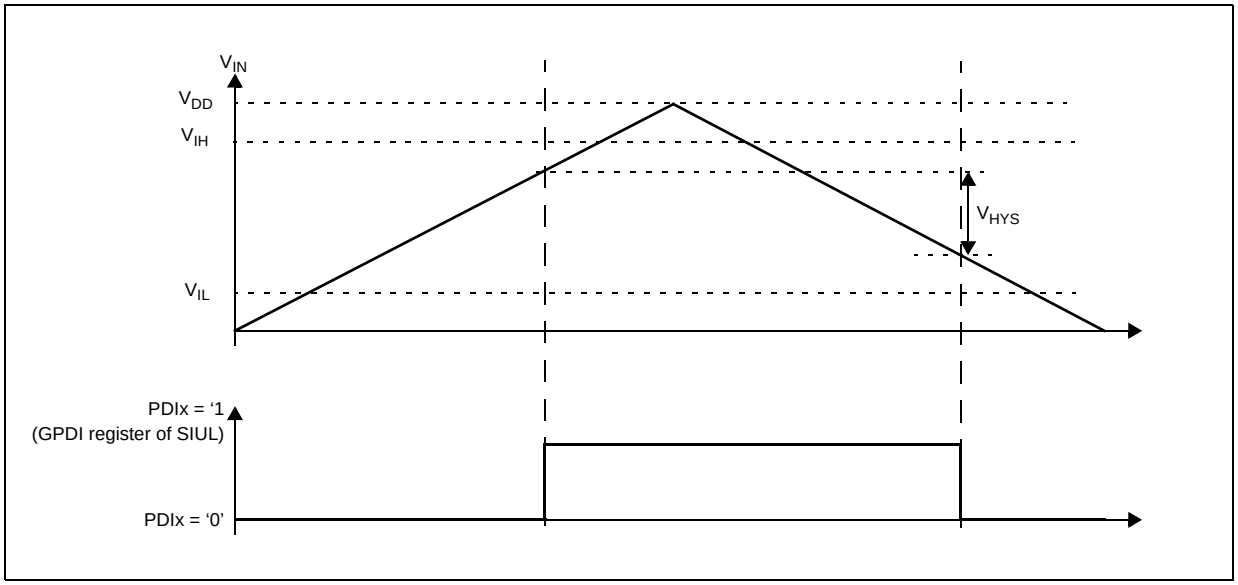


Figure 5. I/O input DC electrical characteristics definition

Table 13. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.3	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	P	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	—	nA
		P			T_A = 25 °C	—	2	—	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}	SR	P	Width of input pulse rejected by analog filter[3]	—		—	—	40[4]	ns
W_{NFI}	SR	P	Width of input pulse accepted by analog filter(3)	—		1000[4]	—	—	ns

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3 Analog filters are available on all wakeup lines.
4 The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

Table 21. Reset electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	Reset input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	Reset input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the RGM module section of the device Reference Manual).
4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.8 Power management electrical characteristics

4.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage supply $V_{DD\_HV\_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD\_HV\_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.

Table 22. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600[3]	mA

NOTES:
1. $V_{DD\_HV\_A}$ = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

4.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

NOTE

When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

Table 24. Low voltage power domain electrical characteristics[1]

Symbol		C	Parameter	Conditions[2]		Value			Unit
						Min	Typ[3]	Max[4]	
I_{DDMAX}[5]	CC	D	RUN mode maximum average current	—		—	210	300[6,7]	mA
I_{DDRUN}	CC	P	RUN mode typical average current[8]	at 120 MHz	T_A = 25 °C	—	150	200[9]	mA
		D		at 80 MHz	T_A = 25 °C	—	110[8]	150[10]	mA
		C		at 120 MHz	T_A = 125 °C	—	180	270	mA
I_{DDHALT}	CC	P	HALT mode current[11]	at 120 MHz	T_A = 25 °C	—	20	27	mA
		C		at 120 MHz	T_A = 125 °C	—	35	113	mA
I_{DDSTOP}	CC	P	STOP mode current[12]	No clocks active	T_A = 25 °C	—	0.4	3	mA
		C			T_A = 125 °C	—	16	95	mA
$I_{DDSTDBY3}$ (96 KB RAM retained)	CC	P	STANDBY3 mode current[13]	No clocks active	T_A = 25 °C	—	50	99	µA
		C			T_A = 125 °C	—	630	3200	µA
$I_{DDSTDBY2}$ (64 KB RAM retained)	CC	C	STANDBY2 mode current[14]	No clocks active	T_A = 25 °C	—	40	94	µA
		C			T_A = 125 °C	—	500	2500	µA
$I_{DDSTDBY1}$ (8 KB RAM retained)	CC	C	STANDBY1 mode current[15]	No clocks active	T_A = 25 °C	—	25	87	µA
		C			T_A = 125 °C	—	230	1250	µA
Adders in LP mode	CC	T	32 KHz OSC	—	T_A = 25 °C	—	—	5	µA
			4–40 MHz OSC	—	T_A = 25 °C	—	—	3	mA
			16 MHz IRC	—	T_A = 25 °C	—	—	500	µA
			128 KHz IRC	—	T_A = 25 °C	—	—	5	µA

NOTES:
1. Except for I_{DDMAX}, all the current values are total current drawn from $V_{DD\_HV\_A}$.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may sunk by device during power-up and standby exit. Please refer to in rush current in Table 22.
7. Maximum “allowed” current is package dependent.
8. Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.

[9] Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.

[10] This value is obtained from limited sample set.

[11] Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

[12] Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.

[13] Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[14] Only for the "P" classification: LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[15] LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF.

4.10 Flash memory electrical characteristics

4.10.1 Program/Erase characteristics

Table 25 shows the code flash memory program and erase characteristics.

Table 25. Code flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	18	50	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	200	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	300	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	600	1300	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}[5]		C	Erase Suspend Request Rate	20	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	10	10	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

NOTES:

[1] Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

[2] Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

[3] The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

[4] Actual hardware programming times. This does not include software overhead.

[5] It is Time between erase suspend resume and the next erase suspend request.

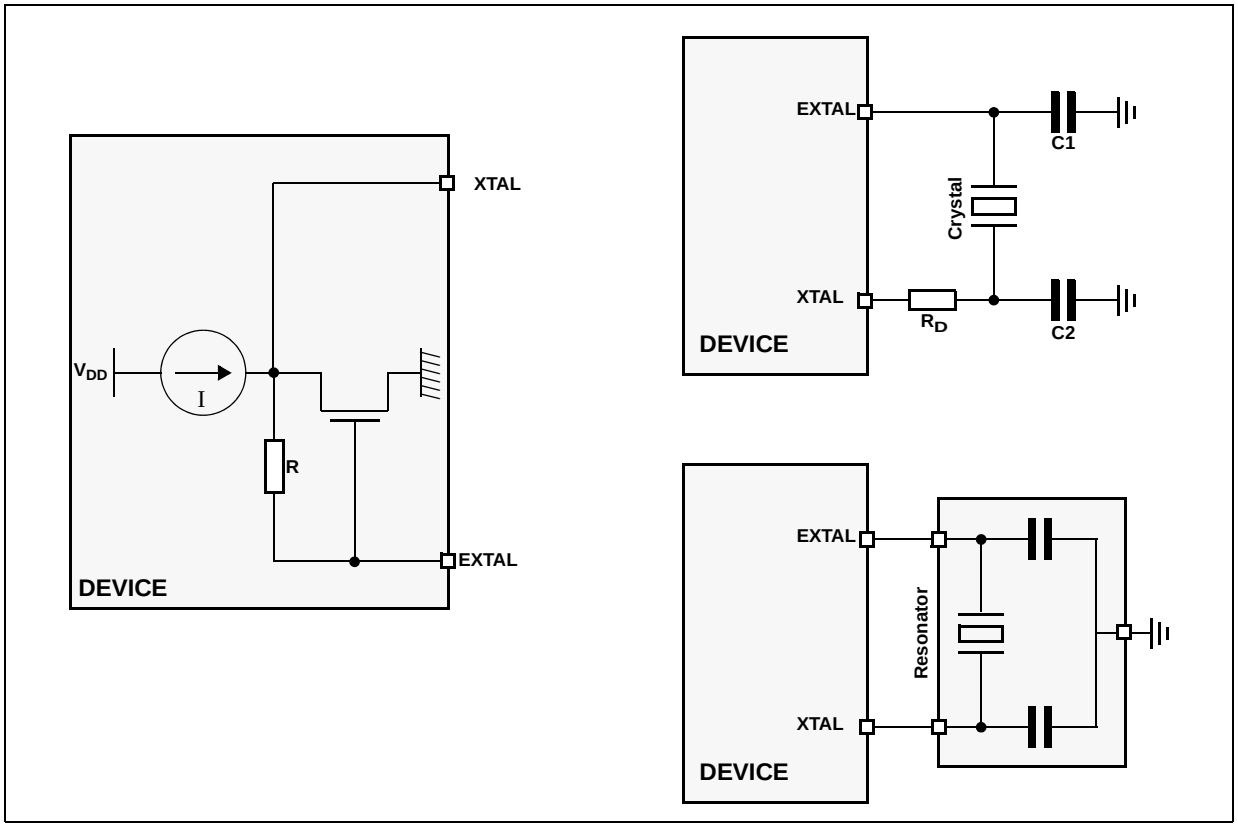


Figure 10. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 34. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00
40	NX5032GA	50	6.18	2.56	8	3.49

NOTES:
1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD\_HV\_A}$	—	$V_{DD\_HV\_A}$ + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.3	—	$0.35V_{DD\_HV\_A}$	V

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE Cz
4. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

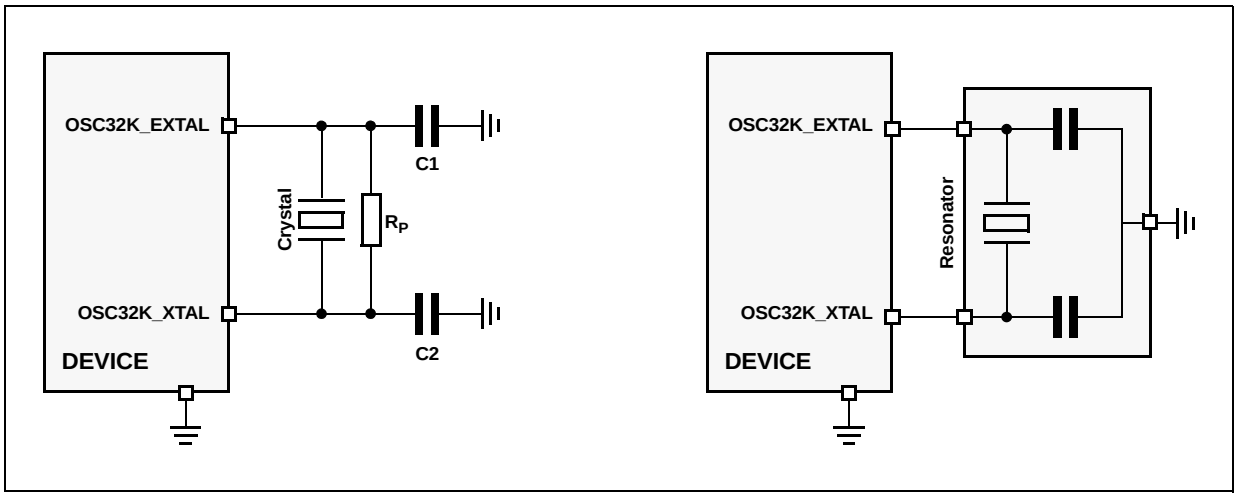


Figure 12. Crystal oscillator and resonator connection scheme

NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

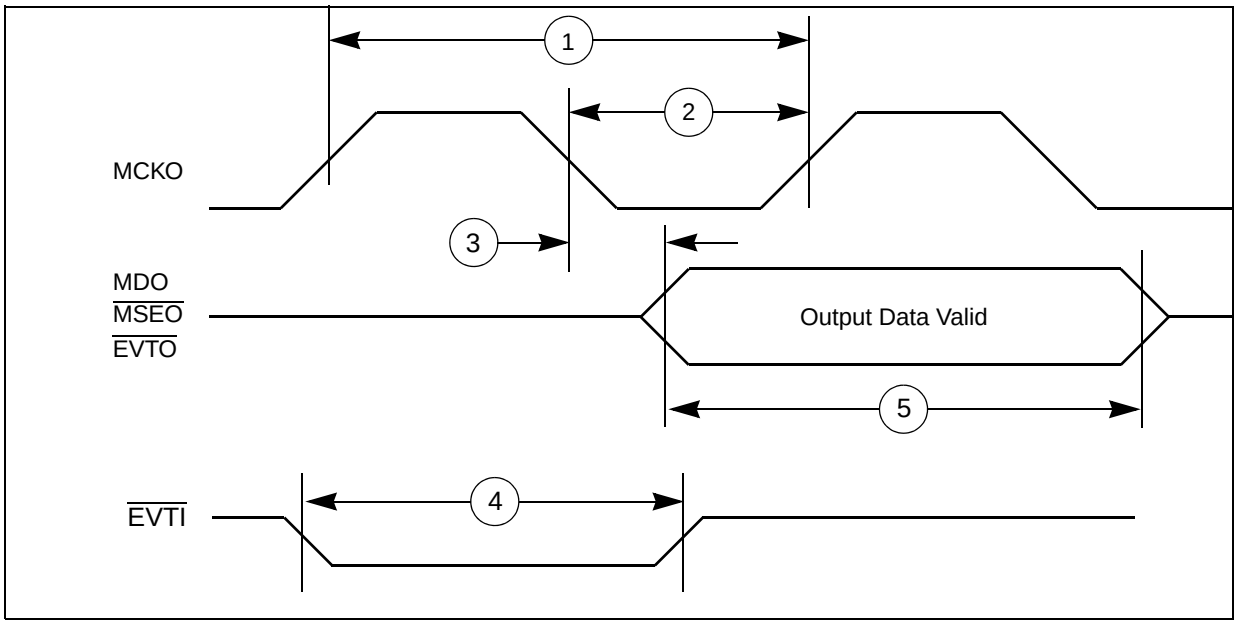


Figure 34. Nexus output timing

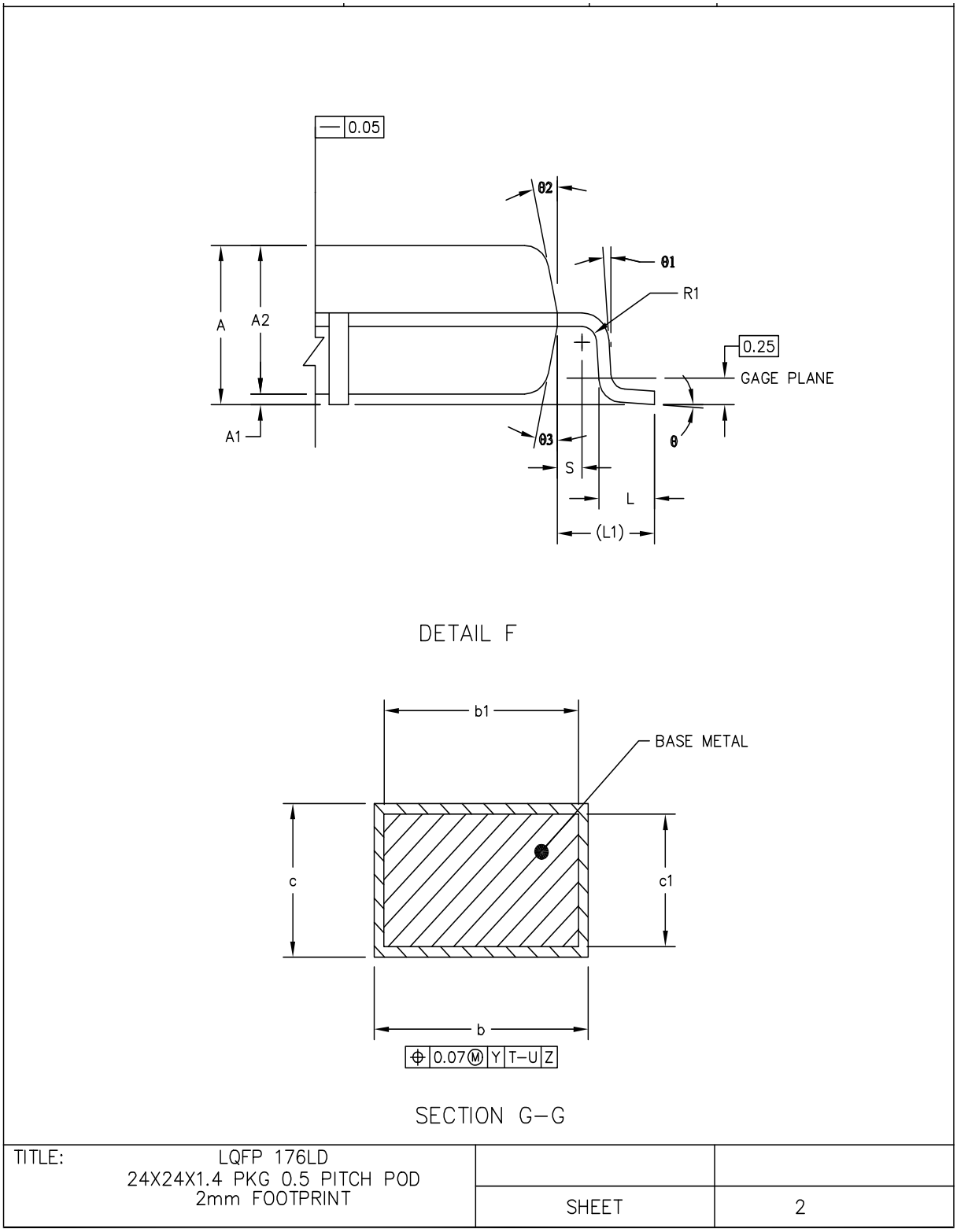


Figure 38. 176 LQFP mechanical drawing (Part 2 of 3)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75								

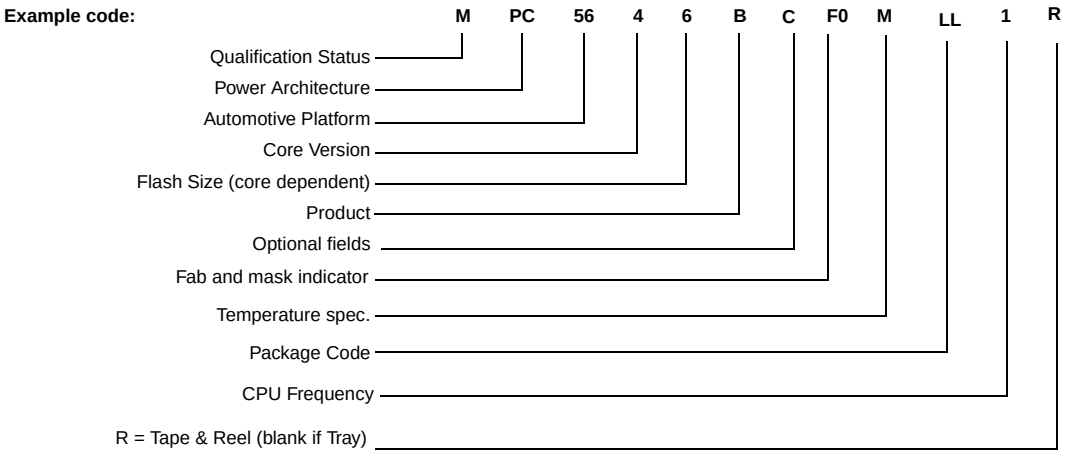
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:		
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	3

Figure 39. 176 LQFP mechanical drawing (Part 3 of 3)

5.1.2 208 LQFP package mechanical drawing

6 Ordering information



Qualification Status
M = MC status
S = Auto qualified
P = PC status

PC = Power Architecture

Automotive Platform
56 = Power Architecture in 90 nm

Core Version
4 = e200z4d core version (highest core version in the case of multiple cores)

Flash Memory Size
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

Product Version
B = Body
C = Gateway

Optional fields
C = CSE module available
Blank = none of these options available

Fab and mask version indicator
F = ATMC
0 = First version of the mask

Temperature spec.
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C

Package Code
LU = 176 LQFP
LT = 208 LQFP
MJ = 256 MAPBGA

CPU Frequency
1 = e200z4d operates up to 120 MHz
8 = e200z4d operates up to 80 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Note: Not all options are available on all devices. Refer to Table 1, which shows the orderable part numbers for MPC564xx.

Figure 45. Orderable parts

Table 52. Revision history (continued)

Revision	Date	Changes
4	23 June 2011	• Interchanged the denominator with numerator in Equation 11 of Input impedance and ADC accuracy section • Removed the note (All ADC conversion characteristics described in the table below are applicable only for the precision channels. The data for semi-precision and extended channels is awaited and same will be subsequently updated in later revs.) in the ADC electrical characteristics section. • In On-chip peripherals current consumption table, replaced IDD_HV_ADC with IDD_HV_ADC0 and IDD_HV_ADC1 values as per ADC specs • In ADC conversion characteristics (10-bit ADC_0) table, the minimum sample time of ADC0 changed to 500 at 32 MHz • In ADC conversion characteristics (10-bit ADC_0) table, removed the entry for sample time at 30 MHz • In Conversion characteristics (12-bit ADC_1)table, changed TUEX to TUES and INLX to INLS (Extended channels are not supported by the device. So, changed to standard channel.)

Table 52. Revision history (continued)

Revision	Date	Changes
6	12 Feb 2014	• Removed occurrences of 208BGA from Table 3 System pin descriptions. • Added PM[3] and PM[4] in the figure note 1 of Figure 4, 256-pin BGA configuration. • Added a table note in Table 19 I/O supplies. • Updated Figure 8, Voltage regulator capacitance connection and added a note in this figure. • Removed max values of V_{LPREG} and V_{MREG}, changed min value of V_{LPREG} to 1.21 V, and updated V_{MREG} and V_{LPREG} after trimming values in Table 22 Voltage regulator electrical characteristics. • Updated 1st footnote and updated max values for I_{DDRUN}, I_{DDHALT}, I_{DDSTOP}, $I_{DDSTDBY3}$, $I_{DDSTDBY2}$, $I_{DDSTDBY1}$ and removed values at 85°C and 105°C in Table 24 Low voltage power domain electrical characteristics. • Added a footnote below Table 28 Flash memory read access timing. • Updated the formula in Eq. 11 in Section 4.17.1.1, "Input impedance and ADC accuracy. • Added Figure 17, Input equivalent circuit (extended channels). • Updated t_{ADC0_PU} value to 1.5 as max and added footnote for I_{INJ} in Table 42 ADC conversion characteristics (10-bit ADC_0). • Added Category column in Table 43 Conversion characteristics (12-bit ADC_1). • Added the IDD_HV_ADC0 values in Table 48 On-chip peripherals current consumption. • Added a note in Figure 45, Orderable parts.

NOTE

This revision history uses clickable cross-references for ease of navigation. The numbers and titles in each cross-reference are relative to the latest published release.