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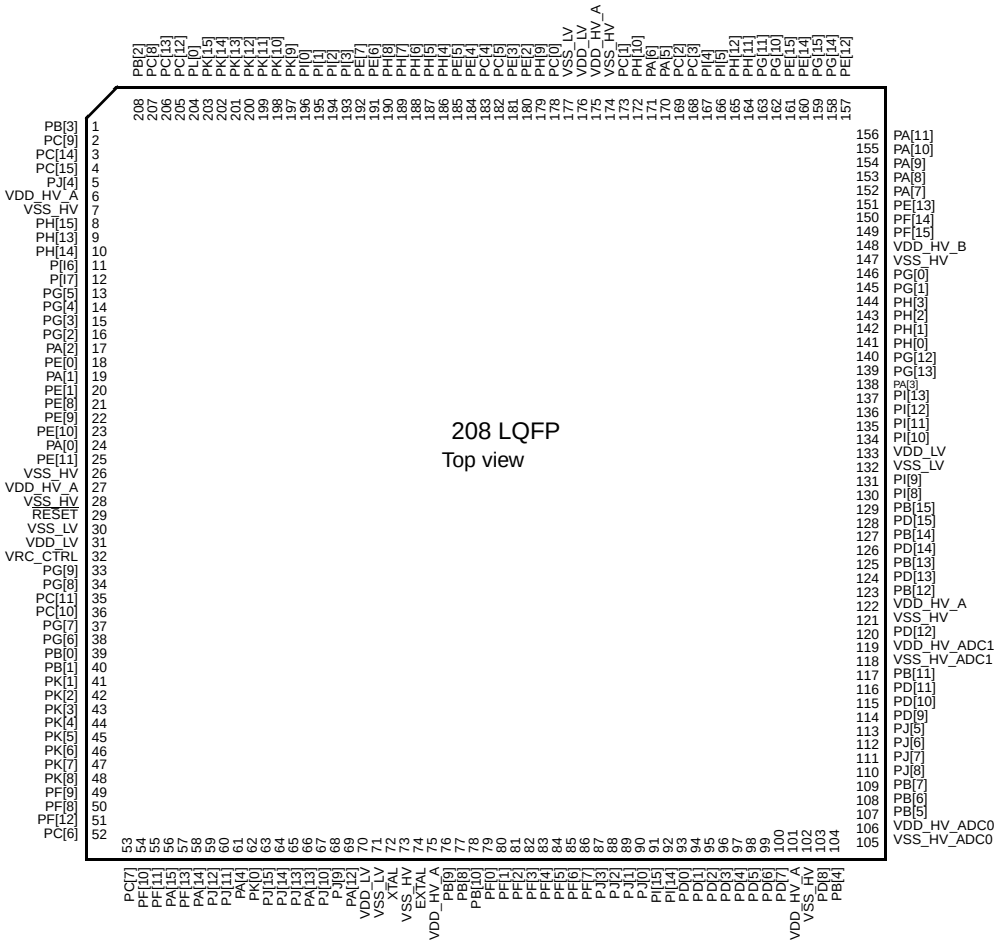
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646bf0mlu1



NOTE
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

Figure 3. 208-pin LQFP configuration

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M/S	Tristate	52	66	R5
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M/S	Tristate	50	58	P4
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M/S	Tristate	48	56	R2
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlexD_0	I/O O I/O I	M/S	Tristate	39	39	L3
PB[1]	PCR[17]	AF0 AF1 AF2 — — —	GPIO[17] — E0UC[31] LIN0RX WKPU[4] CAN0RX	SIUL — eMIOS_0 LINFlexD_0 WKPU FlexCAN_0	I/O — I/O I I I	S	Tristate	40	40	M2
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlexD_0 I^2C eMIOS_0	I/O O I/O I/O	M/S	Tristate	176	208	A2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11] LIN0RX	SIUL eMIOS_0 I^2C — WKPU LINFlexD_0	I/O I/O I/O — I I	S	Tristate	1	1	D4
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — —	GPI[20] — — — ADC0_P[0] ADC1_P[0]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	88	104	T16

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	S	Tristate	97	117	M13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	101	123	L14
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	103	125	L15
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/S	Input, weak pull-up	154	178	B10
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/M	Tristate	149	173	D9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/S	Tristate	145	169	B11

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX EIRQ[6]	SIUL DSPI_1 ADC_0 — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O I I I	S	Tristate	144	168	C11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 ALT4 — — —	GPIO[36] E1UC[31] — FR_B_TX_EN SIN_1 CAN3RX EIRQ[18]	SIUL eMIOS_1 — Flexray DSPI_1 FlexCAN_3 SIUL	I/O I/O — O I I I	M/S	Tristate	159	183	A9
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[37] SOUT_1 CAN3TX — FR_A_TX EIRQ[7]	SIUL DSPI_1 FlexCAN_3 — Flexray SIUL	I/O O O — O I	M/S	Tristate	158	182	B9
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] —	SIUL LINFlexD_1 eMIOS_1 —	I/O O I/O —	S	Tristate	44	52	N3
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] — LIN1RX WKPU[12]	SIUL — eMIOS_1 — LINFlexD_1 WKPU	I/O — I/O — I I	S	Tristate	45	53	N4
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[13]	PCR[77]	AF0 AF1 AF2 AF3 —	GPIO[77] SOUT_2 E1UC[20] — RXD[3]	SIUL DSPI_2 eMIOS_1 — FEC	I/O O I/O — I	M/S	Tristate	127	151	C16
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	M/S	Tristate	136	160	A14
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] SCK_6	SIUL DSPI_2 eMIOS_1 DSPI_6	I/O I/O I/O I/O	M/S	Tristate	137	161	C12
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ADC0_S[8]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	63	79	P7
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3
PF[14]	PCR[94]	AF0 AF1 AF2 AF3 ALT4	GPIO[94] CAN4TX E1UC[27] CAN1TX MDIO	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1 FEC	I/O O I/O O I/O	M/S	Tristate	126	150	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — — —	GPIO[95] E1UC[4] — — RX_DV CAN1RX CAN4RX EIRQ[13]	SIUL eMIOS_1 — — FEC FlexCAN_1 FlexCAN_4 SIUL	I/O I/O — — I I I I	M/S	Tristate	125	149	D15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3 ALT4	GPIO[96] CAN5TX E1UC[23] — MDC	SIUL FlexCAN_5 eMIOS_1 — FEC	I/O O I/O — O	F	Tristate	122	146	E13
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — — —	GPIO[97] — E1UC[24] — TX_CLK CAN5RX EIRQ[14]	SIUL — eMIOS_1 — FEC FlexCAN_5 SIUL	I/O — I/O — I I I	M	Tristate	121	145	E14
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M/S	Tristate	16	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	15	15	E1
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M/S	Tristate	14	14	F2

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1

4 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 5 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see MPC5646C Reference Manual.

4.2.1 NVUSRO [PAD3V5V(0)] field description

Table 6 shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD\_HV\_A}$ domain.

Table 6. PAD3V5V(0) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

4.2.2 NVUSRO [PAD3V5V(1)] field description

Table 7 shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD\_HV\_B}$ domain.

Table 7. PAD3V5V(1) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

4.3 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on VDD_HV_B pins with respect to common ground (V_{SS_HV})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V

Table 18. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[4] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 All values need to be confirmed during device validation.
4 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply is associated to a V_{DD}/V_{SS_HV} supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 19. I/O supplies

Package	I/O Supplies							
256 MAPBGA	Equivalent to 208-pin LQFP segment pad distribution + G6, G11, H11, J11							
208 LQFP	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$) pin28 (V_{SS_HV})	pin73 (V_{SS_HV}) pin75 ($V_{DD\_HV\_A}$)	pin101 ($V_{DD\_HV\_A}$) pin102 (V_{SS_HV})	pin132 (V_{SS_HV}) pin133 ($V_{DD\_HV\_A}$)	pin147 (V_{SS_HV}) pin148 ($V_{DD\_HV\_B}$)	pin174 (V_{SS_HV}) pin175 ($V_{DD\_HV\_A}$)	—

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 31. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	120	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP176 package Test conforming to IEC 61967-2, f_{OSC} = 40 MHz/f_{CPU} = 120 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14[3]	dBµV

NOTES:
1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.
3. All values need to be confirmed during device validation.

4.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 32. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

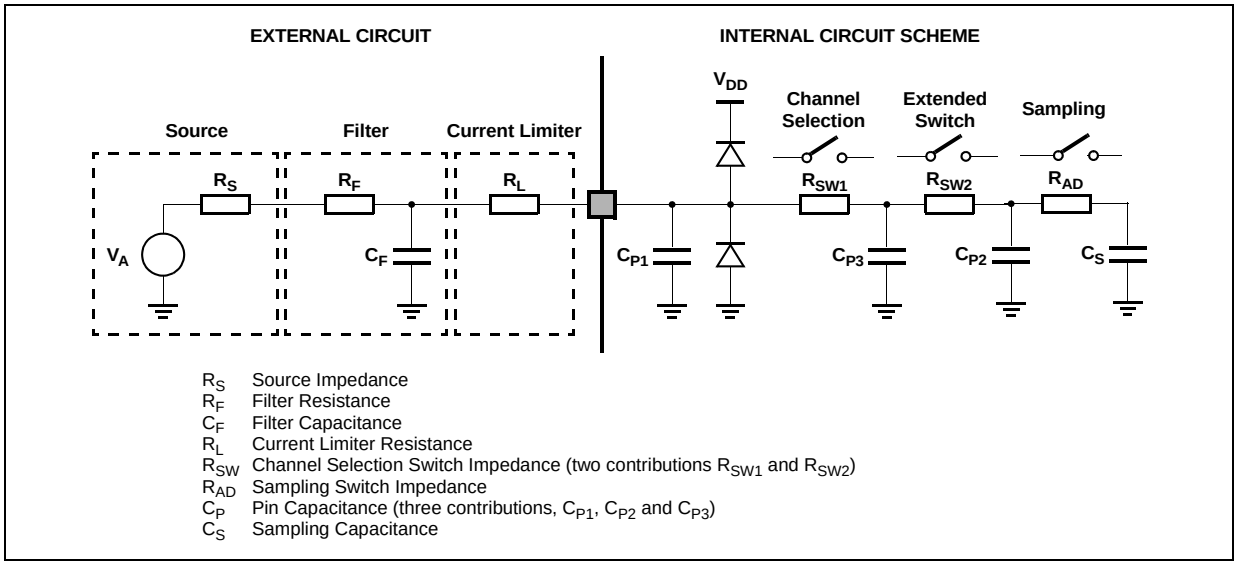


Figure 17. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 16): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

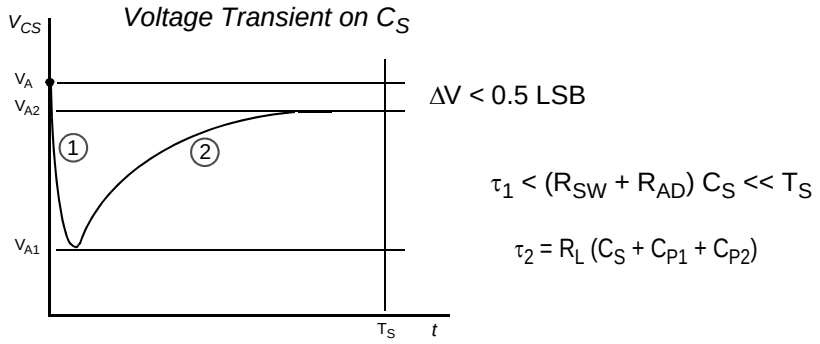


Figure 18. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

4.17.1.2 ADC electrical characteristics

Table 41. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 42. ADC conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1	—	$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 2%	MHz
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[4]	f_{ADC} = 32 MHz	500	—		ns
t_{ADC0_C}	CC	P	Conversion time[5,6]	f_{ADC} = 32 MHz	0.625	—		µs
				f_{ADC} = 30 MHz	0.700	—		
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ

Table 48. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2]	Unit
						Typ	
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

NOTES:
1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2 f_{periph} is in absolute value.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

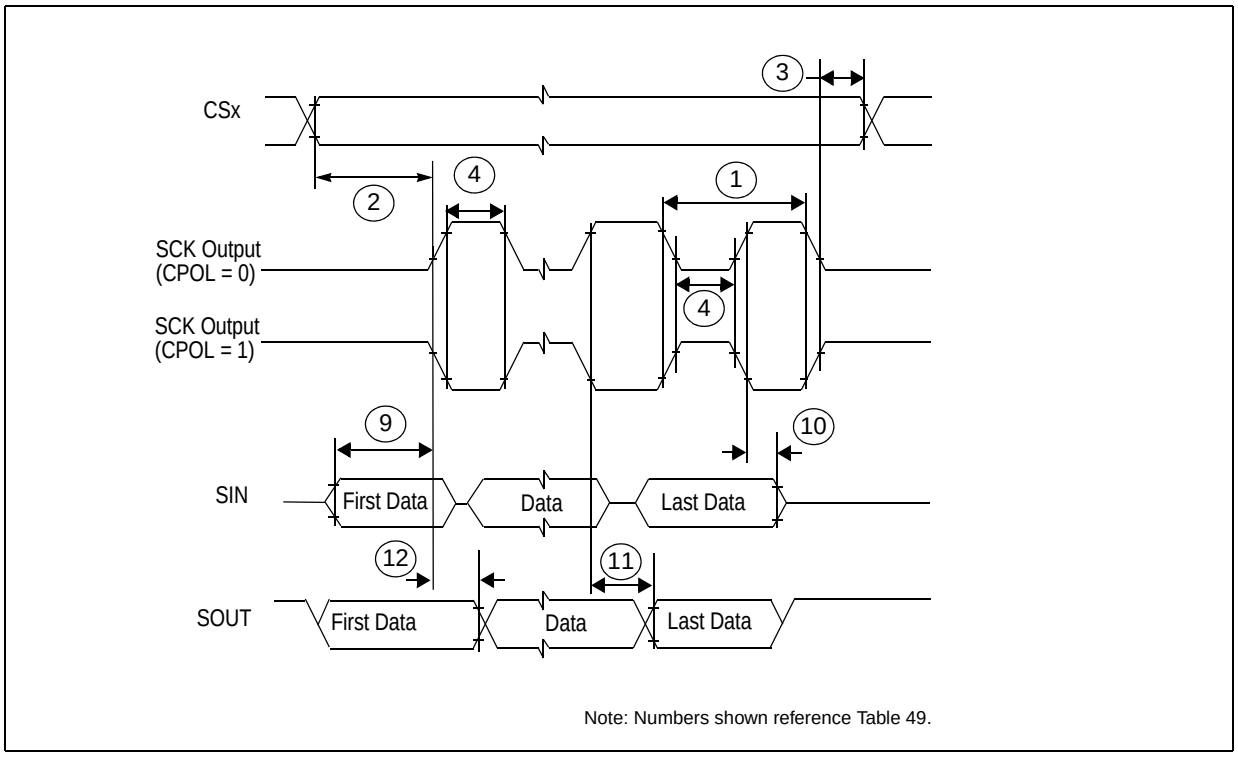


Figure 29. DSPI modified transfer format timing–master, CPHA = 0

Table 51. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

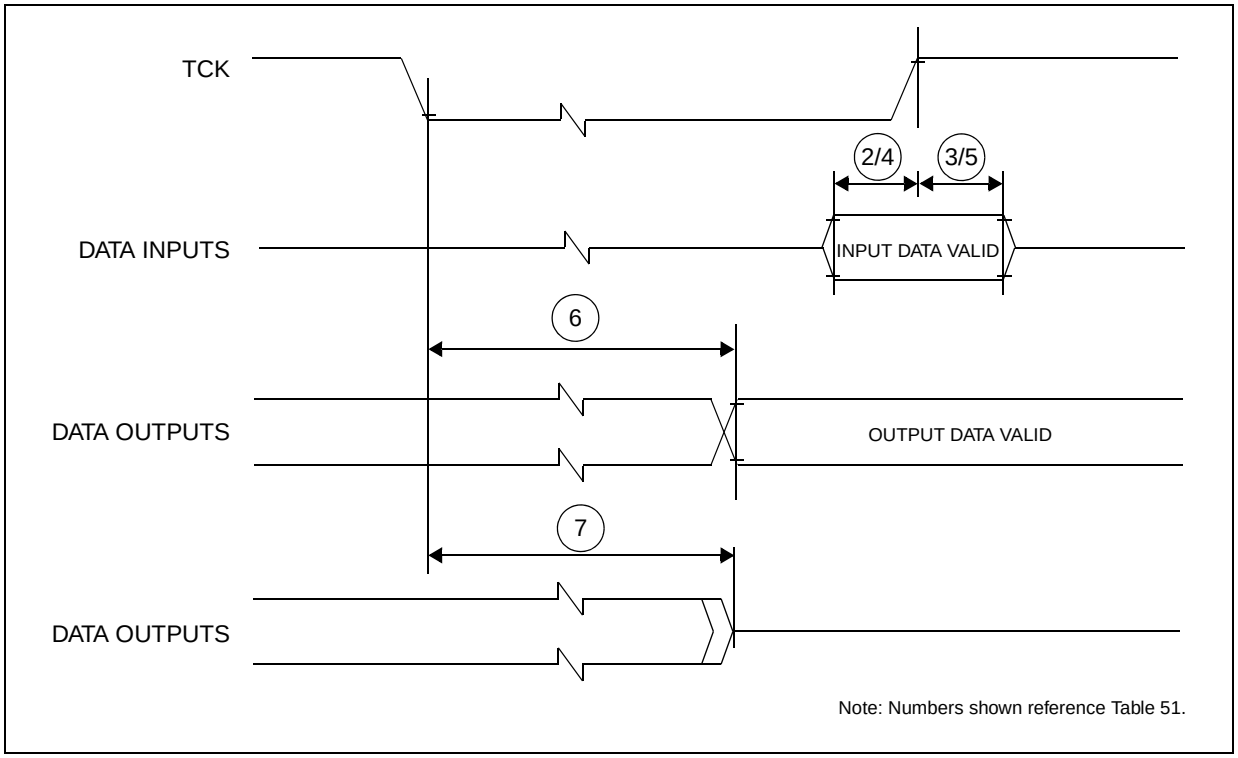


Figure 36. Timing diagram - JTAG boundary scan

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75								

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:		
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	3

Figure 39. 176 LQFP mechanical drawing (Part 3 of 3)

5.1.2 208 LQFP package mechanical drawing

Table 52. Revision history (continued)

Revision	Date	Changes
3	28 April 2011	• Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics • Updated Crystal oscillator and resonator connection scheme figure • Specified NPN transistor as the recommended BCP68 transistor throughout the document • Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} • Revised the footnotes in the “Functional port pin descriptions” table. • In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. • Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] • ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. • Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classification from “C” to “D”. • Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. • Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. • Functional port pin description: Added a footnote at the PB [9] port pin. • Absolute maximum ratings table: Added footnote 1. • Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. • Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. • FMPLL electrical characteristics table: Updated Δt_{LTJIT}. • Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. • MII serial management channel timing table: Updated M12 • JTAG characteristics table: Updated t_{TDOV}. • Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. • DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. • IO consumption table: Updated all parameter values. • DSPI electricals: Updated Δt_{CSC} max to 115 ns. • Low voltage power domain electrical characteristics table: Added footnote 9. • ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.