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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646bf0mlu1r

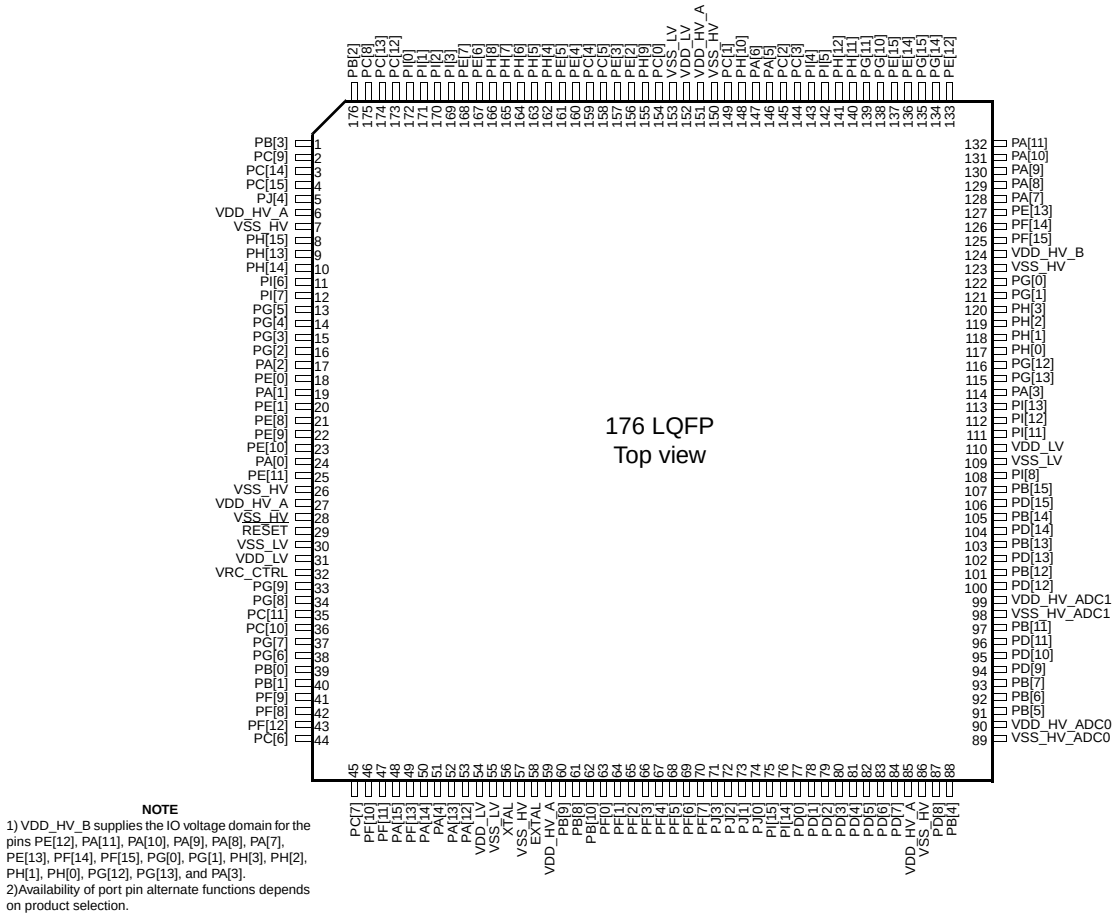
Table 1. MPC5646C family comparison[1] (continued)

Feature	MPC5644B		MPC5644C			MPC5645B		MPC5645C			MPC5646B		MPC5646C		
Package	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO[12]	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

NOTES:
1 Feature set dependent on selected peripheral multiplexing; table shows example.
2 Based on 125 °C ambient operating temperature and subject to full device characterisation.
3 The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4 DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5 Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6 There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7 16x precision channels (ANP) and 3x standard (ANS).
8 Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9 As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10 CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11 STCU controls MBIST activation and reporting.
12 Estimated I/O count for proposed packages based on multiplexing with peripherals.

3 Package pinouts and signal descriptions

The available LQFP pinouts and the MAPBGA ballmaps are provided in the following figures. For functional port pin description, see Table 4.



NOTE

1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2)Availability of port pin alternate functions depends on product selection.

Figure 2. 176-pin LQFP configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]									PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]									PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]			VSS_LV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTRL	VDD_LV	PG[9]			VSS_LV	VSS_LV	VSS_HV	VSS_HV			PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]			VSS_LV	VSS_LV	VSS_LV	VDD_LV			PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]									PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]									PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — —	GPI[21] — — — ADC0_P[1] ADC1_P[1]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	91	107	N13
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — —	GPI[22] — — — ADC0_P[2] ADC1_P[2]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	92	108	N14
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — —	GPI[23] — — — ADC0_P[3] ADC1_P[3]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	93	109	R16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPI[24] — — — ADC0_S[0] ADC1_S[4] WKPU[25] OSC32k_XTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	61	77	T11
PB[9][5]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPI[25] — — — ADC0_S[1] ADC1_S[5] WKPU[26] OSC32k_EXTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	60	76	T10
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] SOUT_1 CAN3TX — ADC0_S[2] ADC1_S[6] WKPU[8]	SIUL DSPI_1 FlexCAN_3 — ADC_0 ADC_1 WKPU	I/O O — — I I I	S	Tristate	62	78	N7

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	108	130	J14
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	131	J15
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	134	J16
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	S	Tristate	111	135	H16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 CS0_2 — ADC0_S[20]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	112	136	G15
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 CS1_2 — ADC0_S[21]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	113	137	G14
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	S	Tristate	76	92	T12

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up[8]	—	—	0.5	V/µs
			—	0.5	—	V/min
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
$V_{DD\_HV\_B}$	SR	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in Section 3, ”Package pinouts and signal descriptions” for the list of channels operating in $V_{DD\_HV\_B}$ domain)	—	3.0	3.6	V

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}[4]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$[5]	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$[7]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} –0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up[8]	—	—	0.5	V/µs
			—	0.5	—	V/min
T_{A} C-Grade Part	SR	Ambient temperature under bias	—	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	—	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	—	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
3. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin.

Table 17. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	

Table 19. I/O supplies (continued)

Package	I/O Supplies							
176 LQFP	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$) pin28 (V_{SS_HV})	pin57 (V_{SS_HV}) pin59 ($V_{DD\_HV\_A}$)	pin85 ($V_{DD\_HV\_A}$) pin86 (V_{SS_HV})	pin123 (V_{SS_HV}) pin124 ($V_{DD\_HV\_B}$)	pin150 (V_{SS_HV}) pin151 ($V_{DD\_HV\_A}$)	—	—

Table 20. I/O consumption

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
I_{SWTSLW}[4]	CC	D	Peak I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	19.9	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	15.5	
I_{SWTMED}(4)	CC	D	Peak I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	28.8	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16.3	
I_{SWTFST}(4)	CC	D	Peak I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	113.5	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	52.1	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.22	mA
				C_L = 25 pF, 4 MHz		—	—	3.13	
				C_L = 100 pF, 2 MHz		—	—	6.54	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.51	
				C_L = 25 pF, 4 MHz		—	—	2.14	
				C_L = 100 pF, 2 MHz		—	—	4.33	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.5	mA
				C_L = 25 pF, 40 MHz		—	—	13.32	
				C_L = 100 pF, 13 MHz		—	—	18.26	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.91	
				C_L = 25 pF, 40 MHz		—	—	8.47	
				C_L = 100 pF, 13 MHz		—	—	10.94	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	21.05	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	55.77	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	34.89	

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

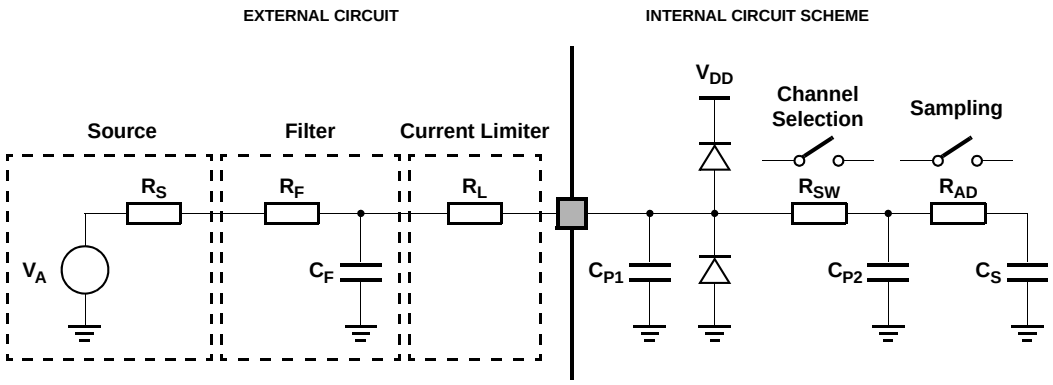
Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with $CS+Cp_2$ equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*($CS+Cp_2$)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $CS+Cp_2$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the following relation

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.



R_S	Source Impedance
R_F	Filter Resistance
C_F	Filter Capacitance
R_L	Current Limiter Resistance
R_{SW}	Channel Selection Switch Impedance
R_{AD}	Sampling Switch Impedance
C_P	Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S	Sampling Capacitance

Figure 16. Input equivalent circuit (precise channels)

4.19.2 DSPI characteristics

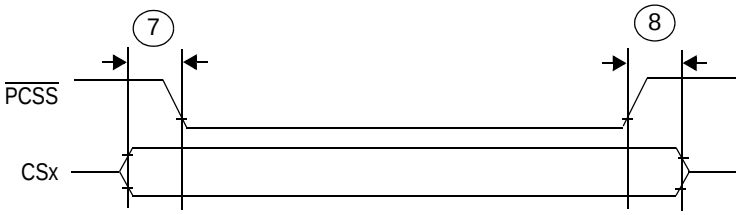
Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

Table 49. DSPI timing (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Data Setup Time for Inputs	t_{SUI}			
	Master (MTFE = 0)		36	—	ns
	Slave		5	—	ns
	Master (MTFE = 1, CPHA = 0)[5]		36	—	ns
	Master (MTFE = 1, CPHA = 1)		36	—	ns
10	Data Hold Time for Inputs	t_{HI}			
	Master (MTFE = 0)		0	—	ns
	Slave		4	—	ns
	Master (MTFE = 1, CPHA = 0)[5]		0	—	ns
	Master (MTFE = 1, CPHA = 1)		0	—	ns
11	Data Valid (after SCK edge)	t_{SUO}			
	Master (MTFE = 0)		—	12	ns
	Slave		—	37	ns
	Master (MTFE = 1, CPHA = 0)		—	12	ns
	Master (MTFE = 1, CPHA = 1)		—	12	ns
12	Data Hold Time for Outputs	t_{HO}			
	Master (MTFE = 0)		0[6]	—	ns
	Slave		9.5	—	ns
	Master (MTFE = 1, CPHA = 0)		0[7]	—	ns
	Master (MTFE = 1, CPHA = 1)		0[8]	—	ns

NOTES:
1. This value of this parameter is dependent upon the external device delays and the other parameters mentioned in this table.
2. The maximum value is programmable in DSPI_CTAR*n* [PSSCK] and DSPI_CTAR*n* [CSSCK]. For MPC5646C, the spec value of t_{CSC} will be attained only if T_{DSPI} x PSSCK x CSSCK > Δt_{CSC}.
3. The maximum value is programmable in DSPI_CTAR*n* [PASC] and DSPI_CTAR*n* [ASC]. For MPC5646C, the spec value of t_{ASC} will be attained only if T_{DSPI} x PASC x ASC > $\Delta t_{ASC.}$
4. The parameter value is obtained from t_{SUSS} and t_{SUO} for slave.
5. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b00.
6. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 0) is –2 ns.
7. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 0) is –2 n.
8. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 1) is –2 ns.



Note: Numbers shown reference Table 49.

Figure 33. DSPI PCS strobe (PCSS) timing

4.19.3 Nexus characteristics

Table 50. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time[2]	t_{MCYC}	16.3	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, MSEO, EVTO Data Valid[3]	t_{MDOV}	–0.1	0.25	t_{MCYC}
4	EVTI Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
5	EVTO Pulse Width	t_{EVTOPW}	1		t_{MCYC}
6	TCK Cycle Time[4]	t_{TCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
9	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

NOTES:
1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DDE} = 4.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.
2. MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.
3. MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.
4. The system clock frequency needs to be three times faster than the TCK frequency.

Figure 44. 256 MAPBGA mechanical drawing (Part 2 of 2)

Table 52. Revision history (continued)

Revision	Date	Changes
3	28 April 2011	• Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics • Updated Crystal oscillator and resonator connection scheme figure • Specified NPN transistor as the recommended BCP68 transistor throughout the document • Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} • Revised the footnotes in the “Functional port pin descriptions” table. • In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. • Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] • ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. • Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classification from “C” to “D”. • Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. • Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. • Functional port pin description: Added a footnote at the PB [9] port pin. • Absolute maximum ratings table: Added footnote 1. • Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. • Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. • FMPLL electrical characteristics table: Updated Δt_{LTJIT}. • Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. • MII serial management channel timing table: Updated M12 • JTAG characteristics table: Updated t_{TDOV}. • Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. • DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. • IO consumption table: Updated all parameter values. • DSPI electricals: Updated Δt_{CSC} max to 115 ns. • Low voltage power domain electrical characteristics table: Added footnote 9. • ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.

Table 52. Revision history (continued)

Revision	Date	Changes
6	12 Feb 2014	• Removed occurrences of 208BGA from Table 3 System pin descriptions. • Added PM[3] and PM[4] in the figure note 1 of Figure 4, 256-pin BGA configuration. • Added a table note in Table 19 I/O supplies. • Updated Figure 8, Voltage regulator capacitance connection and added a note in this figure. • Removed max values of V_{LPREG} and V_{MREG}, changed min value of V_{LPREG} to 1.21 V, and updated V_{MREG} and V_{LPREG} after trimming values in Table 22 Voltage regulator electrical characteristics. • Updated 1st footnote and updated max values for I_{DDRUN}, I_{DDHALT}, I_{DDSTOP}, $I_{DDSTDBY3}$, $I_{DDSTDBY2}$, $I_{DDSTDBY1}$ and removed values at 85°C and 105°C in Table 24 Low voltage power domain electrical characteristics. • Added a footnote below Table 28 Flash memory read access timing. • Updated the formula in Eq. 11 in Section 4.17.1.1, "Input impedance and ADC accuracy. • Added Figure 17, Input equivalent circuit (extended channels). • Updated t_{ADC0_PU} value to 1.5 as max and added footnote for I_{INJ} in Table 42 ADC conversion characteristics (10-bit ADC_0). • Added Category column in Table 43 Conversion characteristics (12-bit ADC_1). • Added the IDD_HV_ADC0 values in Table 48 On-chip peripherals current consumption. • Added a note in Figure 45, Orderable parts.

NOTE

This revision history uses clickable cross-references for ease of navigation. The numbers and titles in each cross-reference are relative to the latest published release.