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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d, e200z0h
Core Size	32-Bit Dual-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646ccf0mlu1

Table 4. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 — —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] CAN1RX	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU FlexCAN_1	I/O I/O O I/O I I	M/S	Tristate	24	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — — —	GPIO[1] E0UC[1] — — WKPU[2] CAN3RX NMI[0][3]	SIUL eMIOS_0 — — WKPU FlexCAN_3 WKPU	I/O I/O — — I I I	S	Tristate	19	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 — —	GPIO[2] E0UC[2] — MA[2] WKPU[3] NMI[1][3]	SIUL eMIOS_0 — ADC_0 WKPU WKPU	I/O I/O — O I I	S	Tristate	17	17	F1
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — — —	GPIO[3] E0UC[3] LIN5TX CS4_1 RX_ER_CLK EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlexD_5 DSPI_1 FEC SIUL ADC_1	I/O I/O O O I I I	M/S	Tristate	114	138	G16
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9]	SIUL eMIOS_0 — DSPI_1 LINFlexD_5 WKPU	I/O I/O — I/O I I	S	Tristate	51	61	T2
PA[5]	PCR[5]	AF0 AF1 AF2	GPIO[5] E0UC[5] LIN4TX	SIUL eMIOS_0 LINFlexD_4	I/O I/O O	M/S	Tristate	146	170	C10
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 LIN4RX EIRQ[1]	SIUL eMIOS_0 — DSPI_1 LINFlexD_4 SIUL	I/O I/O — O I I	S	Tristate	147	171	D11

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — —	GPI[21] — — — ADC0_P[1] ADC1_P[1]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	91	107	N13
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — —	GPI[22] — — — ADC0_P[2] ADC1_P[2]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	92	108	N14
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — —	GPI[23] — — — ADC0_P[3] ADC1_P[3]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	93	109	R16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPI[24] — — — ADC0_S[0] ADC1_S[4] WKPU[25] OSC32k_XTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	61	77	T11
PB[9][5]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPI[25] — — — ADC0_S[1] ADC1_S[5] WKPU[26] OSC32k_EXTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	60	76	T10
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] SOUT_1 CAN3TX — ADC0_S[2] ADC1_S[6] WKPU[8]	SIUL DSPI_1 FlexCAN_3 — ADC_0 ADC_1 WKPU	I/O O — — I I I	S	Tristate	62	78	N7

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPI[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	87	103	P14
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPI[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	94	114	N16
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPI[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	95	115	M14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPI[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	96	116	M15
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	S	Tristate	100	120	L13
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	S	Tristate	102	124	K14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[62] CS1_1 E0UC[26] — FR_DBG[0] ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	104	126	K13

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD\_HV\_A/HV\_B}$ or $V_{IN} < V_{SS\_HV}$), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on $V_{DD\_HV\_A}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on $V_{DD\_HV\_B}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}[3]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$[4]	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	3.0[5]	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$[7]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}[4]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$[5]	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$[7]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} –0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up[8]	—	—	0.5	V/µs
			—	0.5	—	V/min
T_{A} C-Grade Part	SR	Ambient temperature under bias	—	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	—	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	—	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
3. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin.

[9] Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.

[10] This value is obtained from limited sample set.

[11] Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

[12] Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.

[13] Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[14] Only for the "P" classification: LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.

[15] LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF.

4.10 Flash memory electrical characteristics

4.10.1 Program/Erase characteristics

Table 25 shows the code flash memory program and erase characteristics.

Table 25. Code flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	18	50	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	200	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	300	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	600	1300	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}[5]		C	Erase Suspend Request Rate	20	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	10	10	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

NOTES:

[1] Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

[2] Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

[3] The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

[4] Actual hardware programming times. This does not include software overhead.

[5] It is Time between erase suspend resume and the next erase suspend request.

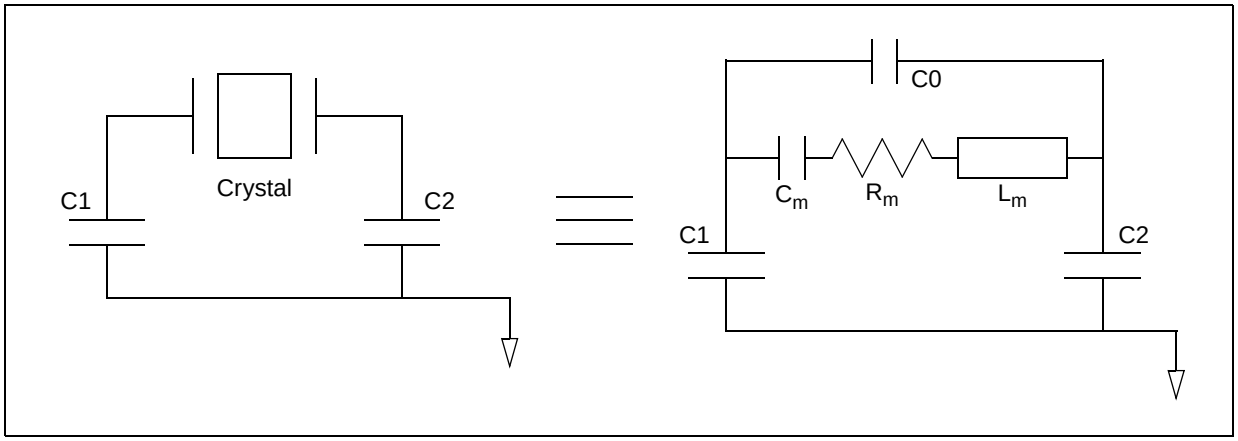

Figure 13. Equivalent circuit of a quartz crystal

Table 36. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled @ C0 = 2.85 pF[4]	—	—	65	kΩ
		AC coupled @ C0 = 4.9 pF[(4)]	—	—	50	
		AC coupled @ C0 = 7.0 pF[(4)]	—	—	35	
		AC coupled @ C0 = 9.0 pF[(4)]	—	—	30	

NOTES:
1 The crystal used is Epson Toyocom MC306.
2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3 Maximum ESR (R_m) of the crystal is 50 kΩ.
4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

Table 38. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle(3)	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4 f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	100	nA
		D		T_A = 55 °C	—	—	200	nA
		D		T_A = 125 °C	—	—	1	µA

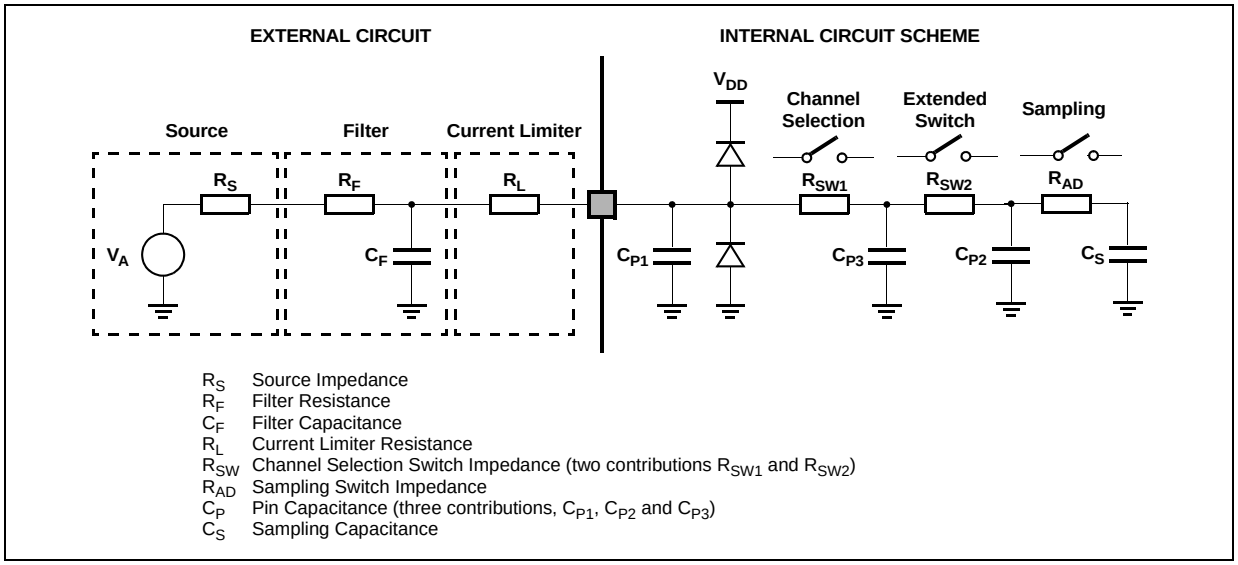

Figure 17. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 16): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

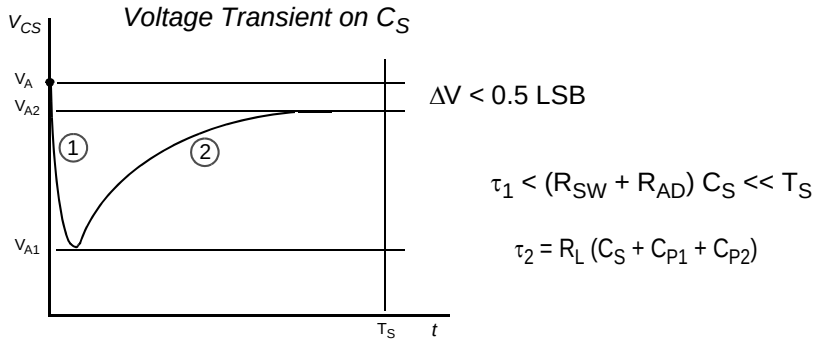

Figure 18. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

4.19 On-chip peripherals

4.19.1 Current consumption

Table 48. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2] Typ	Unit
$I_{DD\_HV\_A(CAN)}$	CC	D	CAN (FlexCAN) supply current on $V_{DD\_HV\_A}$	500 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs	$7.652 \times f_{periph} + 84.73$	µA
				125 Kbps		$8.0743 \times f_{periph} + 26.757$	
$I_{DD\_HV\_A(eMIOS)}$	CC	D	eMIOS supply current on $V_{DD\_HV\_A}$	Static consumption: eMIOS channel OFF Global prescaler enabled		$28.7 \times f_{periph}$	
				Dynamic consumption: It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_HV\_A(SCI)}$	CC	D	SCI (LINFlex) supply current on $V_{DD\_HV\_A}$	Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps		$4.7804 \times f_{periph} + 30.946$	
$I_{DD\_HV\_A(SPI)}$	CC	D	SPI (DSPI) supply current on $V_{DD\_HV\_A}$	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits		$16.3 \times f_{periph}$	
$I_{DD\_HV\_A(ADC)}$	CC	D	ADC supply current on $V_{DD\_HV\_A}$	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	$0.0409 \times f_{periph}$	mA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)	$0.0049 \times f_{periph}$	
IDD_HV_ADC0	CC	D	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	4	mA

Table 48. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2]	Unit
						Typ	
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

NOTES:
1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2 f_{periph} is in absolute value.

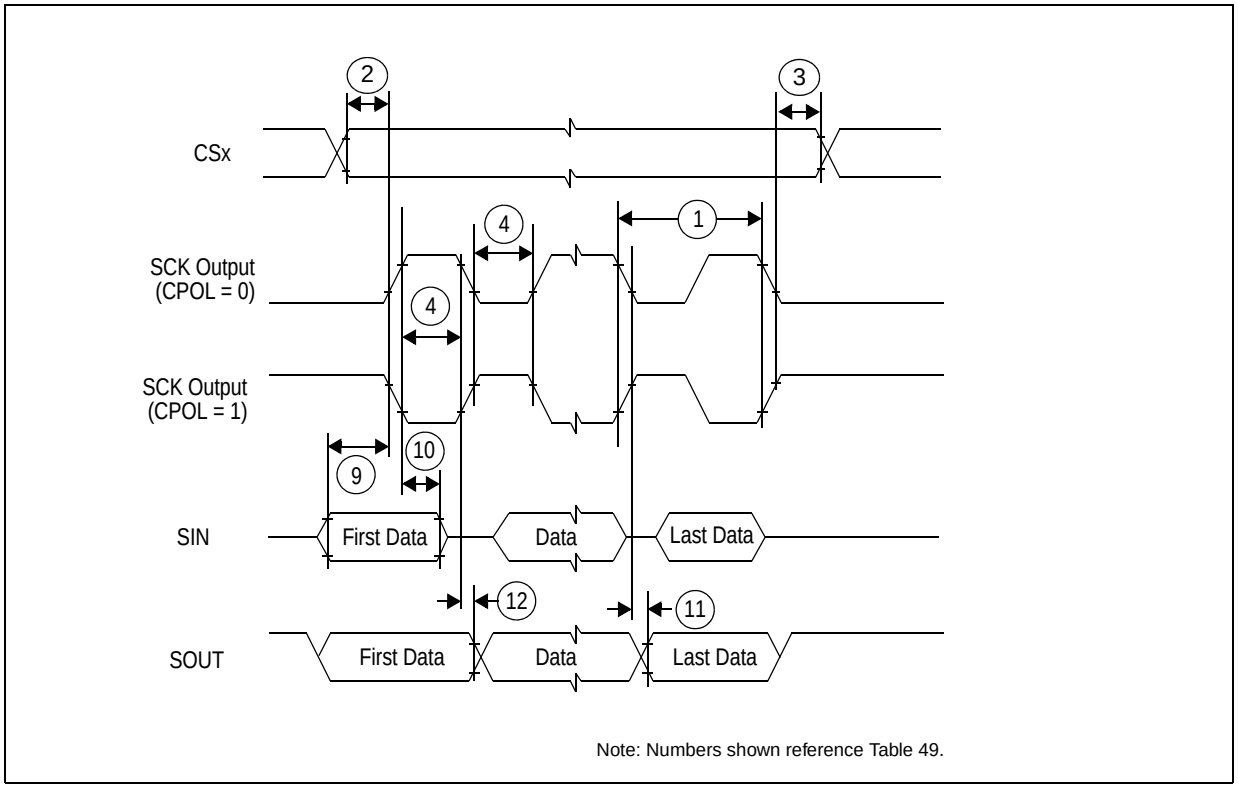

Figure 25. DSPI classic SPI timing–master, CPHA = 0

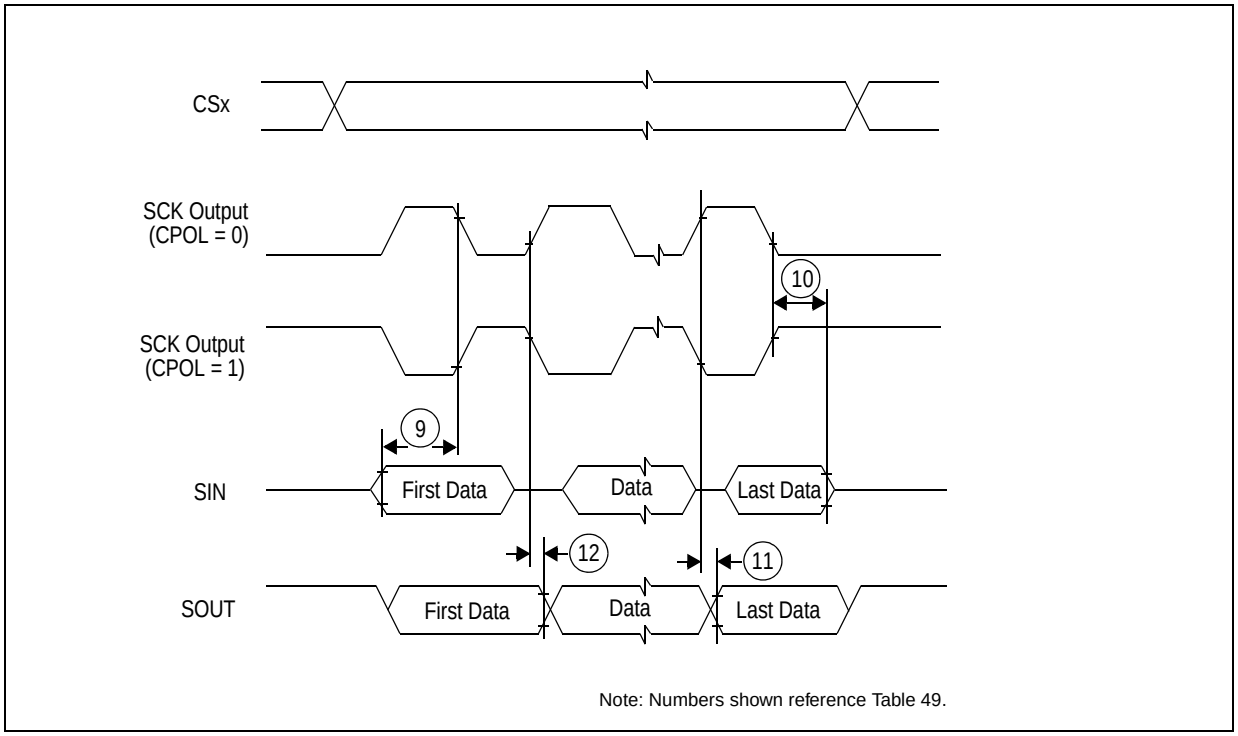

Figure 26. DSPI classic SPI timing–master, CPHA = 1

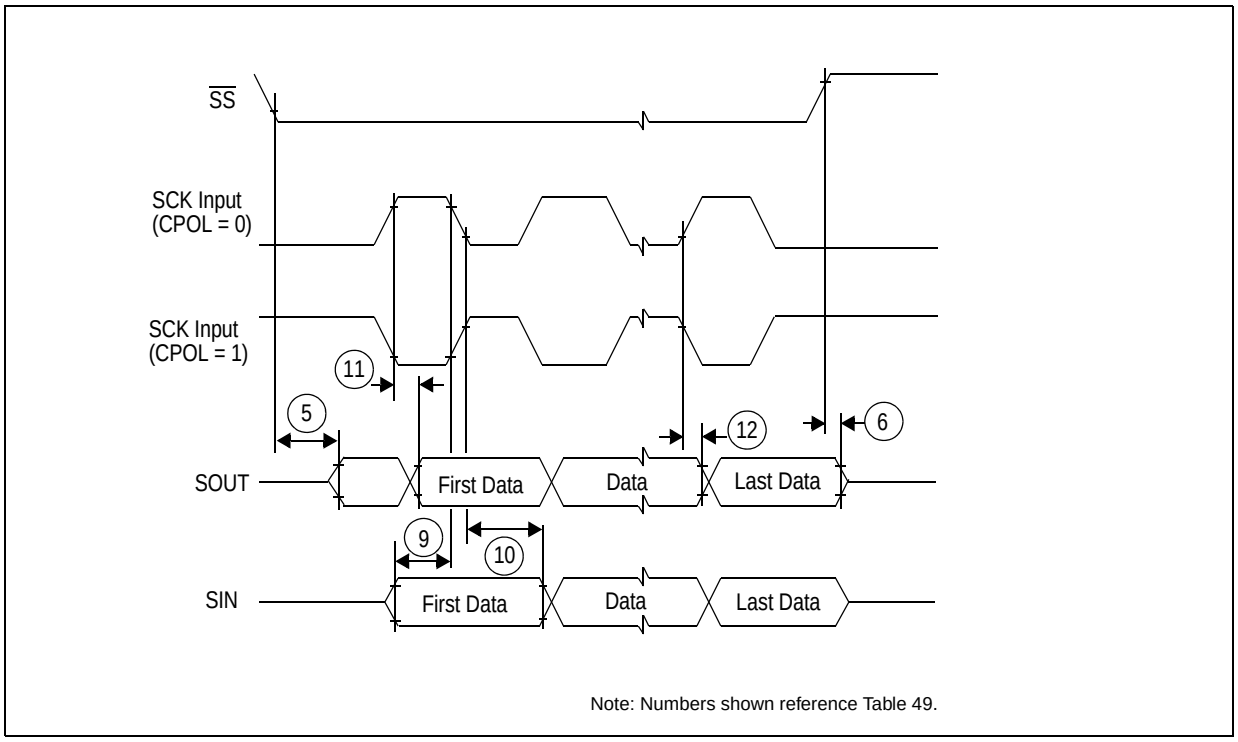

Figure 28. DSPI classic SPI timing–slave, CPHA = 1

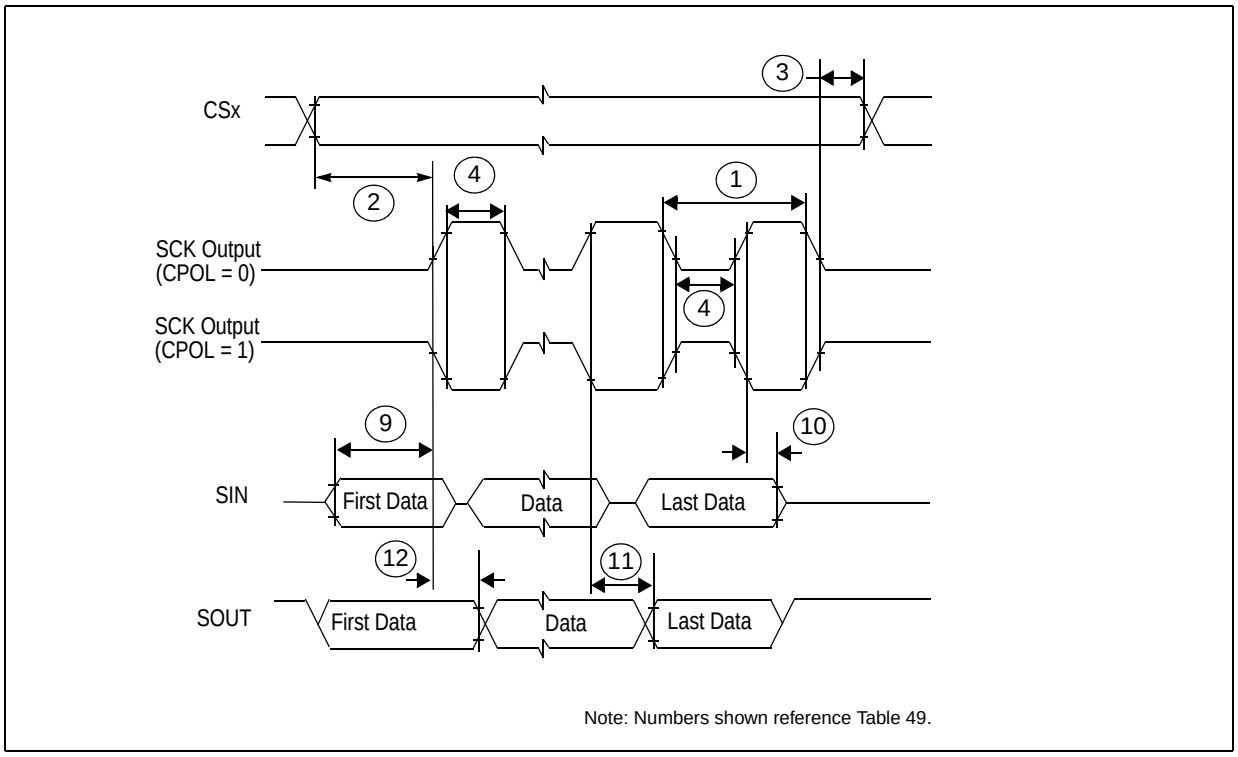

Figure 29. DSPI modified transfer format timing–master, CPHA = 0

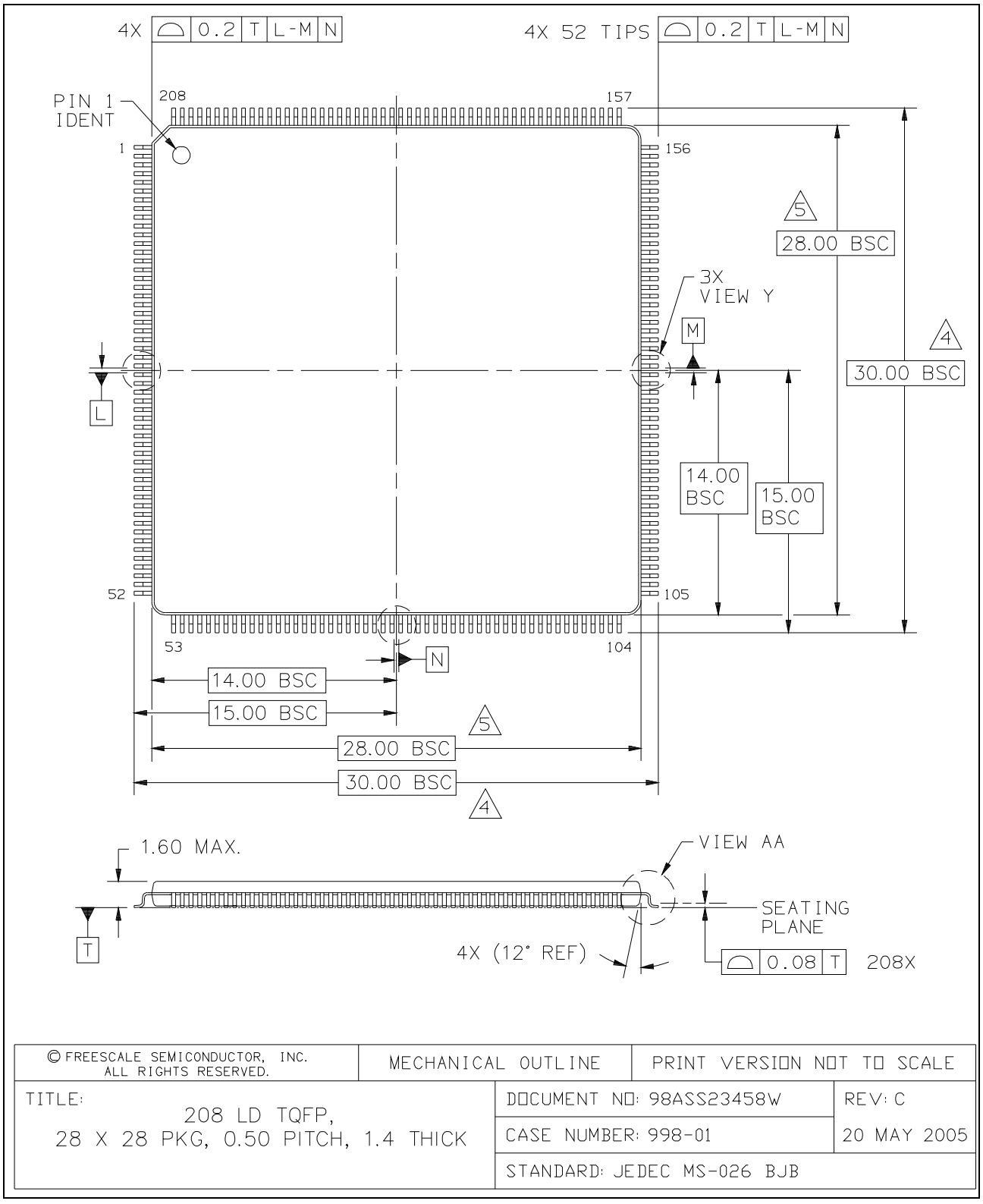

Figure 40. 208 LQFP mechanical drawing (Part 1 of 3)

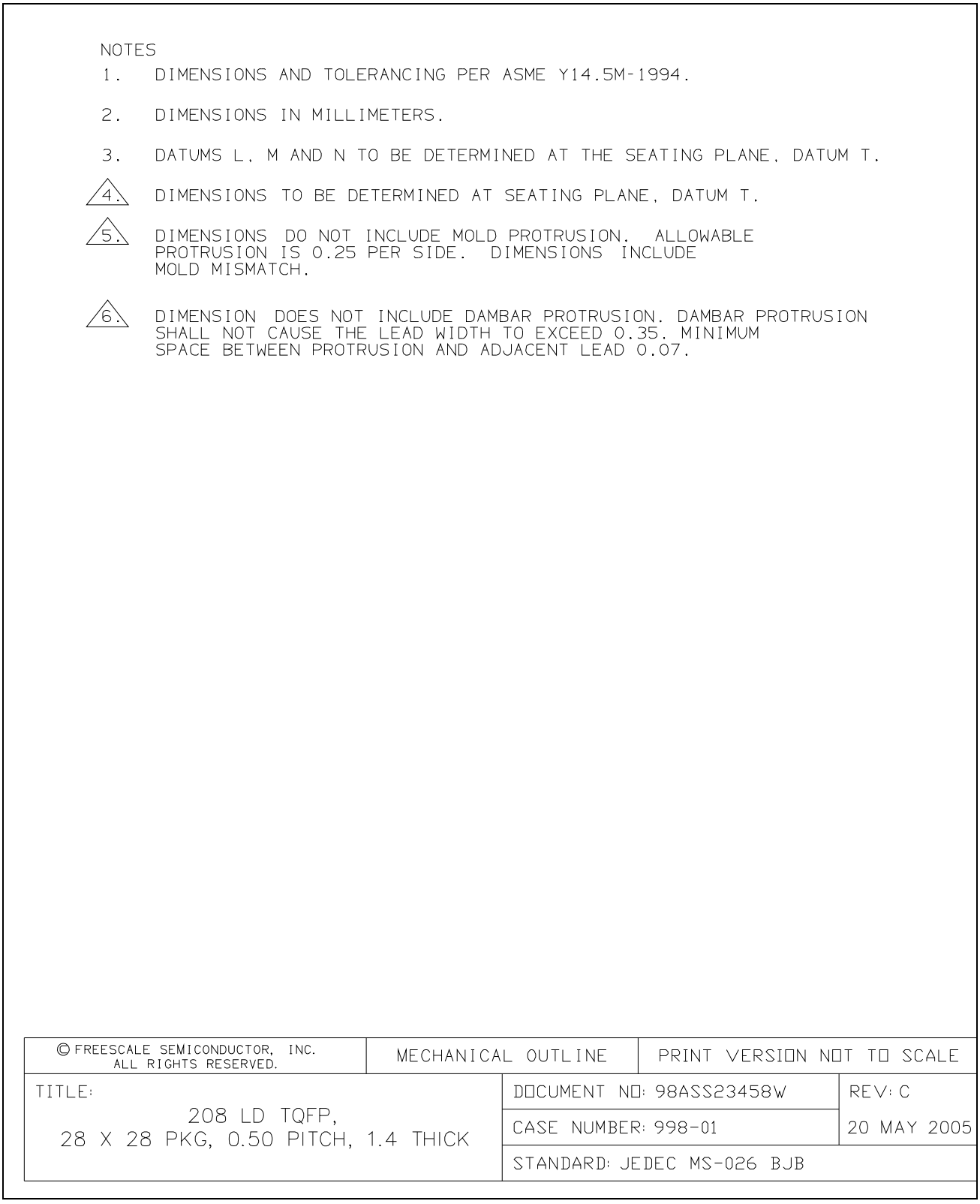

Figure 42. 208 LQFP mechanical drawing (Part 3 of 3)

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