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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d, e200z0h
Core Size	32-Bit Dual-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646ccf0mlu1r

Table 2 summarizes the functions of the blocks present on the MPC5646C.

Table 2. MPC5646C series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Cryptographic Security Engine (CSE)	Supports the encoding and decoding of any kind of data
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width
DMA Channel Multiplexer (DMAMUX)	Allows to route DMA sources (called slots) to DMA channels
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Fast Ethernet Controller (FEC)	Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks
Internal multiplexer (IMUX) SIUL subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	S	Tristate	97	117	M13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	101	123	L14
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	103	125	L15
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/S	Input, weak pull-up	154	178	B10
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/M	Tristate	149	173	D9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/S	Tristate	145	169	B11

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPI[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	87	103	P14
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPI[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	94	114	N16
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPI[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	95	115	M14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPI[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	96	116	M15
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	S	Tristate	100	120	L13
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	S	Tristate	102	124	K14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[62] CS1_1 E0UC[26] — FR_DBG[0] ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	104	126	K13

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M/S	Tristate	166	190	A6
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3 —	GPIO[121] — — — TCK	SIUL — — — JTAGC	I/O — — — I	S	Input, weak pull-up	155	179	A11
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3 —	GPIO[122] — — — TMS	SIUL — — — JTAGC	I/O — — — I	M/S	Input, weak pull-up	148	172	D10
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M/S	Tristate	140	164	A13
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M/S	Tristate	141	165	B12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M/S	Tristate	9	9	B1

2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$. All values need to be confirmed during device validation.
3 Analog filters are available on all wakeup lines.
4 The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 17 provides output driver characteristics for I/O pads when in FAST configuration.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}/V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V_{DD}	—	—	V
		C			I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	0.8V_{DD}	—	—	
		P			I_{OH} = –1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	

Table 17. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1,2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(3)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	

Table 18. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1,2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[4] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3 All values need to be confirmed during device validation.
4 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply is associated to a V_{DD}/V_{SS_HV} supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 19. I/O supplies

Package	I/O Supplies							
256 MAPBGA	Equivalent to 208-pin LQFP segment pad distribution + G6, G11, H11, J11							
208 LQFP	pin6 ($V_{DD\_HV\_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD\_HV\_A}$) pin28 (V_{SS_HV})	pin73 (V_{SS_HV}) pin75 ($V_{DD\_HV\_A}$)	pin101 ($V_{DD\_HV\_A}$) pin102 (V_{SS_HV})	pin132 (V_{SS_HV}) pin133 ($V_{DD\_HV\_A}$)	pin147 (V_{SS_HV}) pin148 ($V_{DD\_HV\_B}$)	pin174 (V_{SS_HV}) pin175 ($V_{DD\_HV\_A}$)	—

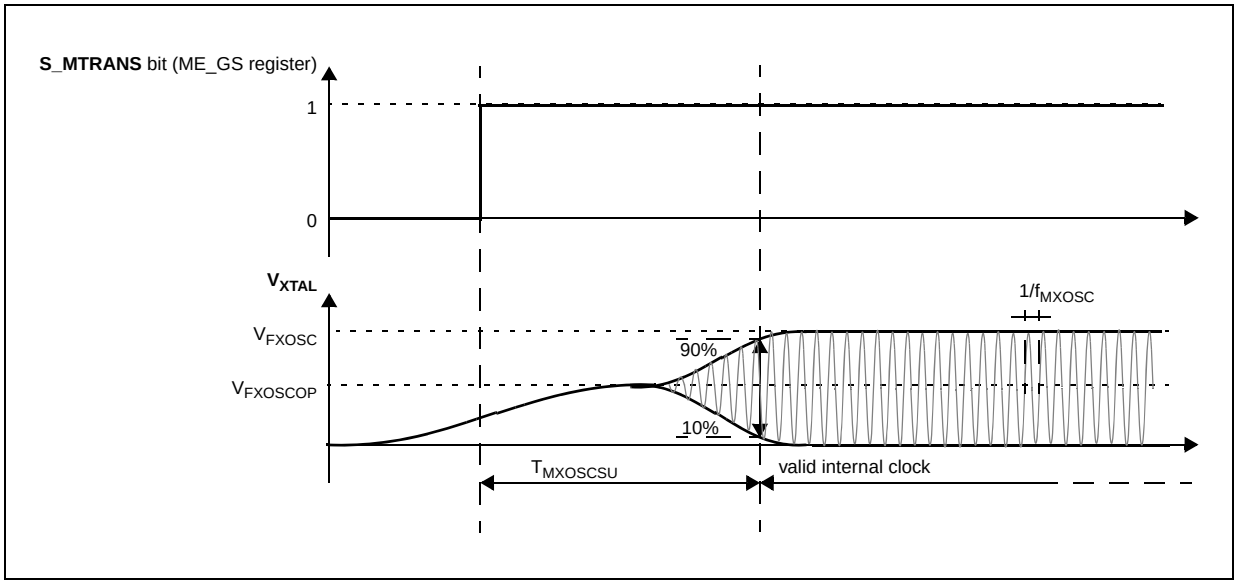


Figure 11. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	40.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%	4[3]	—	20[3]	mA/V
				V_{DD} = 5.0 V ± 10%	4[3]	—	20[3]	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	0.95	—	V
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	1.8		V
I_{FXOSC},[4]	CC	T	Fast external crystal oscillator consumption	V_{DD} = 3.3 V ± 10%, f_{OSC} = 40 MHz	—	2	2.2	mA
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 40 MHz	—	2.3	2.5	
				V_{DD} = 3.3 V ± 10%, f_{OSC} = 16 MHz	—	1.3	1.5	
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 16 MHz	—	1.6	1.8	
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	—	5	ms

Table 38. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle(3)	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2 All values need to be confirmed during device validation.
3 PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4 f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	100	nA
		D		T_A = 55 °C	—	—	200	nA
		D		T_A = 125 °C	—	—	1	µA

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

4.17.1.2 ADC electrical characteristics

Table 41. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 42. ADC conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1	—	$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 2%	MHz
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[4]	f_{ADC} = 32 MHz	500	—		ns
t_{ADC0_C}	CC	P	Conversion time[5,6]	f_{ADC} = 32 MHz	0.625	—		µs
				f_{ADC} = 30 MHz	0.700	—		
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the MPC5646C Reference Manual for details of this option and how to enable it.

Table 45. MII transmit signal timing[1]

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

NOTES:
1 Output pads configured with SRE = 0b11.

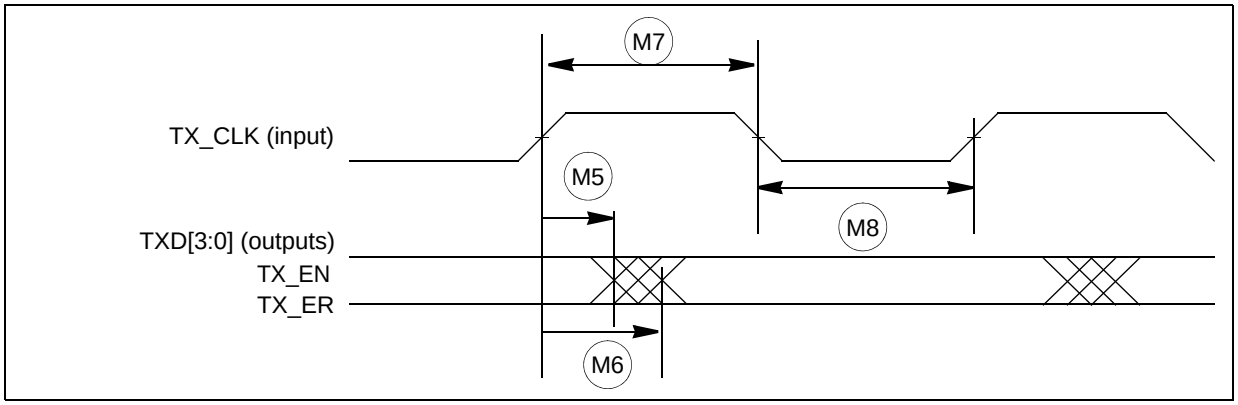


Figure 22. MII transmit signal timing diagram

4.18.3 MII Async Inputs Signal Timing (CRS and COL)

Table 46. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

NOTES:
1 Output pads configured with SRE = 0b11.

Table 48. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2]	Unit
						Typ	
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

NOTES:
1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2 f_{periph} is in absolute value.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

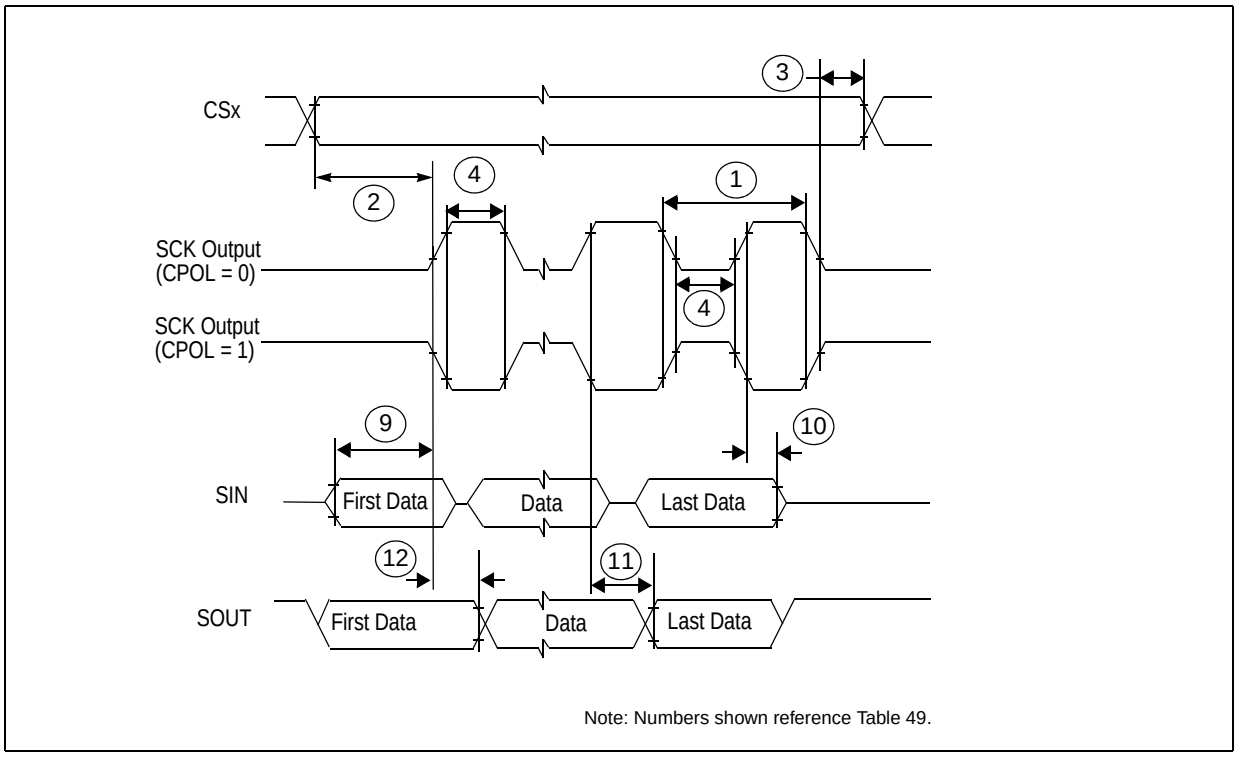
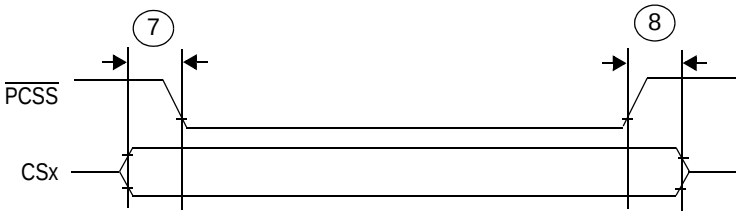


Figure 29. DSPI modified transfer format timing–master, CPHA = 0



Note: Numbers shown reference Table 49.

Figure 33. DSPI PCS strobe (PCSS) timing

4.19.3 Nexus characteristics

Table 50. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time[2]	t_{MCYC}	16.3	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, MSEO, EVTO Data Valid[3]	t_{MDOV}	–0.1	0.25	t_{MCYC}
4	EVTI Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
5	EVTO Pulse Width	t_{EVTOPW}	1		t_{MCYC}
6	TCK Cycle Time[4]	t_{TCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
9	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

NOTES:
1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DDE} = 4.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.
2. MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.
3. MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.
4. The system clock frequency needs to be three times faster than the TCK frequency.

Table 51. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

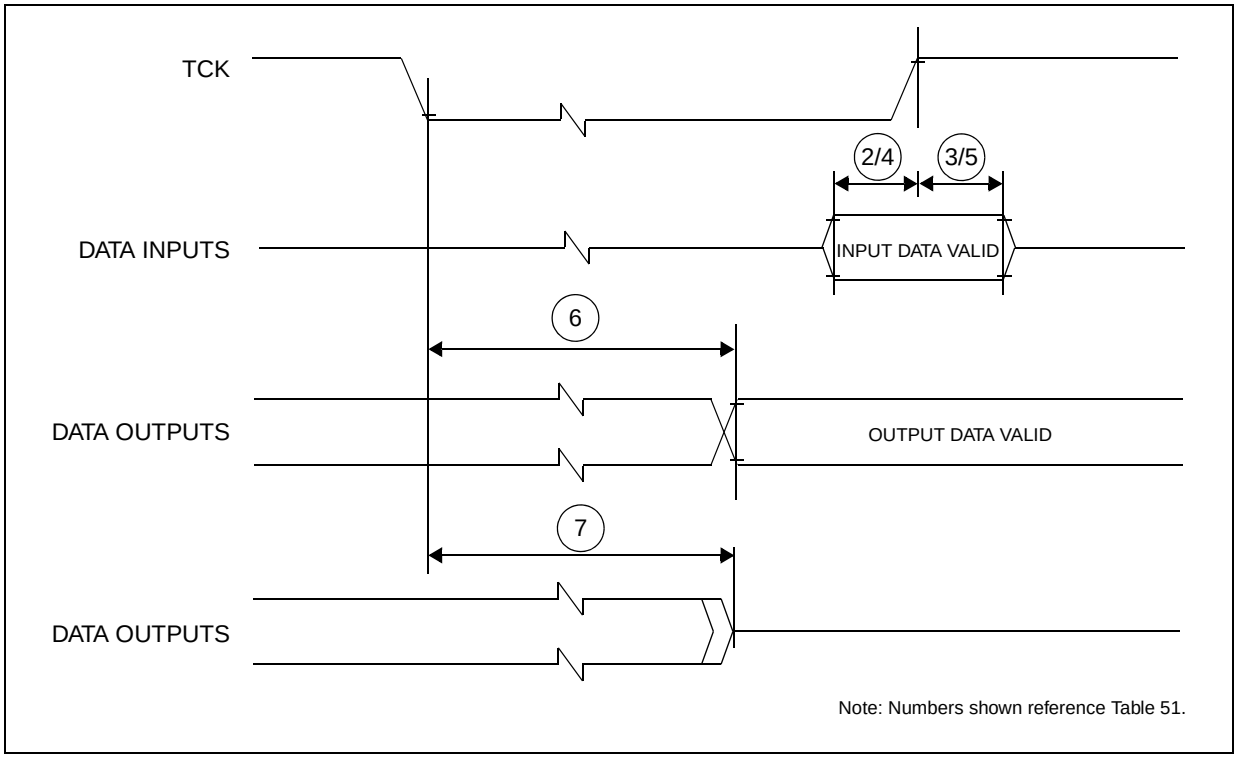


Figure 36. Timing diagram - JTAG boundary scan

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75								

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:		
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	3

Figure 39. 176 LQFP mechanical drawing (Part 3 of 3)

5.1.2 208 LQFP package mechanical drawing

7 Revision history

Table 52 summarizes revisions to this document.

Table 52. Revision history

Revision	Date	Changes
1	15 April 2010	Initial Release
2	17 August 2010	• Editing and formatting updates throughout the document. • Updated Voltage regulator capacitance connection figure. • Added a new sub-section "V_{DD_BV} Options" • Program and erase specifications: -Updated Tdwprogram TYP to 22 us -Updated T128Kpperase Max to 5000 ms -Added t_{ESUS} parameter • Added 208 MAPBGA thermal characteristics • Added recommendation in the Voltage regulator electrical characteristics section. • Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same. • Added new sections - Pad types, System pins and functional ports • Updated TYP numbers in the Flash program and erase specifications table • Added a new table: Program and erase specifications (Data Flash) • Flash read access timing table: Added Data flash memory numbers • Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter • Updated feature list. • MPC5646C 3M family comparison table: Updated ADC channels and added ADC footnotes. • MPC5646C 3M block diagram: Updated ADC channels and added legends. • MPC5646C 3M series block summary: Added new blocks. • Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins. • Electrical Characteristics: Replaced VSS with VSS_HV throughout the section. • Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0". • Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables. • LQFP thermal characteristics section: Updated numbers for LQFP packages. • Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments. • Code flash memory—Program and erase specifications: Updated tESRT to 20 ms. • ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document. • DSPI characteristics section: Replaced PCSx with CSx in all figures and tables.