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What is "Embedded - Microcontrollers"?

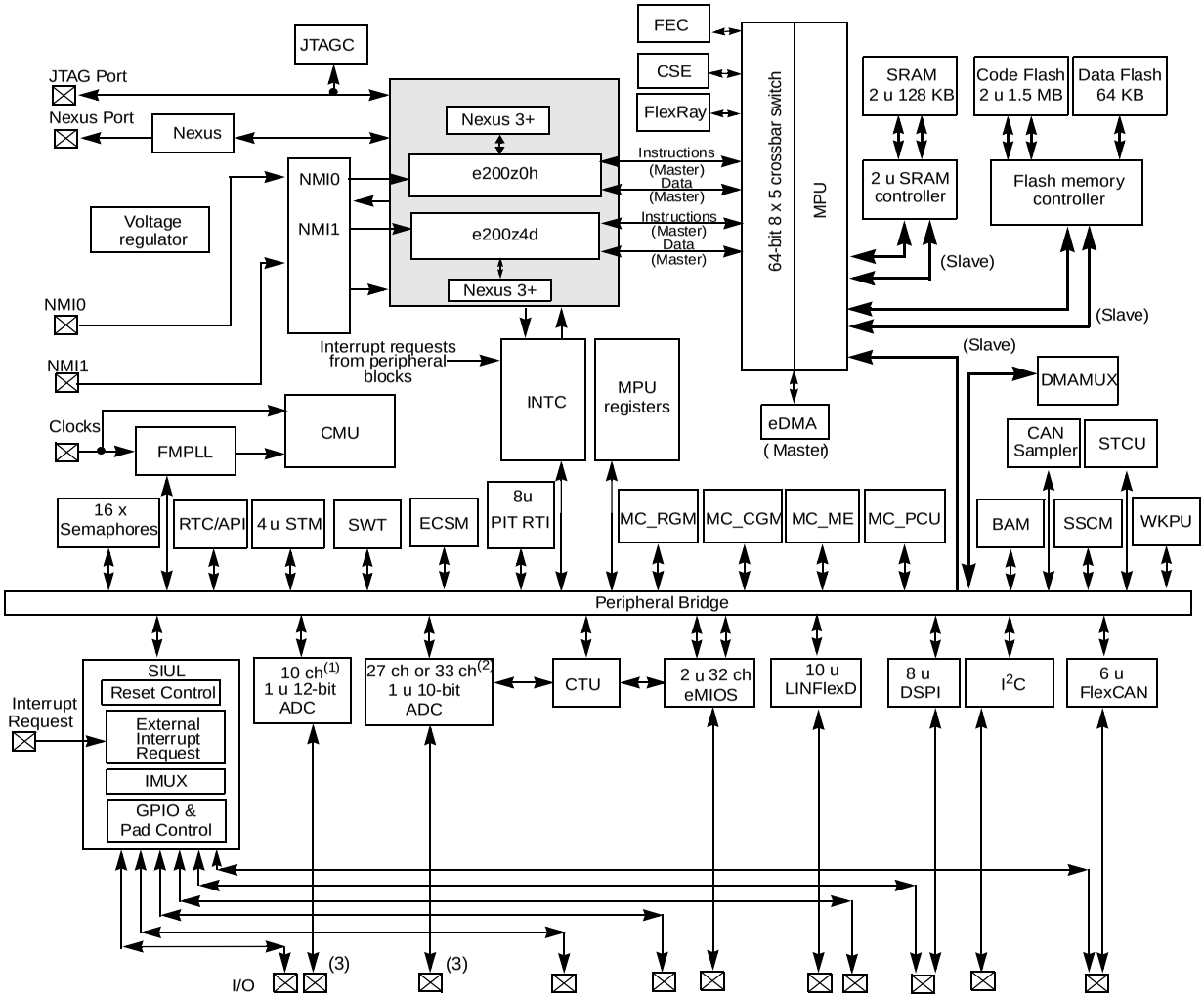
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4d, e200z0h
Core Size	32-Bit Dual-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5646ccf0vlt1

2 Block diagram

Figure 1shows the detailed block diagram of the MPC5646C.



Legend:

ADC	Analog-to-Digital Converter	JTAGC	JTAG controller
BAM	Boot Assist Module	LINFlexD	Local Interconnect Network Flexible with DMA support
CSE	Cryptographic Services Engine	MC_ME	Mode Entry Module
CAN	Controller Area Network (FlexCAN)	MC_CGM	Clock Generation Module
CMU	Clock Monitor Unit	MC_PCU	Power Control Unit
CTU	Cross Triggering Unit	MC_RGM	Reset Generation Module
DMAMUX	DMA Channel Multiplexer	MPU	Memory Protection Unit
DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface
eDMA	enhanced Direct Memory Access	NMI	Non-Maskable Interrupt
FlexCAN	Controller Area Network controller modules	PIT_RTI	Periodic Interrupt Timer with Real-Time Interrupt
FEC	Fast Ethenet Controller	RTC/API	Real-Time Clock/ Autonomous Periodic Interrupt
eMIOS	Enhanced Modular Input Output System	SIUL	System Integration Unit Lite
ECSM	Error Correction Status Module	SRAM	Static Random-Access Memory
FMPLL	Frequency-Modulated Phase-Locked Loop	SSCM	System Status Configuration Module
FlexRay	FlexRay Communication Controller	STM	System Timer Module
I2C	Inter-integrated Circuit Bus	SWT	Software Watchdog Timer
IMUX	Internal Multiplexer	STCU	Self Test Control Unit
INTC	Interrupt Controller	WKPU	Wakeup Unit

Notes:
1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
3) 16 x precision channels (ANP) are mapped on input only I/O cells.

Figure 1. MPC5646C block diagram

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	S	Tristate	97	117	M13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	101	123	L14
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	103	125	L15
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/S	Input, weak pull-up	154	178	B10
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/M	Tristate	149	173	D9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/S	Tristate	145	169	B11

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M/S	Tristate	42	50	N2
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — CAN2RX CAN3RX WKPU[22]	SIUL eMIOS_1 DSPI_0 — FlexCAN_2 FlexCAN_3 WKPU	I/O I/O O — I I I	S	Tristate	41	49	M4
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/S	Tristate	46	54	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/S	Tristate	43	51	P1

Table 8. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{RC_CTRL}[2]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$[3]	$V_{DD\_HV\_A}$ 0.3	$V_{DD\_HV\_A}$+0.3	
$V_{DD\_HV\_ADC1}$[4]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$[2]	$V_{DD\_HV\_A}$ 0.3	$V_{DD\_HV\_A}$+0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A/HV\_B}$	$V_{DD\_HV\_A/HV\_B}$ 0.3	$V_{DD\_HV\_A/HV\_B}$ +0.3	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}[5]	SR	Sum of all the static I/O current within a supply segment ($V_{DD\_HV\_A}$ or $V_{DD\_HV\_B}$)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	SR	Storage temperature	—	–55[6]	150	°C

NOTES:
1. $V_{DD\_HV\_B}$ can be independently controlled from $V_{DD\_HV\_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±300 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up[8]	—	—	0.5	V/µs
			—	0.5	—	V/min
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz 2%	–40	125	°C
T_J	SR	Junction temperature under bias	—	40	150	

NOTES:
1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A} + 0.3 = 6.2$ V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
$V_{DD\_HV\_B}$	SR	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in Section 3, ”Package pinouts and signal descriptions” for the list of channels operating in $V_{DD\_HV\_B}$ domain)	—	3.0	3.6	V

4.5.2 Power considerations

The average chip-junction temperature, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{TJA}) \quad \text{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

R_{TJA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{TJA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

4.6 I/O pad electrical characteristics

4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.
- Low power pads—These pads are active in standby mode for wakeup source.

Also, medium/slow and fast/medium pads are available in design which can be configured to behave like a slow/medium and medium/fast pads depending upon the slew-rate control.

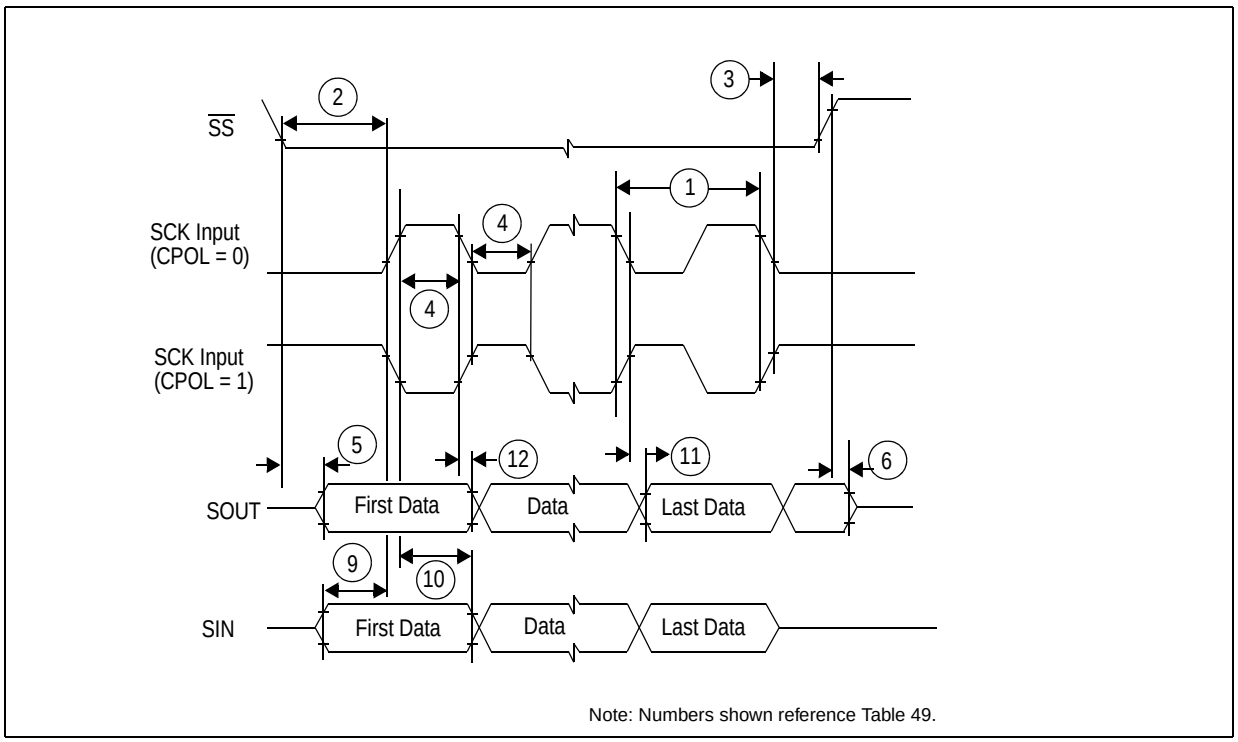


Figure 27. DSPI classic SPI timing–slave, CPHA = 0

Table 51. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

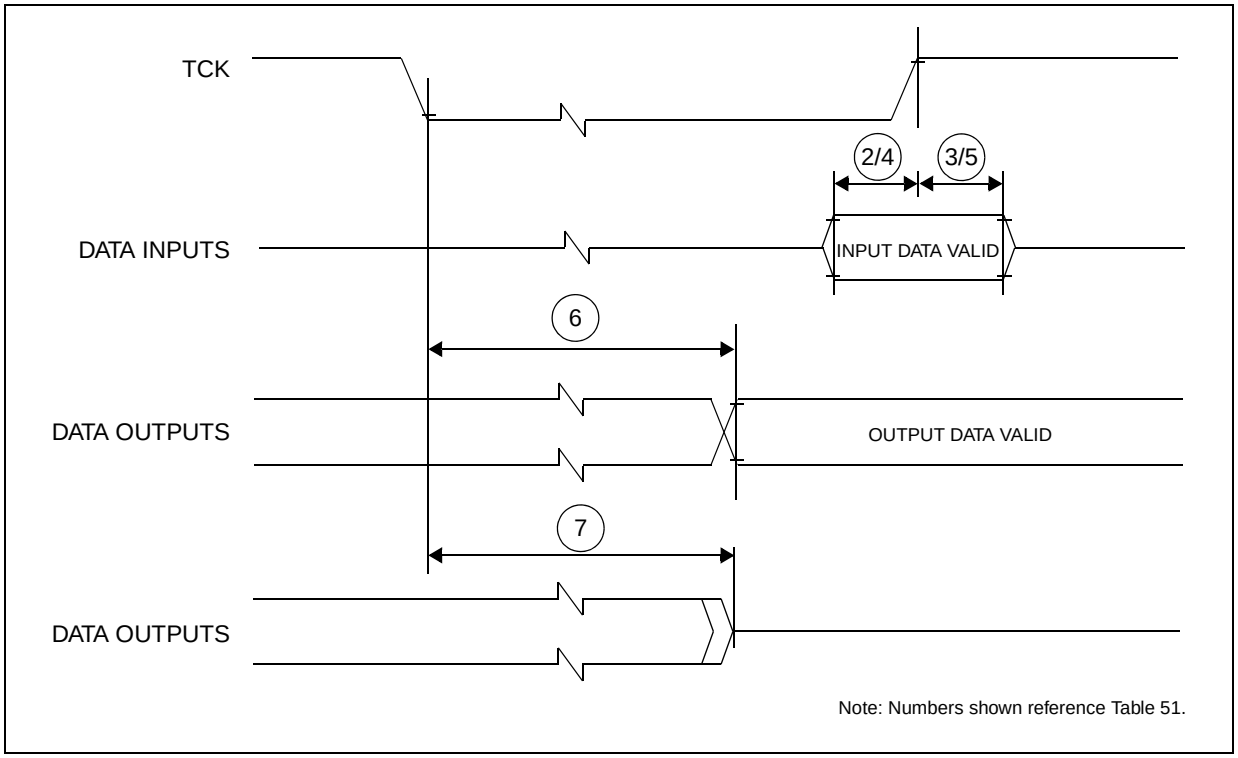


Figure 36. Timing diagram - JTAG boundary scan

5 Package characteristics

5.1 Package mechanical data

5.1.1 176 LQFP package mechanical drawing

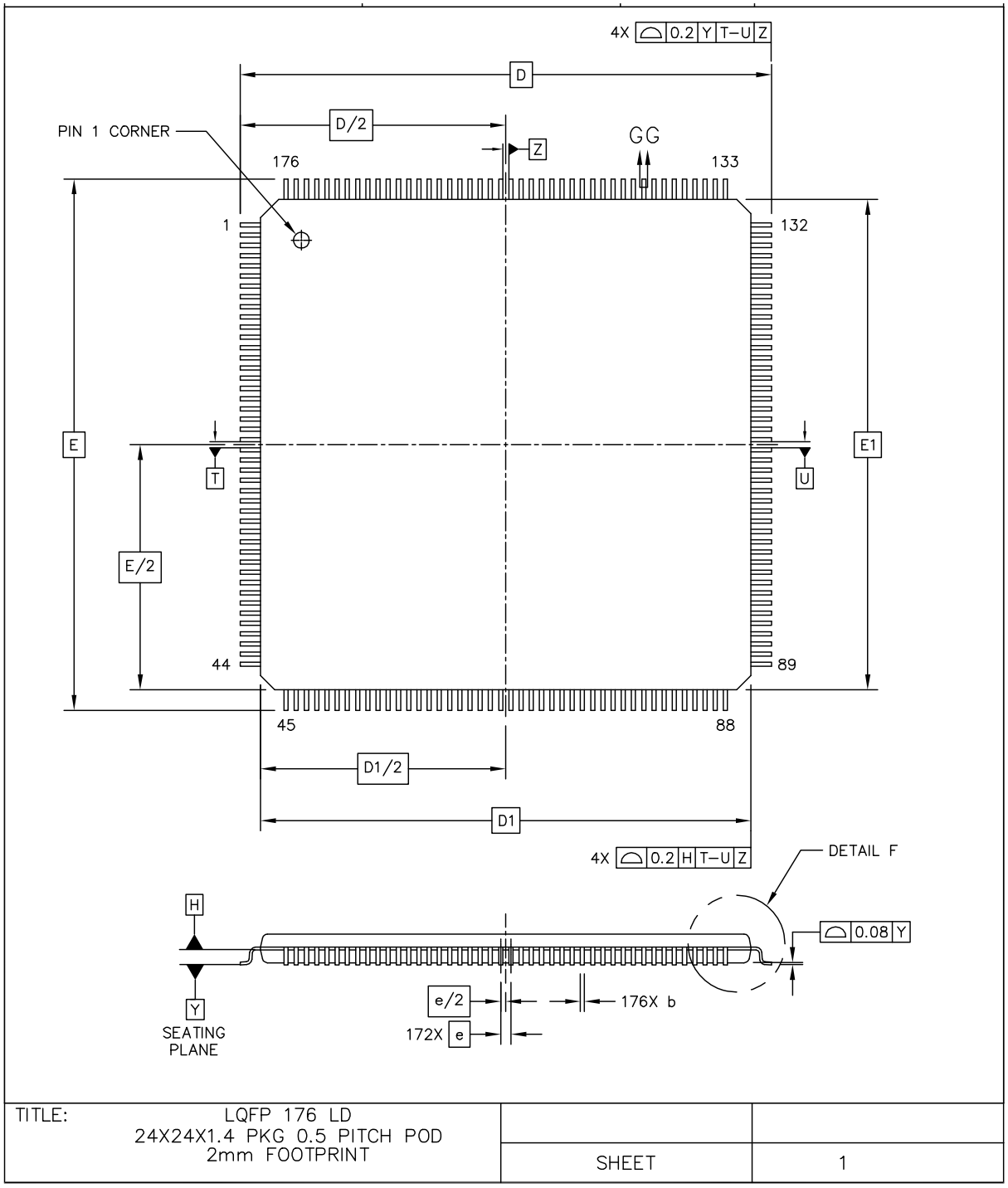


Figure 37. 176 LQFP mechanical drawing (Part 1 of 3)

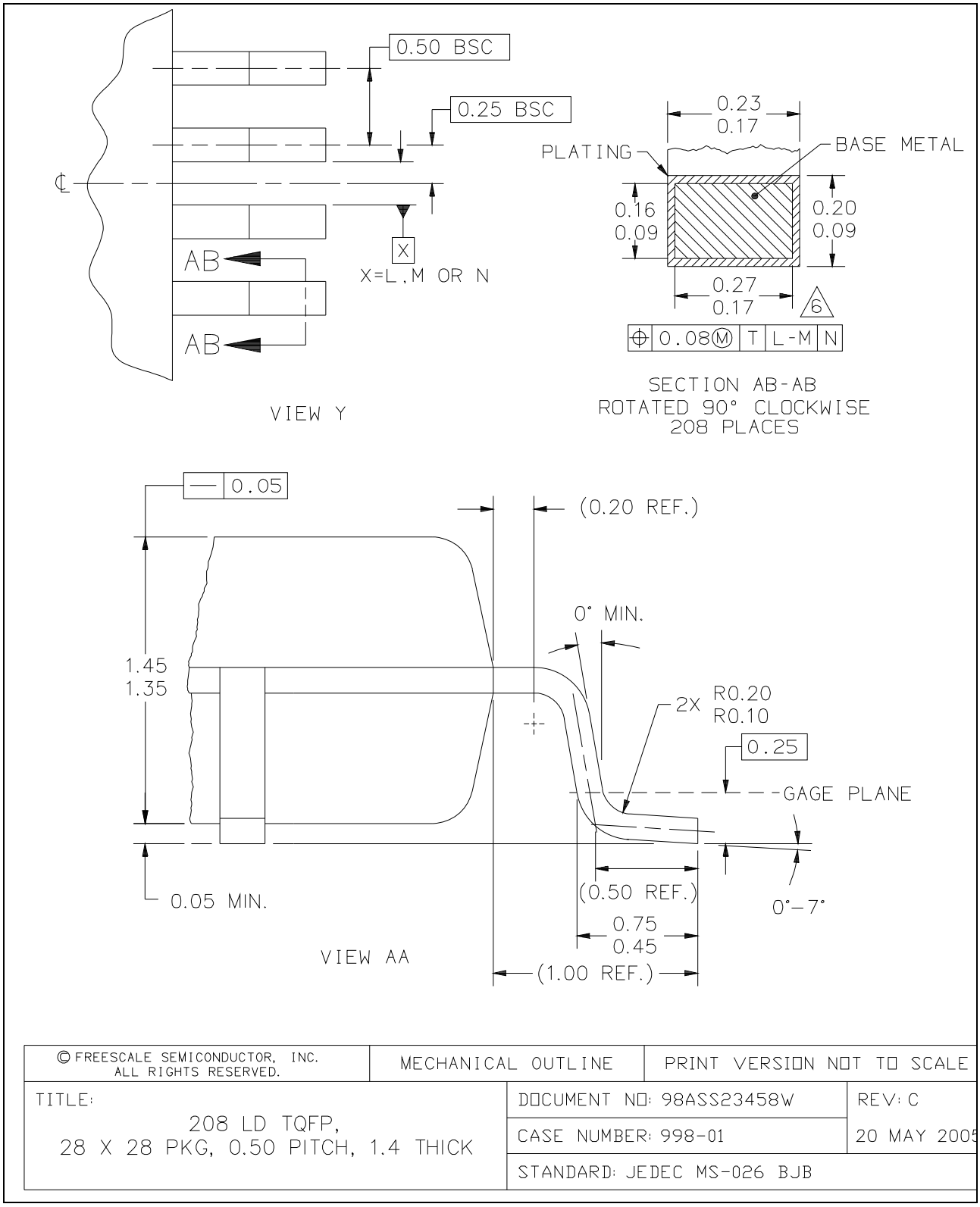
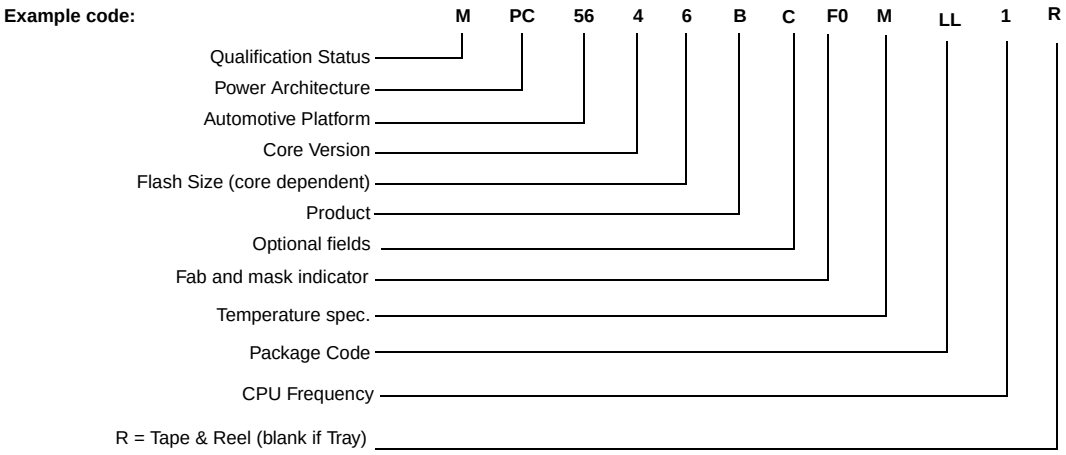


Figure 41. 208 LQFP mechanical drawing (Part 2 of 3)

6 Ordering information



Qualification Status
M = MC status
S = Auto qualified
P = PC status

PC = Power Architecture

Automotive Platform
56 = Power Architecture in 90 nm

Core Version
4 = e200z4d core version (highest core version in the case of multiple cores)

Flash Memory Size
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

Product Version
B = Body
C = Gateway

Optional fields
C = CSE module available
Blank = none of these options available

Fab and mask version indicator
F = ATMC
0 = First version of the mask

Temperature spec.
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C

Package Code
LU = 176 LQFP
LT = 208 LQFP
MJ = 256 MAPBGA

CPU Frequency
1 = e200z4d operates up to 120 MHz
8 = e200z4d operates up to 80 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Note: Not all options are available on all devices. Refer to Table 1, which shows the orderable part numbers for MPC564xx.

Figure 45. Orderable parts