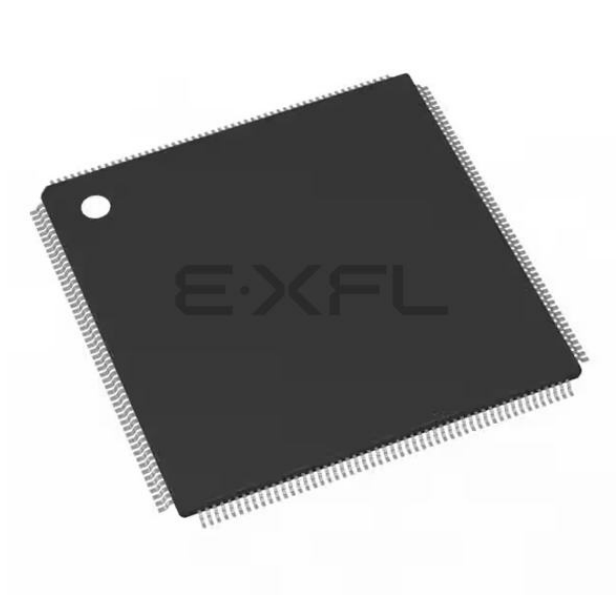

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Supplier Device Package	208-TQFP (28x28)
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Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — — —	GPIO[7] E0UC[7] LIN3TX — RXD[2] EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlexD_3 — FEC SIUL ADC_1	I/O I/O O — I I I	M/S	Tristate	128	152	C15
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — — —	GPIO[8] E0UC[8] E0UC[14] — RXD[1] EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — FEC SIUL MC_RGM LINFlexD_3	I/O I/O I/O — I I I I	M/S	Input, weak pull-up	129	153	B16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 — —	GPIO[9] E0UC[9] — CS2_1 RXD[0] FAB	SIUL eMIOS_0 — DSPI1 FEC MC_RGM	I/O I/O — O I I	M/S	Pull-down	130	154	B15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 — — —	GPIO[10] E0UC[10] SDA LIN2TX COL ADC1_S[2] SIN_1	SIUL eMIOS_0 I^2C LINFlexD_2 FEC ADC_1 DSPI_1	I/O I/O I/O O I I I	M/S	Tristate	131	155	A15
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — — —	GPIO[11] E0UC[11] SCL — RX_ER EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C — FEC SIUL LINFlexD_2 ADC_1	I/O I/O I/O — I I I I	M/S	Tristate	132	156	B14
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	53	69	P6

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M/S	Tristate	52	66	R5
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M/S	Tristate	50	58	P4
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M/S	Tristate	48	56	R2
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlexD_0	I/O O I/O I	M/S	Tristate	39	39	L3
PB[1]	PCR[17]	AF0 AF1 AF2 — — —	GPIO[17] — E0UC[31] LIN0RX WKPU[4] CAN0RX	SIUL — eMIOS_0 LINFlexD_0 WKPU FlexCAN_0	I/O — I/O I I I	S	Tristate	40	40	M2
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlexD_0 I^2C eMIOS_0	I/O O I/O I/O	M/S	Tristate	176	208	A2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11] LIN0RX	SIUL eMIOS_0 I^2C — WKPU LINFlexD_0	I/O I/O I/O — I I	S	Tristate	1	1	D4
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — —	GPI[20] — — — ADC0_P[0] ADC1_P[0]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	88	104	T16

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[46] E0UC[14] SCK_2 — FR_DBG[2] EIRQ[8]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	3	3	B2
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 ALT4	GPIO[47] E0UC[15] CS0_2 — FR_DBG[3] EIRQ[20]	SIUL eMIOS_0 DSPI_2 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	4	4	A1
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPI[48] — — — ADC0_P[4] ADC1_P[4] WKPU[27]	SIUL — — — ADC_0 ADC_1 WKPU	I — — — I I I	I	Tristate	77	93	R12

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[63] CS2_1 E0UC[27] — FR_DBG[1] ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	106	128	J13
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX WKPU[6]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	18	18	G2
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M/S	Tristate	20	20	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[66] E0UC[18] — — FR_A_TX_EN SIN_1 EIRQ[21]	SIUL eMIOS_0 — — Flexray DSPI_1 SIUL	I/O I/O — — O I I	M/S	Tristate	156	180	A7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3 — —	GPIO[67] E0UC[19] SOUT_1 — FR_A_RX WKPU[29]	SIUL eMIOS_0 DSPI_1 — Flexray WKPU	I/O I/O O — I I	M/S	Tristate	157	181	A10
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[68] E0UC[20] SCK_1 — FR_B_TX EIRQ[9]	SIUL eMIOS_0 DSPI_1 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	160	184	A8
PE[5]	PCR[69]	AF0 AF1 AF2 AF3 — —	GPIO[69] E0UC[21] CS0_1 MA[2] FR_B_RX WKPU[30]	SIUL eMIOS_0 DSPI_1 ADC_0 Flexray WKPU	I/O I/O I/O O I I	M/S	Tristate	161	185	B8

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKPU[14]	SIUL eMIOS_0 DSPI_1 — LINFlexD_3 WKPU	I/O I/O O — I I	S	Tristate	25	25	H3
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — — —	GPIO[76] — E1UC[19] — CRS SIN_2 EIRQ[11] ADC1_S[7]	SIUL — eMIOS_1 — FEC DSPI_2 SIUL ADC_1	I/O — I/O — I I I I	M/S	Tristate	133	157	C14

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M/S	Tristate	10	10	C1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M/S	Tristate	8	8	E3
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

4 This voltage is internally generated by the device and no external voltage should be supplied.

5 100 nF capacitance needs to be provided between $V_{DD\_HV\_(ADC0/ADC1)}$/$V_{SS\_HV\_(ADC0/ADC1)}$ pair.

6 Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.

7 PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.

8 Guaranteed by device validation.

NOTE

SRAM retention guaranteed to LVD levels.

4.5 Thermal characteristics

4.5.1 Package thermal characteristics

Table 11. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value[3]			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[4]	Single-layer board—1s	176	—	—	38[5]	°C/W
					208	—	—	41[6]	°C/W
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[7]	Four-layer board—2s2p[7]	176	—	—	31	°C/W
					208	—	—	34	°C/W

NOTES:

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C.

3 All values need to be confirmed during device validation.

4 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

5 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6.

6 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-2 and JESD51-6

7 Junction-to-Board thermal resistance determined per JEDEC JESD51-8.

Table 12. 256 MAPBGA thermal characteristics[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	43[2]	°C/W
				Four-layer board—2s2p	26[3]	

NOTES:

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-ambient thermal resistance determined per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-6 with the board horizontal.

4.5.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

4.6 I/O pad electrical characteristics

4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.
- Low power pads—These pads are active in standby mode for wakeup source.

Also, medium/slow and fast/medium pads are available in design which can be configured to behave like a slow/medium and medium/fast pads depending upon the slew-rate control.

Table 20. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1,2]	Value[3]			Unit
					Min	Typ	Max	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65[4]	

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. All values need to be confirmed during device validation.
4. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

4.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

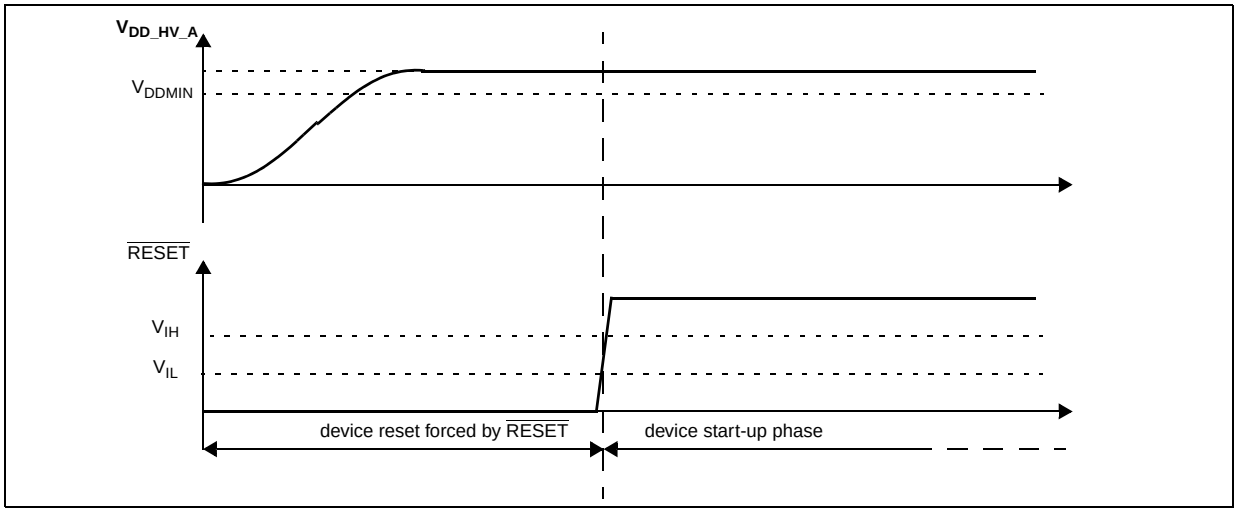


Figure 6. Start-up reset requirements

3 Data based on characterization results, not tested in production.

4 f_{CPU} 120 MHz + 2% can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

4.10.3 Flash memory start-up/switch-off timings

Table 30. Start-up time/Switch-off time

Symbol		C	Parameter		Conditions[1]	Value			Unit
						Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	D	Delay for flash memory module to exit reset mode	Code flash memory	—	—	—	125	µs
				Data flash memory		—	—		
$T_{FLALPEXIT}$	CC	T	Delay for flash memory module to exit low-power mode	Code flash memory	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for flash memory module to exit power-down mode	Code flash memory	—	—	—	30	
				Data flash memory		—	—		
$T_{FLALPENTRY}$	CC	T	Delay for flash memory module to enter low-power mode	Code flash memory	—	—	—	0.5	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

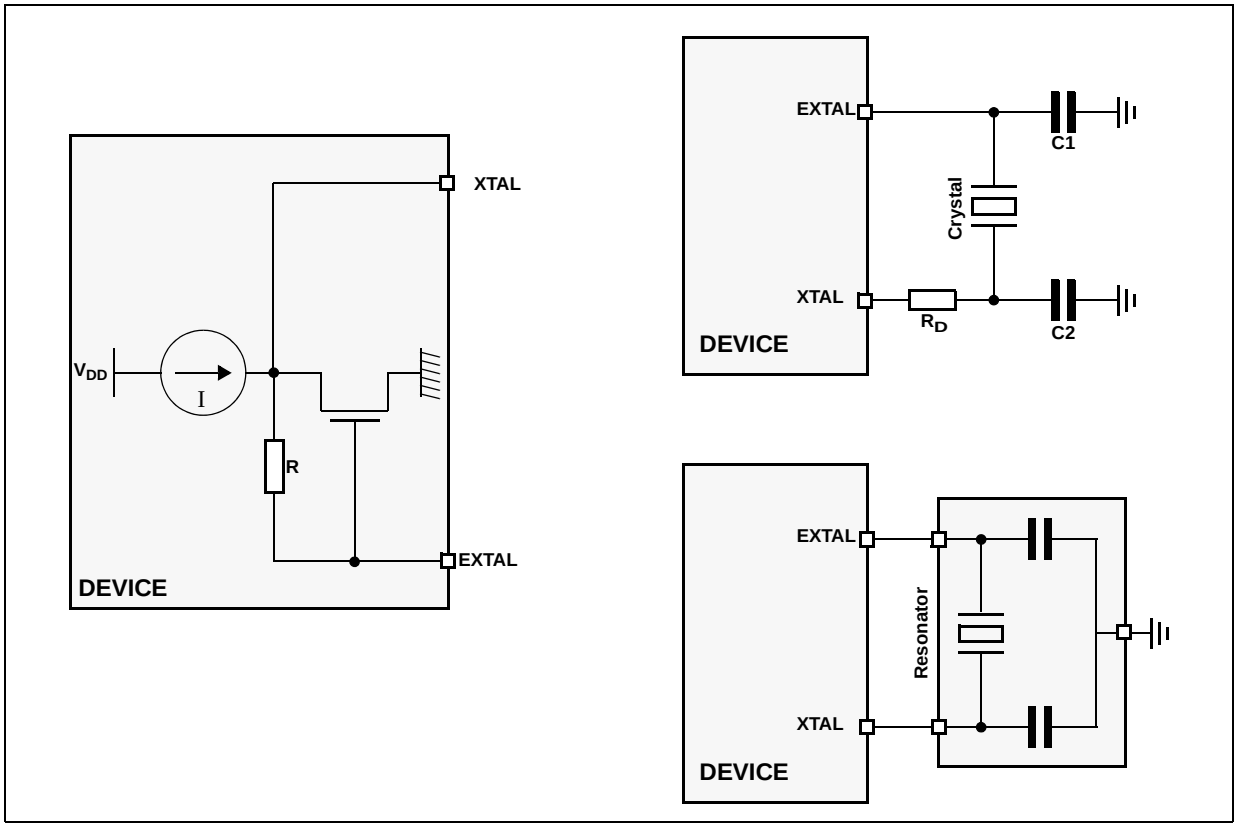


Figure 10. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 34. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00
40	NX5032GA	50	6.18	2.56	8	3.49

NOTES:
1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

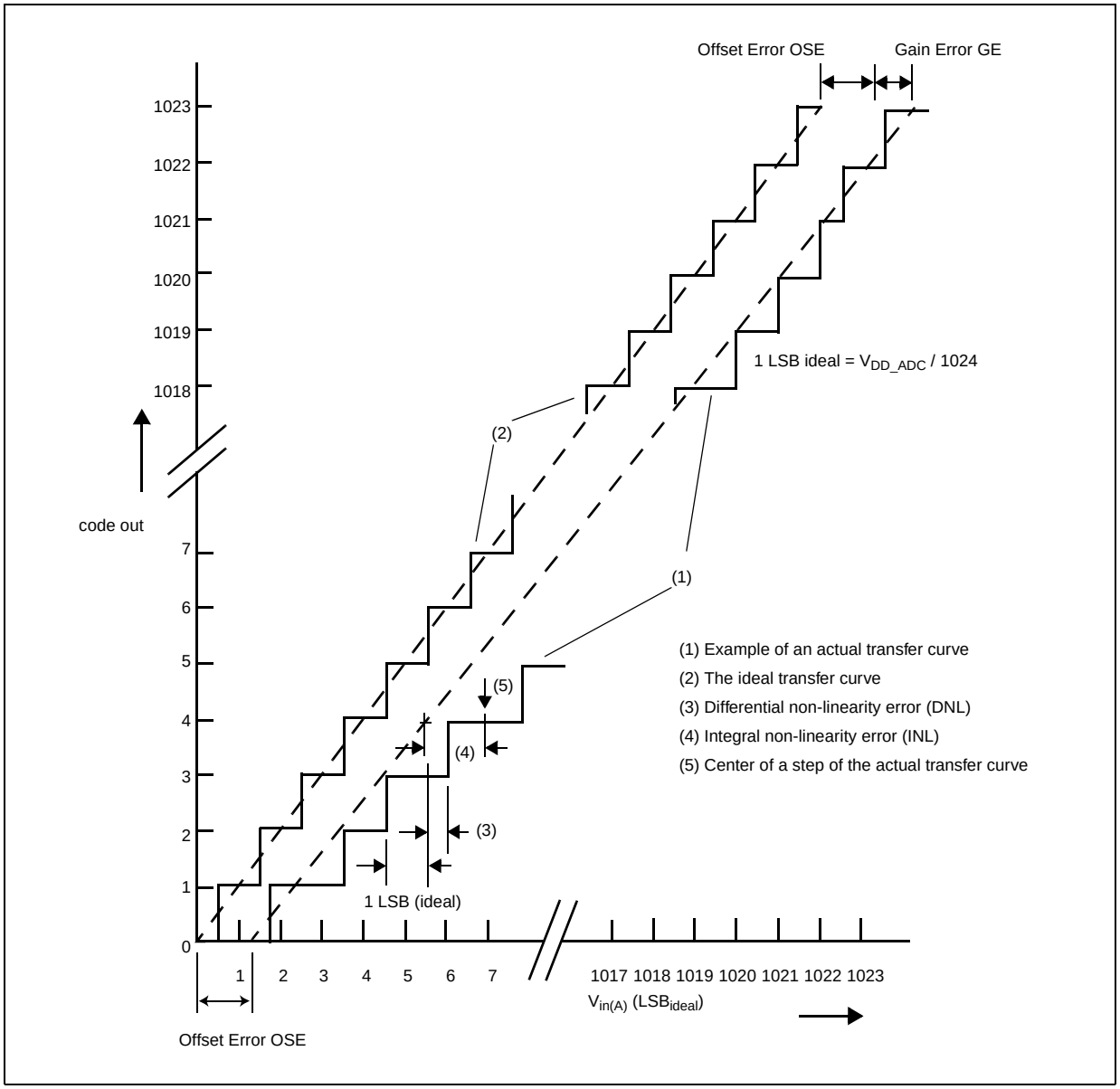


Figure 15. ADC_0 characteristic and error definitions

4.17.1.1 Input impedance and ADC accuracy

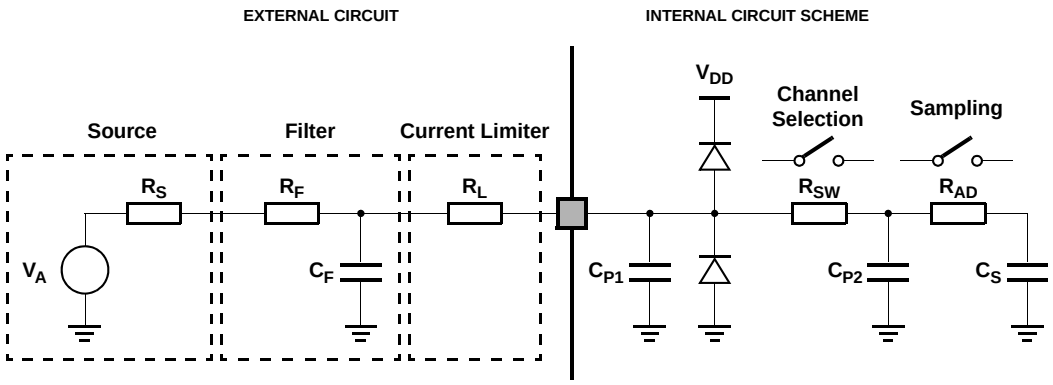
To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device, can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source. A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with $CS+Cp_2$ equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*($CS+Cp_2$)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $CS+Cp_2$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the following relation

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.



R_S	Source Impedance
R_F	Filter Resistance
C_F	Filter Capacitance
R_L	Current Limiter Resistance
R_{SW}	Channel Selection Switch Impedance
R_{AD}	Sampling Switch Impedance
C_P	Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S	Sampling Capacitance

Figure 16. Input equivalent circuit (precise channels)

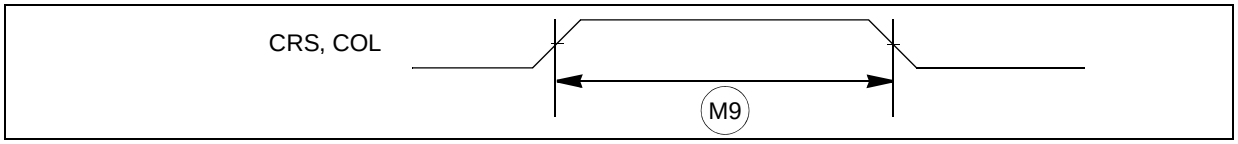


Figure 23. MII async inputs timing diagram

4.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 47. MII serial management channel timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

NOTES:
1 Output pads configured with SRE = 0b11.

4.19.2 DSPI characteristics

Table 49. DSPI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note[1]	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)[4]	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns

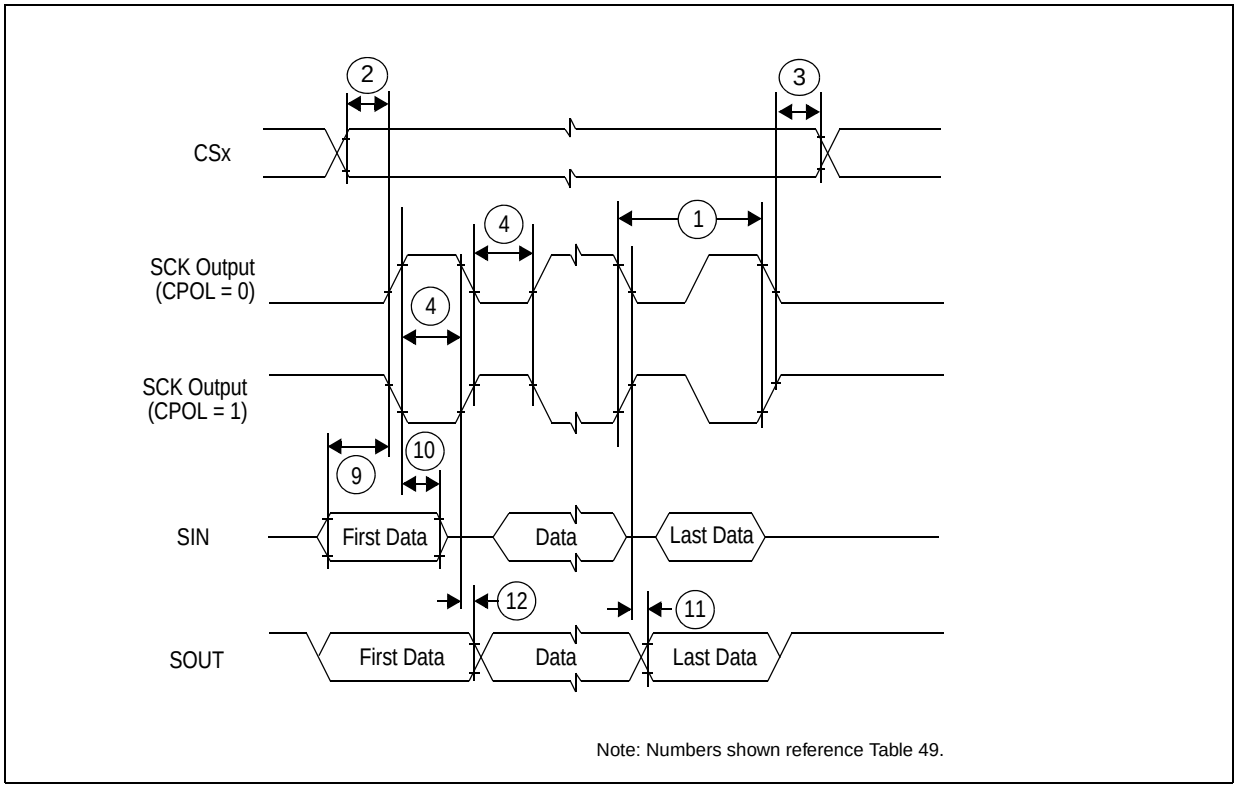


Figure 25. DSPI classic SPI timing–master, CPHA = 0

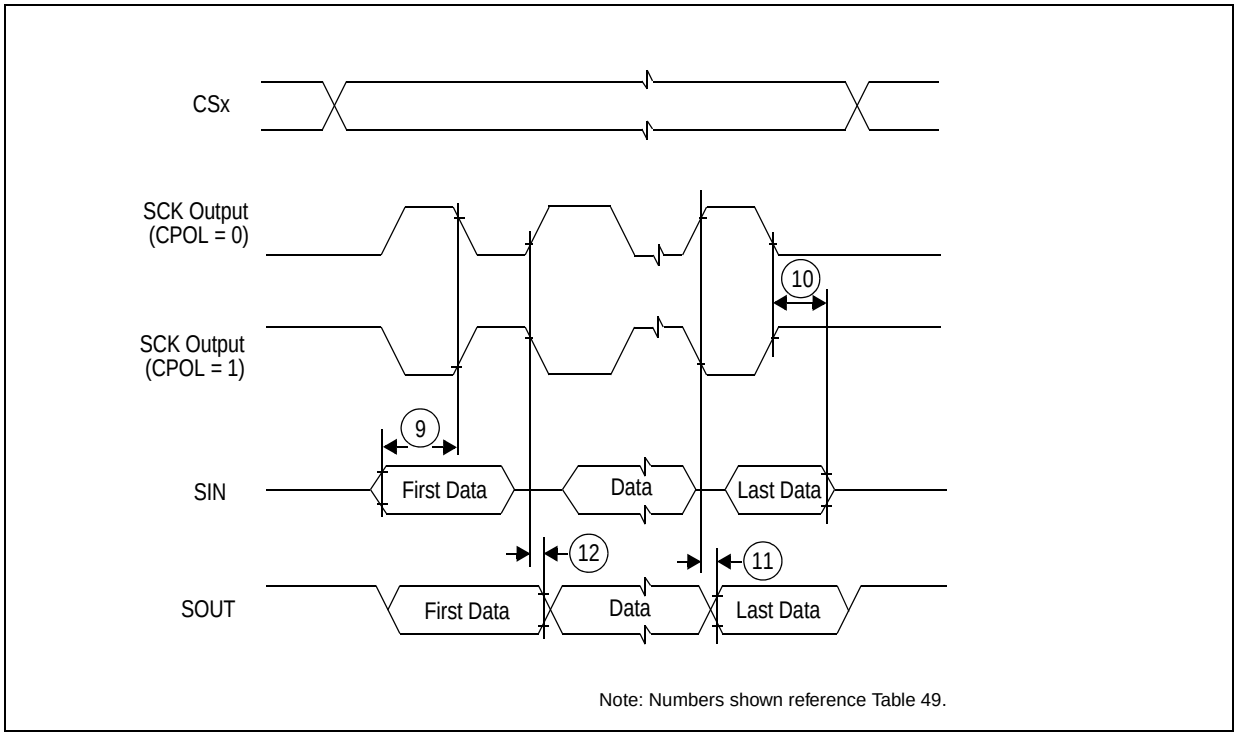


Figure 26. DSPI classic SPI timing–master, CPHA = 1

Table 51. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

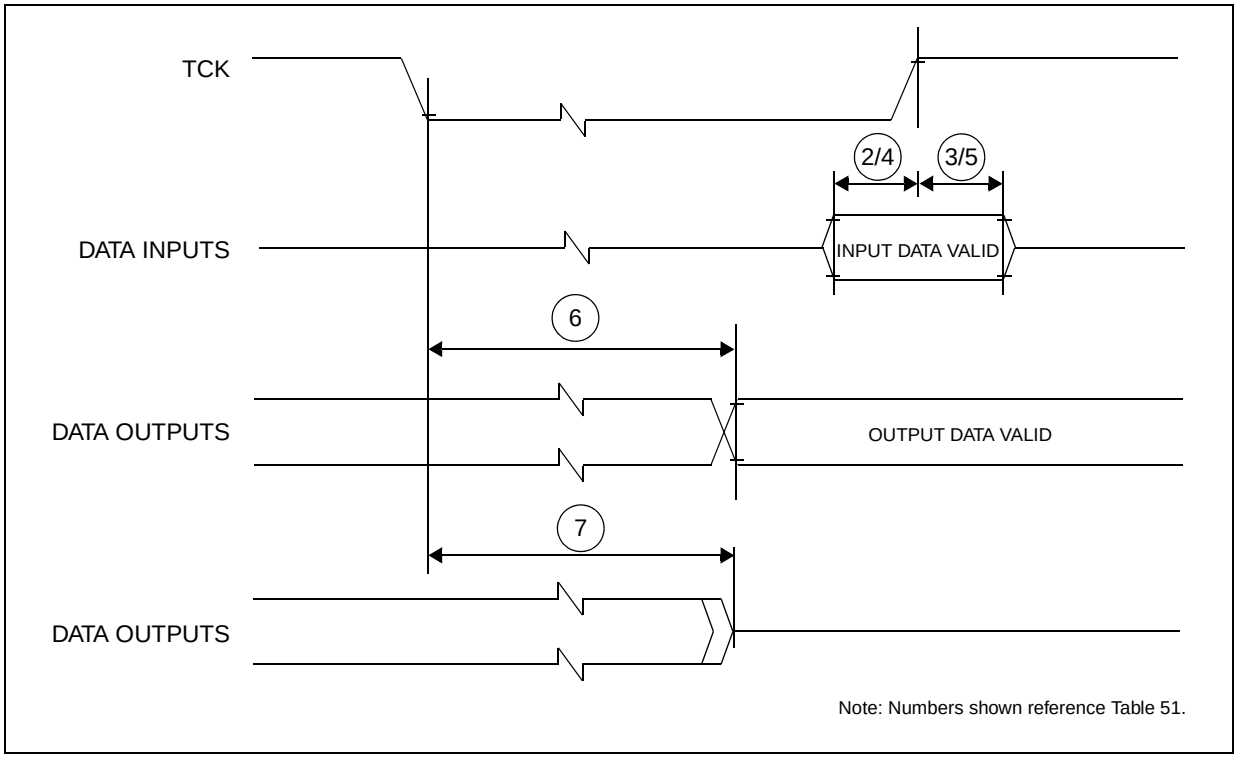


Figure 36. Timing diagram - JTAG boundary scan

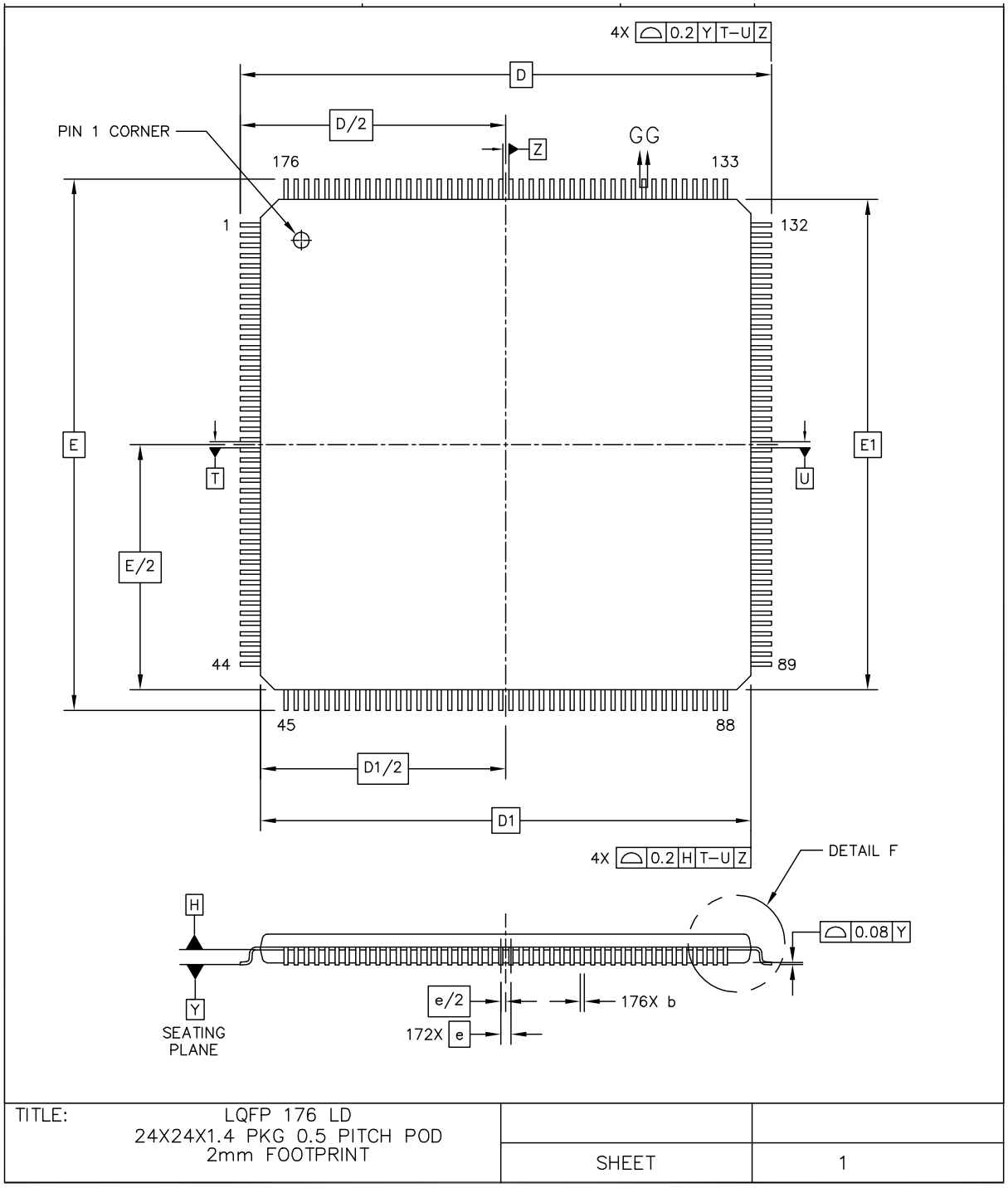


Figure 37. 176 LQFP mechanical drawing (Part 1 of 3)

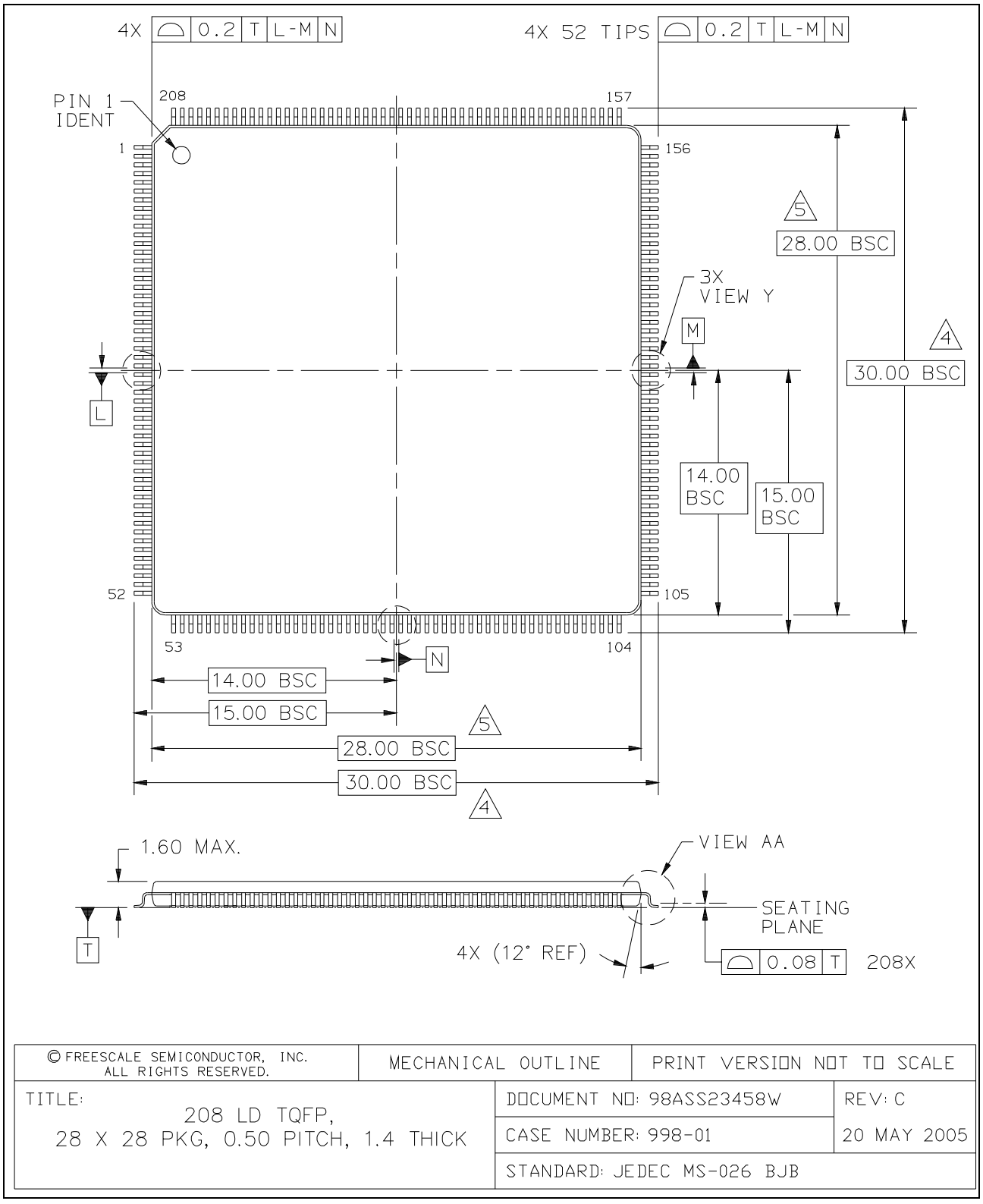


Figure 40. 208 LQFP mechanical drawing (Part 1 of 3)

Table 52. Revision history (continued)

Revision	Date	Changes
3	28 April 2011	• Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics • Updated Crystal oscillator and resonator connection scheme figure • Specified NPN transistor as the recommended BCP68 transistor throughout the document • Code and Data flash memory—Program and erase specifications tables: Renamed the parameter $t_{ESUS\ to}$ T_{eslat} • Revised the footnotes in the “Functional port pin descriptions” table. • In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. For ports PB[12–15], changed ANX to ADC0_X. • Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] • ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. • Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 µs and $T_{16Kpperase}$ to 500 µs. Corrected Teslat classification from “C” to “D”. • Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. • Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. • Functional port pin description: Added a footnote at the PB [9] port pin. • Absolute maximum ratings table: Added footnote 1. • Low voltage power domain electrical characteristics table: Updated IDDHALT, IDDSTOP, IDDSTBY3, IDDSTDBY2, IDDSTDBY1. • Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{mSXOSC}, V_{SXOSC}, $I_{SXOSCBIAS}$ and I_{SXOSC}. • FMPLL electrical characteristics table: Updated Δt_{LTJIT}. • Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. • MII serial management channel timing table: Updated M12 • JTAG characteristics table: Updated t_{TDOV}. • Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. • DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. • IO consumption table: Updated all parameter values. • DSPI electricals: Updated Δt_{CSC} max to 115 ns. • Low voltage power domain electrical characteristics table: Added footnote 9. • ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.