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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d, e200z0h
Core Size	32-Bit Dual-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5646cf0mlu1

Table of Contents

1 Introduction

1.1 Document Overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the MPC5646C device. To ensure a complete understanding of the device functionality, refer also to the MPC5646C Reference Manual.

1.2 Description

The MPC5646C is a new family of next generation microcontrollers built on the Power Architecture embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5646C family expands the range of the MPC560xB microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the MPC5646C automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UISA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5646C family comparison[1] (continued)

Feature	MPC5644B		MPC5644C			MPC5645B		MPC5645C			MPC5646B		MPC5646C		
Package	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA	176 LQFP	208 LQFP	176 LQFP	208 LQFP	256 BGA
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO[12]	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

NOTES:
1 Feature set dependent on selected peripheral multiplexing; table shows example.
2 Based on 125 °C ambient operating temperature and subject to full device characterisation.
3 The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4 DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5 Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6 There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7 16x precision channels (ANP) and 3x standard (ANS).
8 Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9 As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10 CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11 STCU controls MBIST activation and reporting.
12 Estimated I/O count for proposed packages based on multiplexing with peripherals.

F = Fast[1, 2]

I = Input only with analog feature[1]

A = Analog

3.2 System pins

The system pins are listed in Table 3.

Table 3. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					176 LQFP	208 LQFP	256 MAPBGA
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A[1]	—	58	74	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A[1]	—	56	72	T7

NOTES:
1 For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

3.3 Functional ports

The functional port pins are listed in Table 4.

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	108	130	J14
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	131	J15
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	134	J16
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	S	Tristate	111	135	H16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 CS0_2 — ADC0_S[20]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	112	136	G15
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 CS1_2 — ADC0_S[21]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	113	137	G14
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	S	Tristate	76	92	T12

Table 4. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								176 LQFP	208 LQFP	256 MAPBGA
PJ[7]	PCR[151]	AF0 AF1 AF2 AF3 —	GPIO[151] — — — ADC0_S[30]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	111	P16
PJ[8]	PCR[152]	AF0 AF1 AF2 AF3 —	GPIO[152] — — — ADC0_S[31]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	110	P15
PJ[9]	PCR[153]	AF0 AF1 AF2 AF3 —	GPIO[153] — — — ADC1_S[8]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	68	P5
PJ[10]	PCR[154]	AF0 AF1 AF2 AF3 —	GPIO[154] — — — ADC1_S[9]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	67	T5
PJ[11]	PCR[155]	AF0 AF1 AF2 AF3 —	GPIO[155] — — — ADC1_S[10]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	60	R3
PJ[12]	PCR[156]	AF0 AF1 AF2 AF3 —	GPIO[156] — — — ADC1_S[11]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	59	T1
PJ[13]	PCR[157]	AF0 AF1 AF2 AF3 — — — —	GPIO[157] — CS1_7 — CAN4RX ADC1_S[12] CAN1RX WKPU[31]	SIUL — DSPI_7 — FlexCAN_4 ADC_1 FlexCAN_1 WKPU	I/O — O — I I I I	S	Tristate	—	65	N5
PJ[14]	PCR[158]	AF0 AF1 AF2 AF3	GPIO[158] CAN1TX CAN4TX CS2_7	SIUL FlexCAN_1 FlexCAN_4 DSPI_7	I/O O O O	M/S	Tristate	—	64	T4

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD\_HV\_A/HV\_B}$ or $V_{IN} < V_{SS\_HV}$), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$[1]	SR	Voltage on $V_{DD\_HV\_A}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on $V_{DD\_HV\_B}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}[3]		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$[4]	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	3.0[5]	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$[7]	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_A}$[6]	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	

Table 20. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1,2]	Value[3]			Unit
					Min	Typ	Max	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65[4]	

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. All values need to be confirmed during device validation.
4. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

4.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

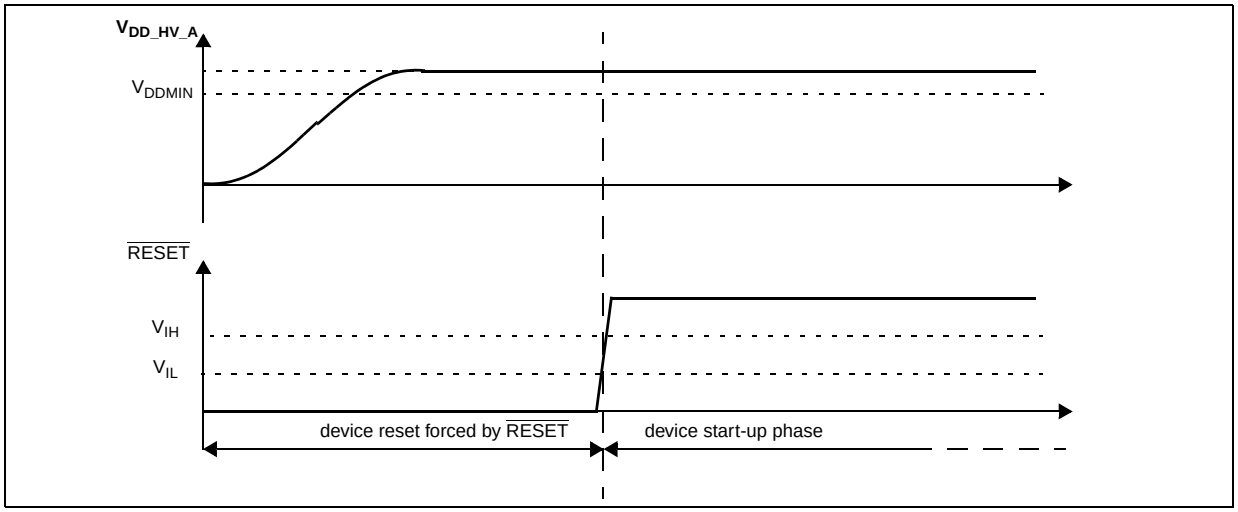


Figure 6. Start-up reset requirements

Table 22. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600[3]	mA

NOTES:
1. $V_{DD\_HV\_A}$ = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

4.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

NOTE

When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

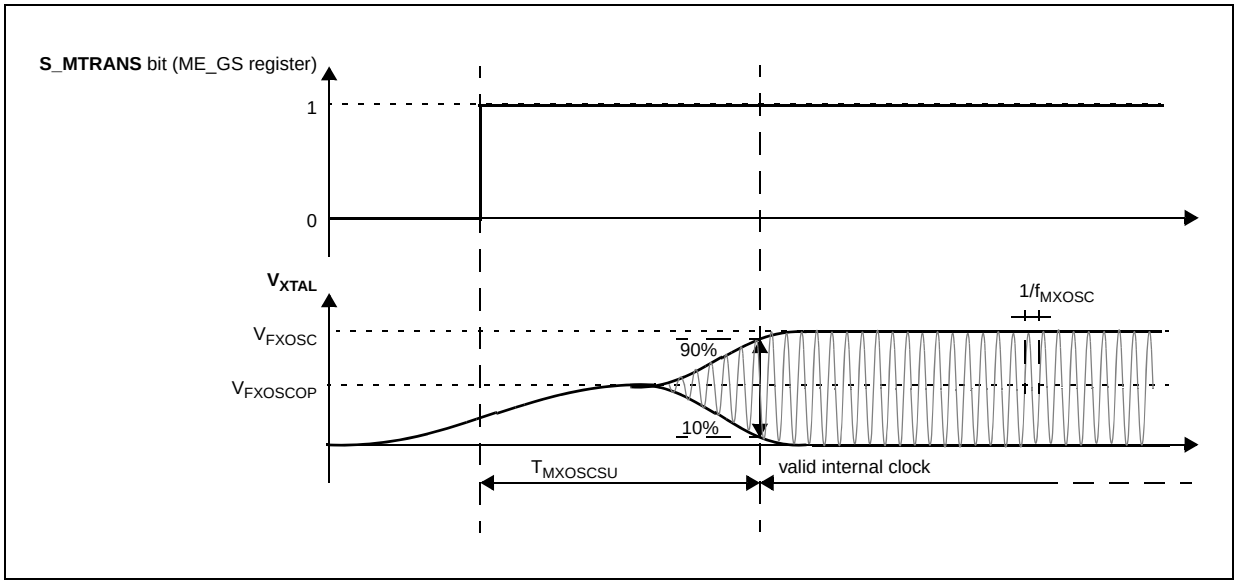


Figure 11. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Table 35. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	40.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%	4[3]	—	20[3]	mA/V
				V_{DD} = 5.0 V ± 10%	4[3]	—	20[3]	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	0.95	—	V
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	1.8		V
I_{FXOSC},[4]	CC	T	Fast external crystal oscillator consumption	V_{DD} = 3.3 V ± 10%, f_{OSC} = 40 MHz	—	2	2.2	mA
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 40 MHz	—	2.3	2.5	
				V_{DD} = 3.3 V ± 10%, f_{OSC} = 16 MHz	—	1.3	1.5	
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 16 MHz	—	1.6	1.8	
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	—	5	ms

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		untrimmed, across temperatures	84	—	205	
I_{SIRC}[3],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

NOTE

Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

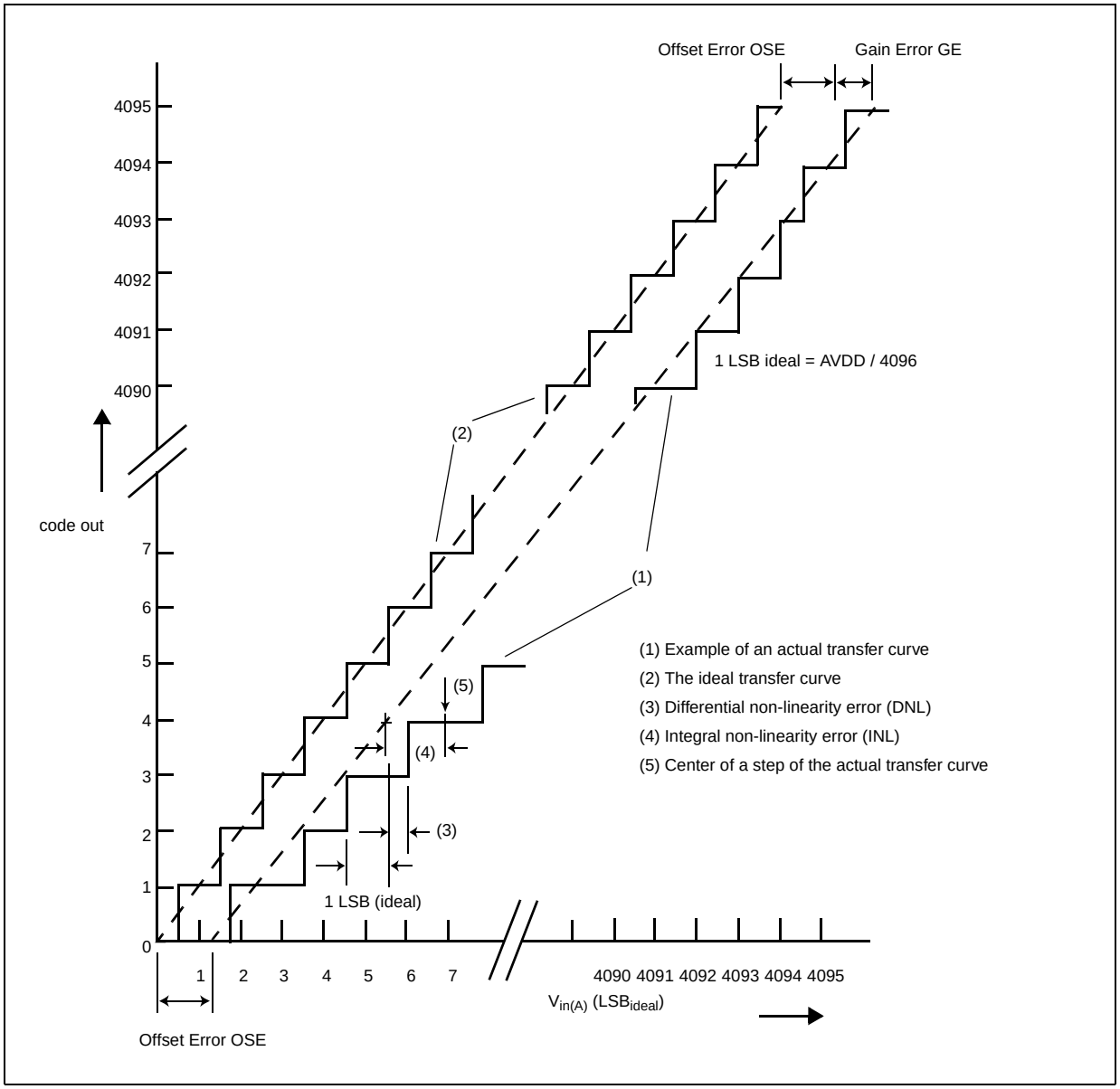


Figure 20. ADC_1 characteristic and error definitions

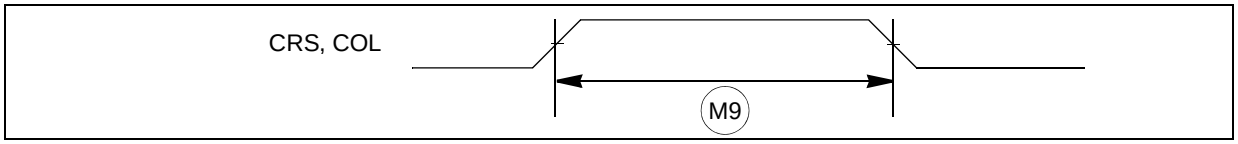


Figure 23. MII async inputs timing diagram

4.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 47. MII serial management channel timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

NOTES:
1 Output pads configured with SRE = 0b11.

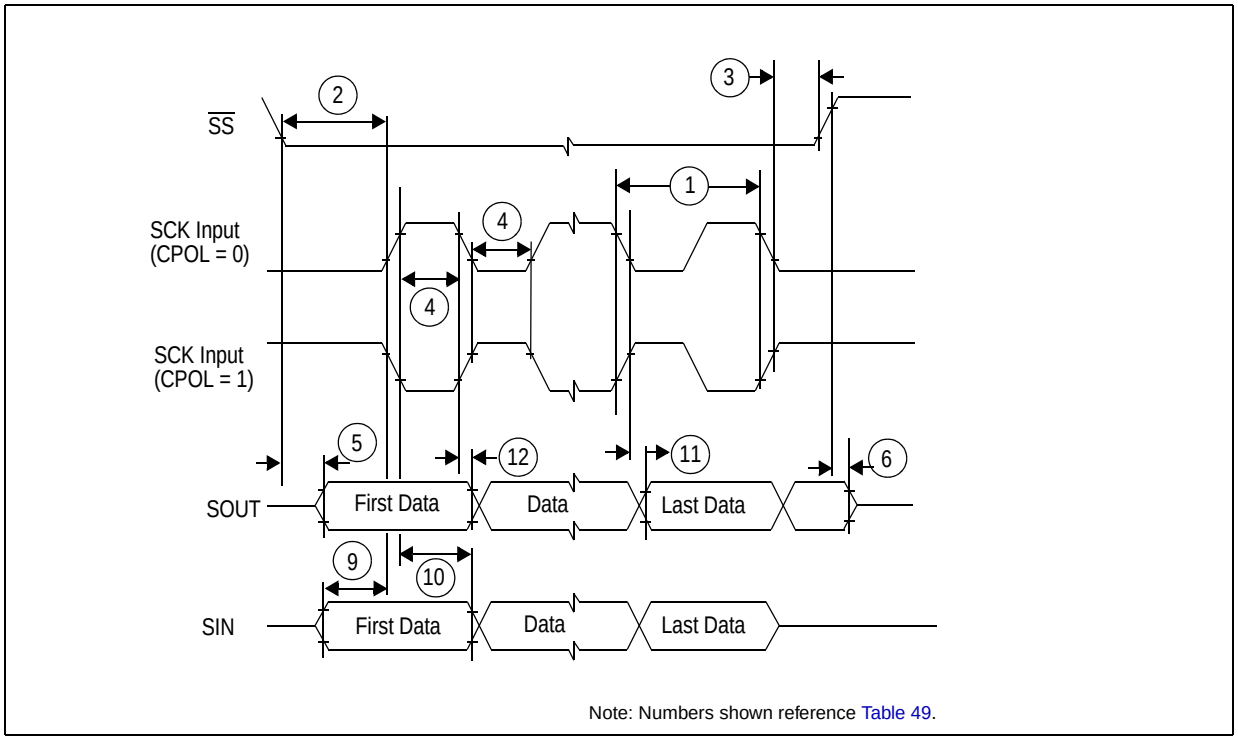


Figure 27. DSPI classic SPI timing–slave, CPHA = 0

5.1.3 256 MAPBGA package mechanical drawing

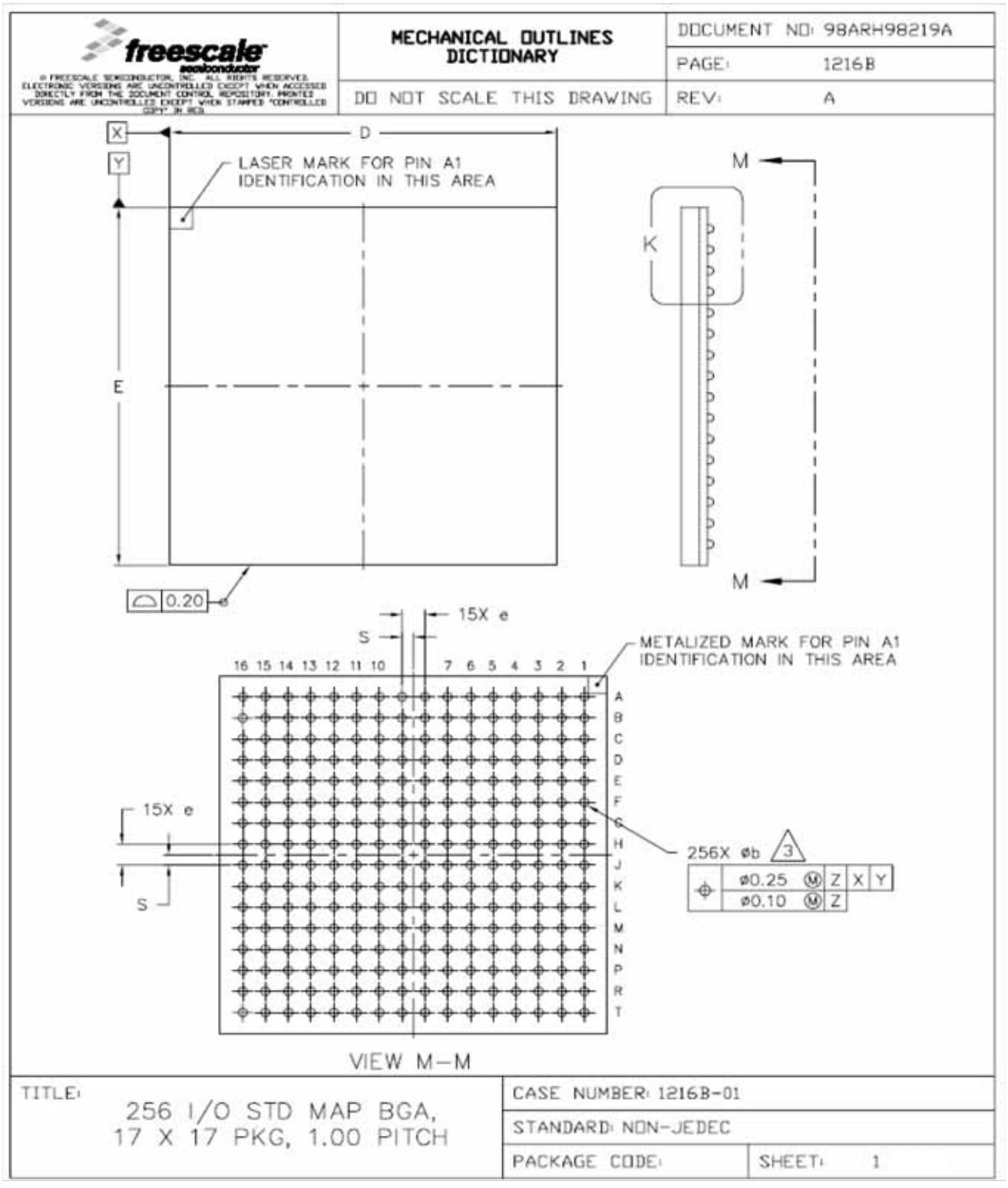
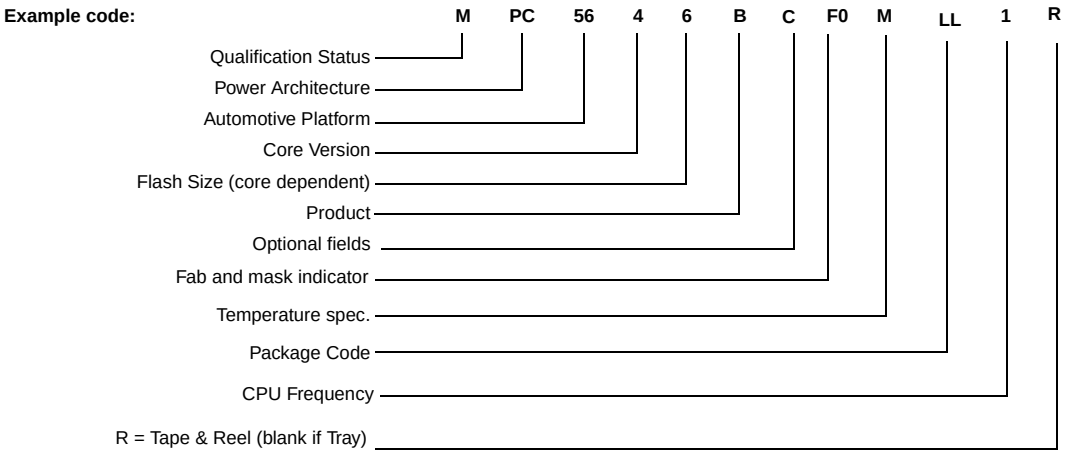


Figure 43. 256 MAPBGA mechanical drawing (Part 1 of 2)

6 Ordering information



Qualification Status
M = MC status
S = Auto qualified
P = PC status

PC = Power Architecture

Automotive Platform
56 = Power Architecture in 90 nm

Core Version
4 = e200z4d core version (highest core version in the case of multiple cores)

Flash Memory Size
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

Product Version
B = Body
C = Gateway

Optional fields
C = CSE module available
Blank = none of these options available

Fab and mask version indicator
F = ATMC
0 = First version of the mask

Temperature spec.
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C

Package Code
LU = 176 LQFP
LT = 208 LQFP
MJ = 256 MAPBGA

CPU Frequency
1 = e200z4d operates up to 120 MHz
8 = e200z4d operates up to 80 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Note: Not all options are available on all devices. Refer to Table 1, which shows the orderable part numbers for MPC564xx.

Figure 45. Orderable parts

7 Revision history

Table 52 summarizes revisions to this document.

Table 52. Revision history

Revision	Date	Changes
1	15 April 2010	Initial Release
2	17 August 2010	• Editing and formatting updates throughout the document. • Updated Voltage regulator capacitance connection figure. • Added a new sub-section "V_{DD_BV} Options" • Program and erase specifications: -Updated Tdwprogram TYP to 22 us -Updated T128Kpperase Max to 5000 ms -Added t_{ESUS} parameter • Added 208 MAPBGA thermal characteristics • Added recommendation in the Voltage regulator electrical characteristics section. • Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same. • Added new sections - Pad types, System pins and functional ports • Updated TYP numbers in the Flash program and erase specifications table • Added a new table: Program and erase specifications (Data Flash) • Flash read access timing table: Added Data flash memory numbers • Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter • Updated feature list. • MPC5646C 3M family comparison table: Updated ADC channels and added ADC footnotes. • MPC5646C 3M block diagram: Updated ADC channels and added legends. • MPC5646C 3M series block summary: Added new blocks. • Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins. • Electrical Characteristics: Replaced VSS with VSS_HV throughout the section. • Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0". • Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables. • LQFP thermal characteristics section: Updated numbers for LQFP packages. • Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments. • Code flash memory—Program and erase specifications: Updated tESRT to 20 ms. • ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document. • DSPI characteristics section: Replaced PCSx with CSx in all figures and tables.

Table 52. Revision history (continued)

Revision	Date	Changes
6	12 Feb 2014	• Removed occurrences of 208BGA from Table 3 System pin descriptions. • Added PM[3] and PM[4] in the figure note 1 of Figure 4, 256-pin BGA configuration. • Added a table note in Table 19 I/O supplies. • Updated Figure 8, Voltage regulator capacitance connection and added a note in this figure. • Removed max values of V_{LPREG} and V_{MREG}, changed min value of V_{LPREG} to 1.21 V, and updated V_{MREG} and V_{LPREG} after trimming values in Table 22 Voltage regulator electrical characteristics. • Updated 1st footnote and updated max values for I_{DDRUN}, I_{DDHALT}, I_{DDSTOP}, $I_{DDSTDBY3}$, $I_{DDSTDBY2}$, $I_{DDSTDBY1}$ and removed values at 85°C and 105°C in Table 24 Low voltage power domain electrical characteristics. • Added a footnote below Table 28 Flash memory read access timing. • Updated the formula in Eq. 11 in Section 4.17.1.1, "Input impedance and ADC accuracy. • Added Figure 17, Input equivalent circuit (extended channels). • Updated t_{ADC0_PU} value to 1.5 as max and added footnote for I_{INJ} in Table 42 ADC conversion characteristics (10-bit ADC_0). • Added Category column in Table 43 Conversion characteristics (12-bit ADC_1). • Added the IDD_HV_ADC0 values in Table 48 On-chip peripherals current consumption. • Added a note in Figure 45, Orderable parts.

NOTE

This revision history uses clickable cross-references for ease of navigation. The numbers and titles in each cross-reference are relative to the latest published release.

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