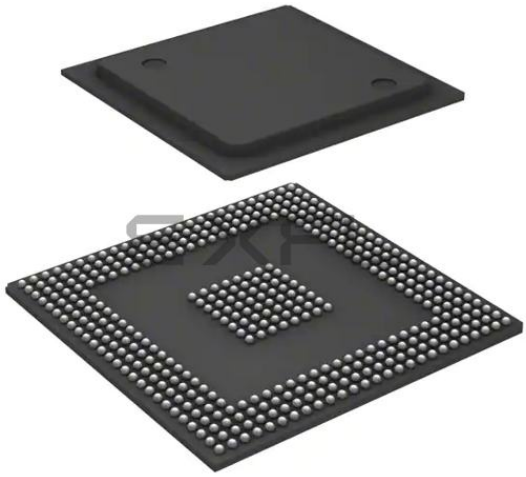

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777cak3mme3r

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability

1.2 Block diagram

The following figure shows a top-level block diagram of the MPC5777C. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch.

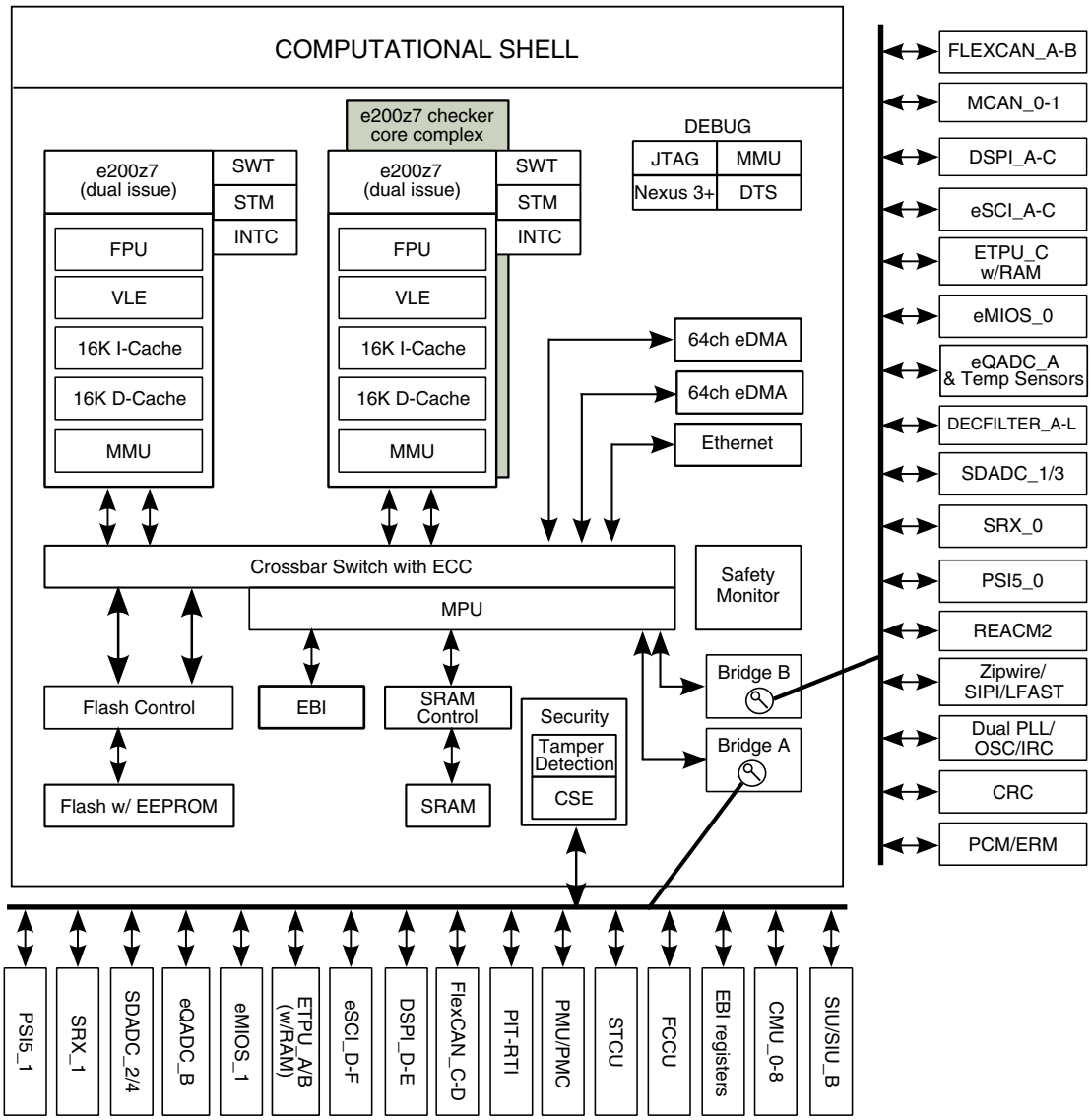
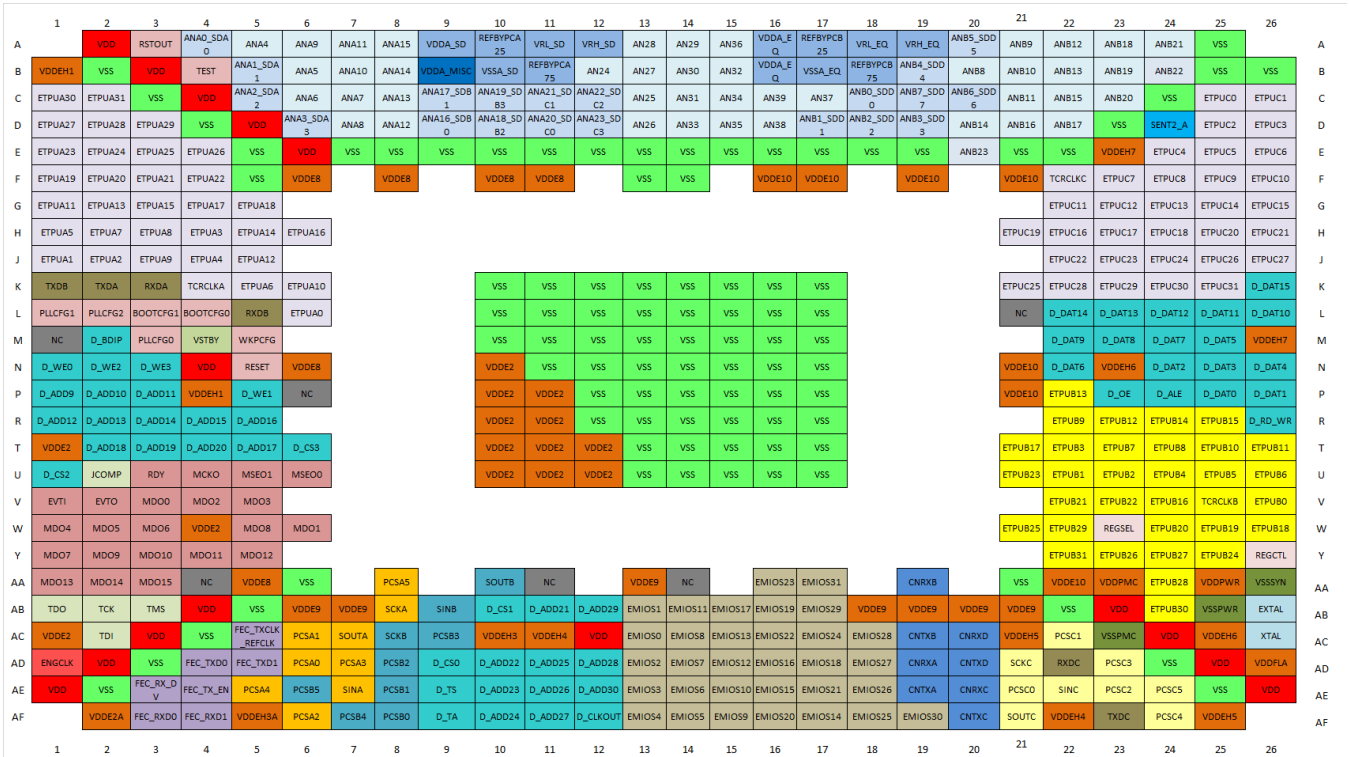


Figure 1. MPC5777C block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0_SDA0	ANA4	ANA9	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN29	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB5_SDD5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN30	AN32	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB4_SDD4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA7	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA22_SDC2	AN25	AN31	AN34	AN39	AN37	ANB0_SDD0	ANB7_SDD7	ANB6_SDD6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA8	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA23_SDC3	AN26	AN33	AN35	AN38	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB14	ANB16	ANB17	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				NC	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	NC	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	NC				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	NC	VDDE8	VSS		PCSA5		SOUTB	NC		VDDE9	NC		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDDPMC	ETPUB28	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5777C 516-ball MAPBGA (full diagram)

3 Electrical characteristics

The following information includes details about power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Absolute maximum ratings

Absolute maximum specifications are stress ratings only. Functional operation at these maxima is not guaranteed.

CAUTION

Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

See Operating conditions for functional operation specifications.

3.4 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted.

If the device operating conditions are exceeded, the functionality of the device is not guaranteed.

Table 3. Device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
f_{SYS}	Device operating frequency[1]	—	—	—	264[2]	MHz
f_{PLATF}	Platform operating frequency	—	—	—	132	MHz
f_{ETPU}	eTPU operating frequency	—	—	—	200	MHz
f_{EBI}	EBI operating frequency	—	—	—	66	MHz
f_{PER}	Peripheral block operating frequency	—	—	—	132	MHz
f_{FM_PER}	Frequency-modulated peripheral block operating frequency	—	—	—	132	MHz
t_{CYC}	Platform clock period	—	—	—	$1/f_{PLATF}$	ns
t_{CYC_ETPU}	eTPU clock period	—	—	—	$1/f_{ETPU}$	ns
t_{CYC_PER}	Peripheral clock period	—	—	—	$1/f_{PER}$	ns
Temperature						
T_J	Junction operating temperature range	Packaged devices	–40.0	—	150.0	°C
T_A (T_L to T_H)	Ambient operating temperature range	Packaged devices	–40.0	—	125.0[3]	°C
Voltage						
V_{DD}	External core supply voltage[4, 5]	LVD/HVD enabled	1.2	—	1.32	V
		LVD/HVD disabled[6, 7, 8, 9]	1.2	—	1.38	
V_{DDA_MISC}	TRNG and IRC supply voltage	—	3.5	—	5.5	V
V_{DDEx}	I/O supply voltage (fast I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEHx}[9]	I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEH1}	eTPU_A, eSCI_A, eSCI_B, and configuration I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
V_{DDPMC}[10]	Power Management Controller (PMC) supply voltage	Full functionality	3.15	—	5.5	V
V_{DDPWR}	SMPS driver supply voltage	Reference to V_{SSPWR}	3.0	—	5.5	V
V_{DDFLA}	Flash core voltage	—	3.15	—	3.6	V
V_{STBY}	RAM standby supply voltage	—	0.95[11]	—	5.5	V

Table continues on the next page...

Table 15. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
01110	14.9
01111	15.8

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the die and package capacitances given by C_{S_XTAL}/C_{S_EXTAL} in Table 14.

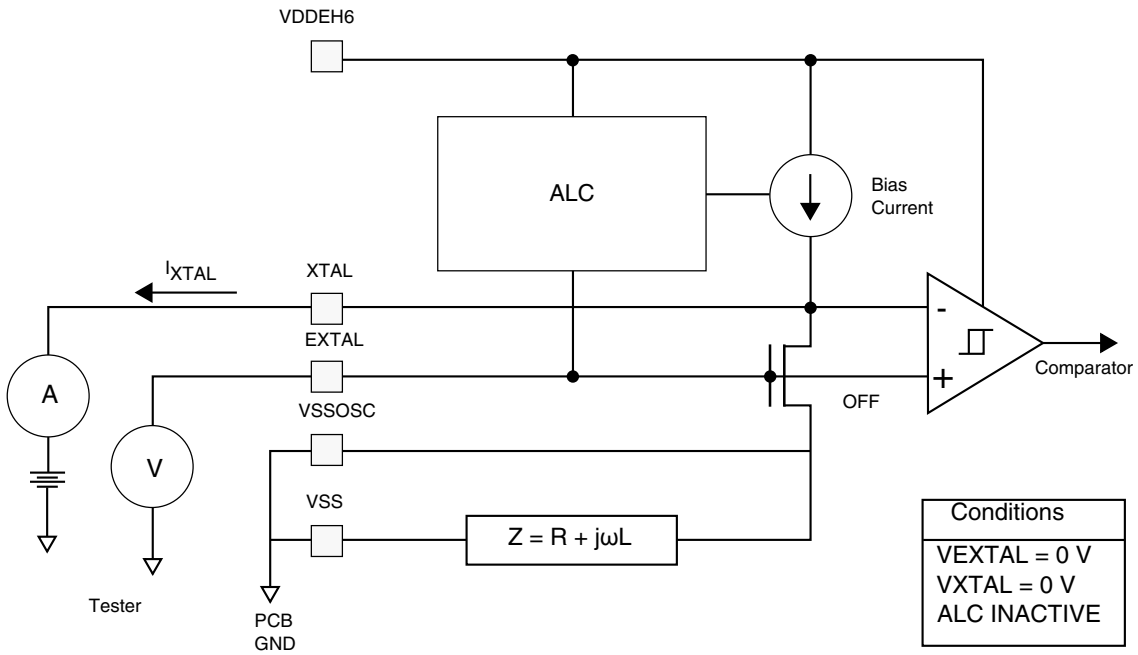


Figure 7. Test circuit

Table 16. Internal RC (IRC) oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRC target frequency	—	—	16	—	MHz
δf_{var_T}	IRC frequency variation	T < 150 °C	–8	—	8	%

3.8 Analog-to-Digital Converter (ADC) electrical specifications

5. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.
6. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
7. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.
8. Condition applies to two adjacent pins at injection limits.
9. Performance expected with production silicon.
10. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.
11. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
12. TUE does not apply to differential conversions.
13. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
14. Guaranteed 10-bit monotonicity.
15. At $V_{RH\_EQ} - V_{RL\_EQ} = 5.12$ V, one LSB = 1.25 mV.

3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

NOTE

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

Table 18. SDADC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	V_{DDA_SD}	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended $V_{INM} = V_{RL\_SD}$	V_{RH_SD}/GAIN			V
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 1	±0.5*V_{RH_SD}			
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 2,4,8,16	±V_{RH_SD}/GAIN			
		Differential $0 < V_{IN} < V_{DDEx}$	±V_{RH_SD}/GAIN			
f_{ADCD_M}	SD clock frequency[4]	—	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	—	—	—	333	Ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	SD register resolution[5]	2's complement notation	16			bit

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	72	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	69	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	66	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	62	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be “clipped.”
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5*V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range $3.6\ V < V_{DDA\_SD} < 4.0\ V$: SNR parameter degrades by 3 dB. SDADC is functional in the range $3.0\ V < V_{RH\_SD} < 4.0\ V$: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

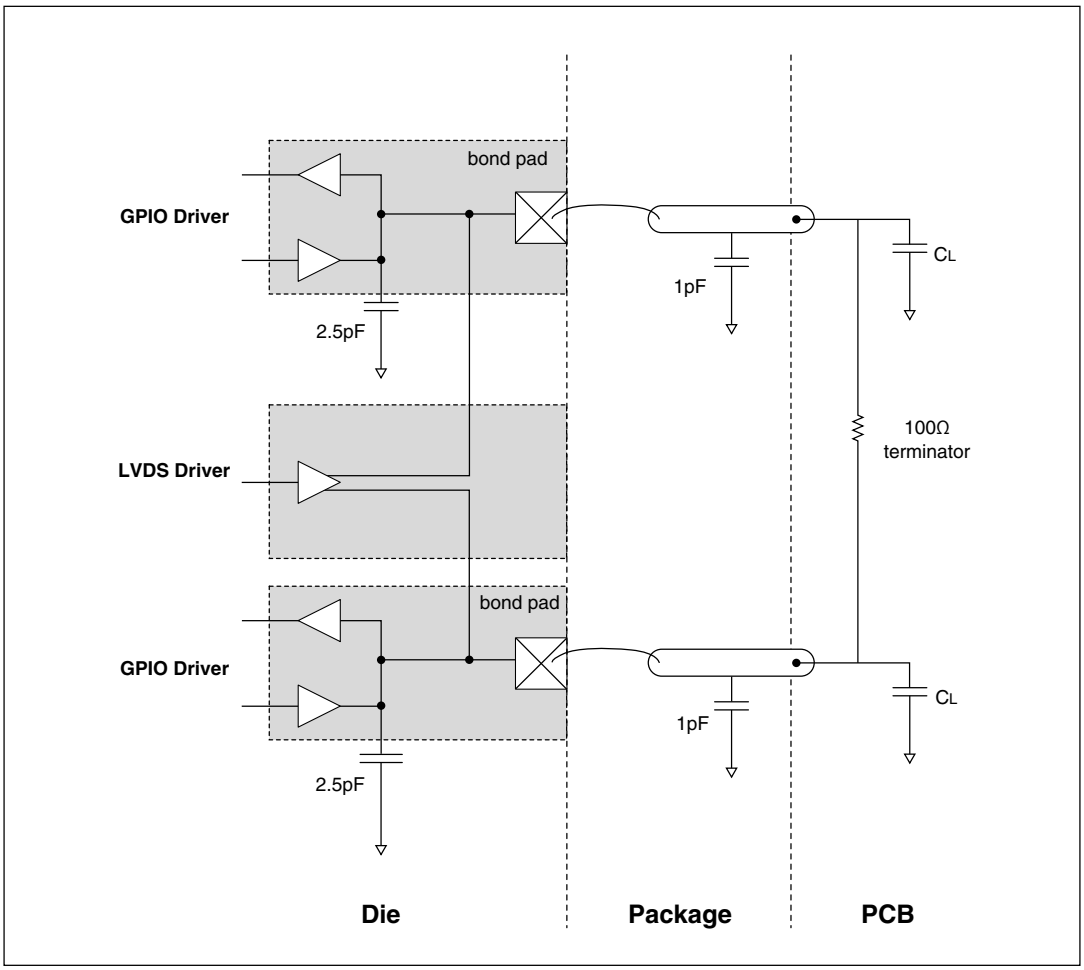


Figure 11. LVDS pad external load diagram

3.10.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 23. LFAST PLL electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
DC_{REF}	PLL reference clock duty cycle	—	45	—	55	%
PN	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
		f_{RF_REF} = 10 MHz	—	—	–64	
f_{VCO}	PLL VCO frequency	—	—	480[2]	—	MHz
t_{LOCK}	PLL phase lock[3]	—	—	—	40	µs

Table continues on the next page...

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

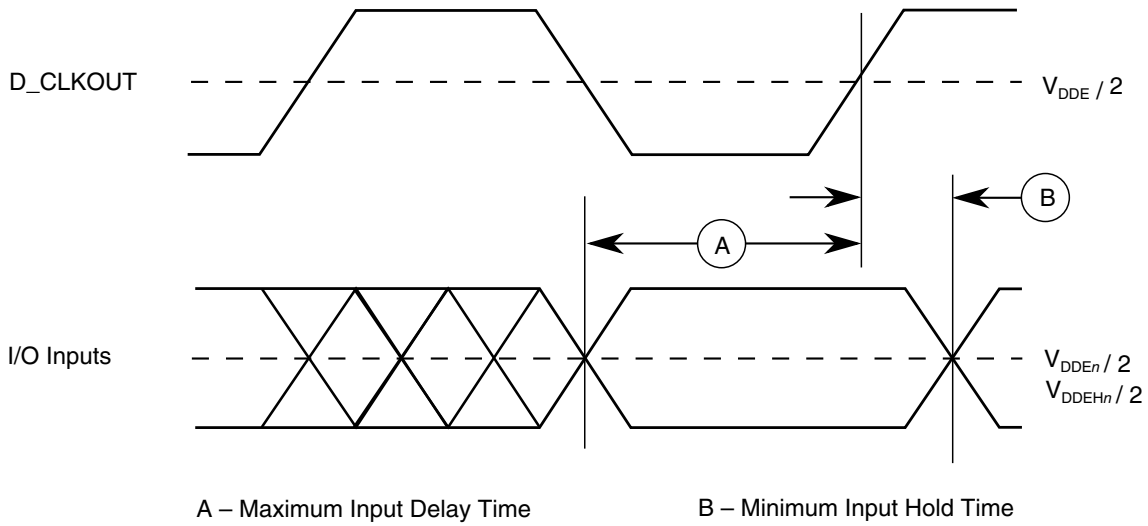


Figure 17. Generic input setup/hold timing

3.13.2 Reset and configuration pin timing

Table 35. Reset and configuration pin timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, TA = TL to TH.
2. For further information on t_{cyc}, see Table 3.

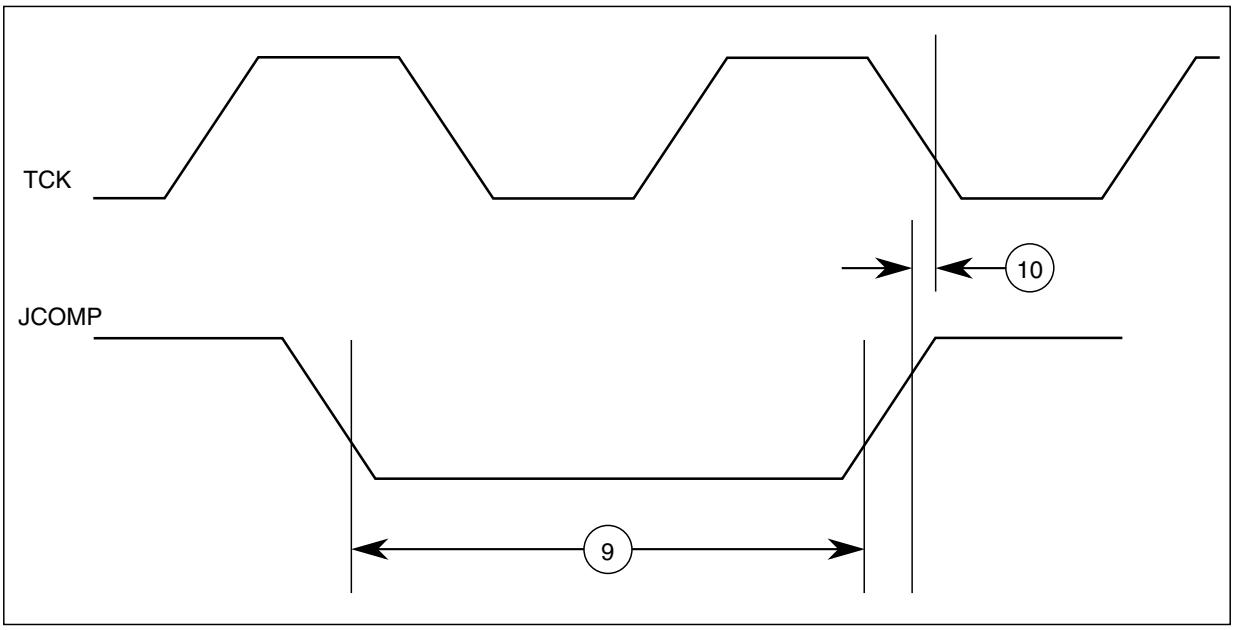


Figure 21. JTAG JCOMP timing

Table 38. Bus operation timing[1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3]	t_{COV}	—	8.5/9.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
	D_DAT[0:15]			11.5		—
	D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]			8.5/9.0		Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	t_{CIS}	7.5	—	ns	—
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	t_{CIH}	1.0	—	ns	—
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.

Table continues on the next page...

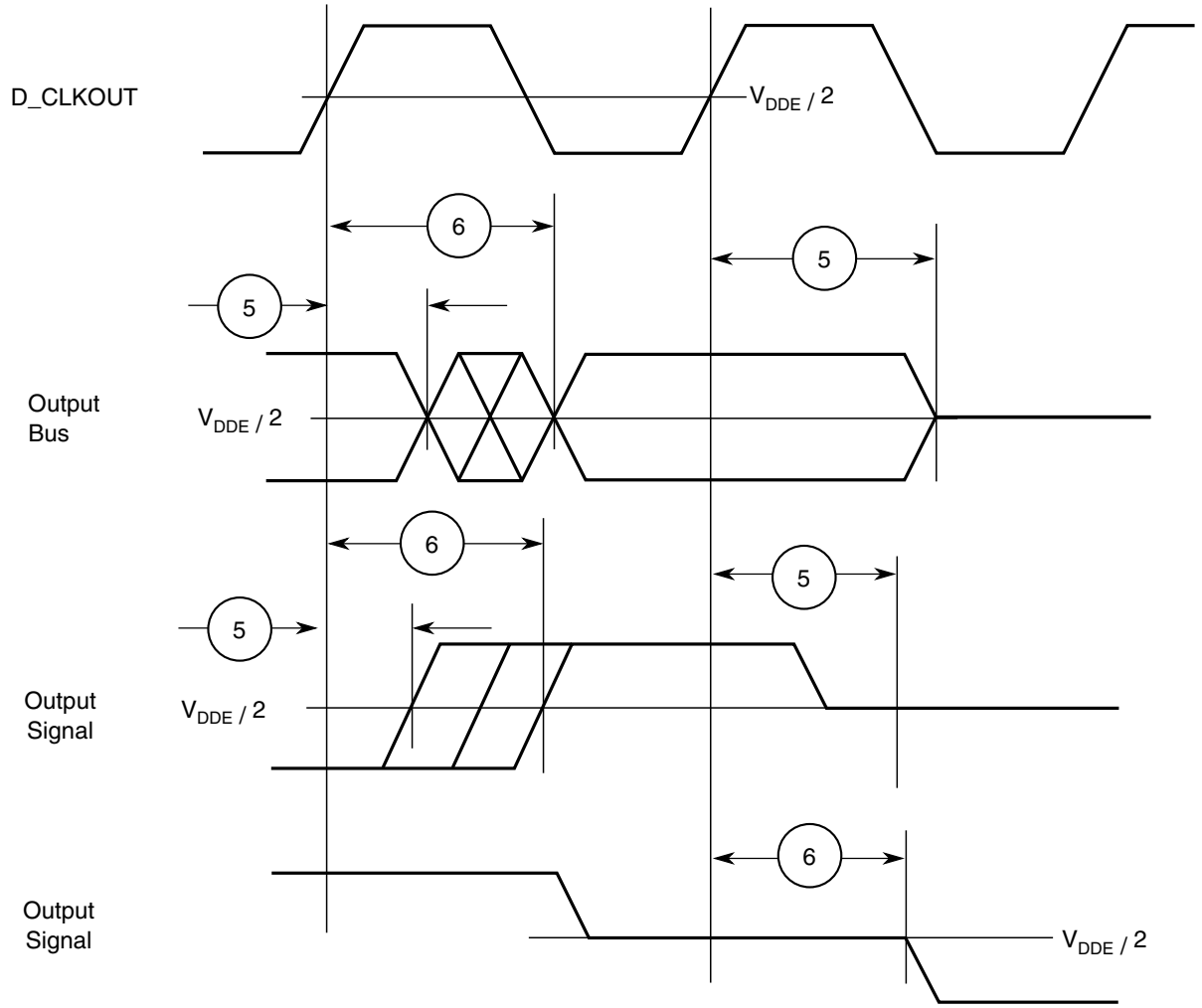


Figure 26. Synchronous output timing

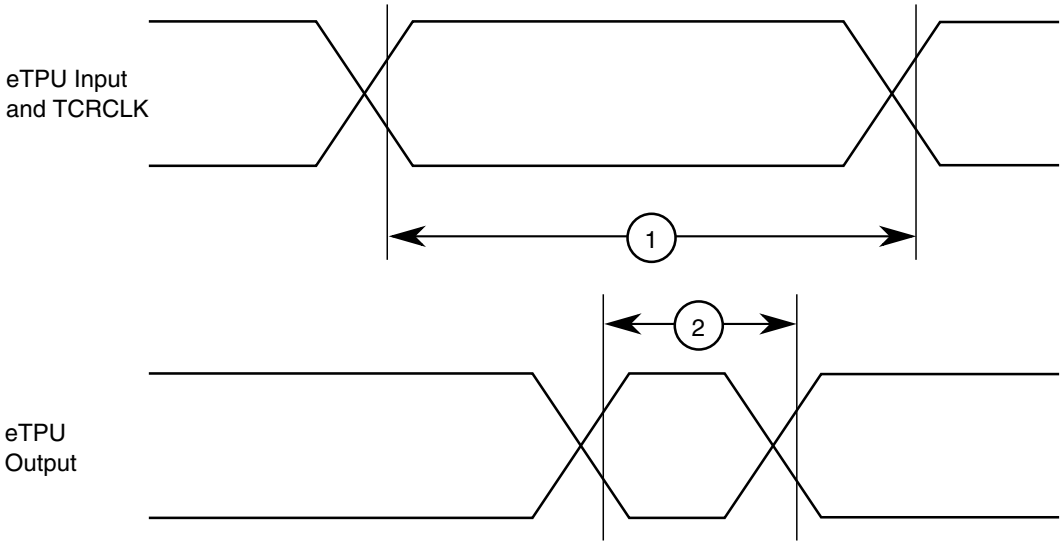


Figure 30. eTPU timing

3.13.8 eMIOS timing

Table 41. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

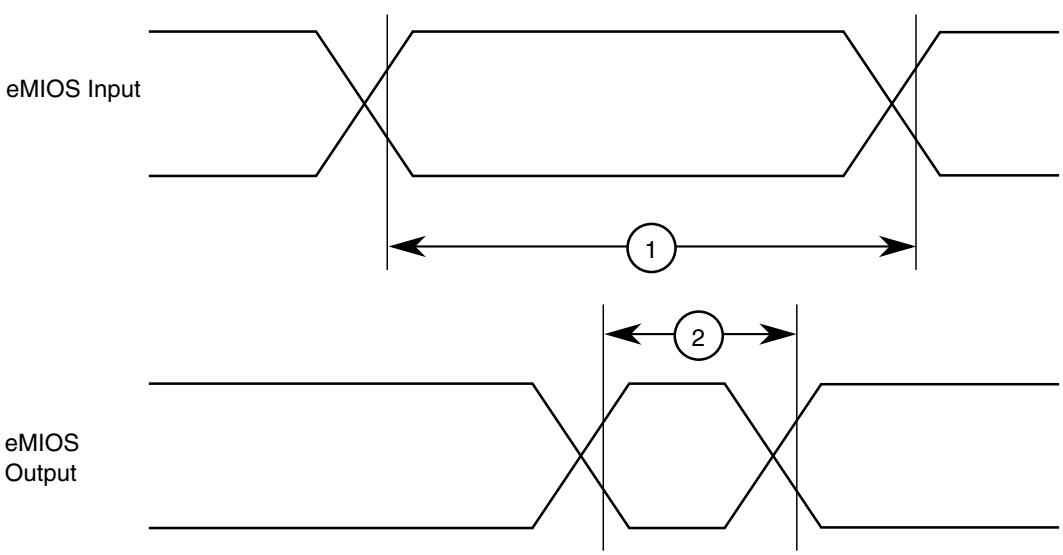


Figure 31. eMIOS timing

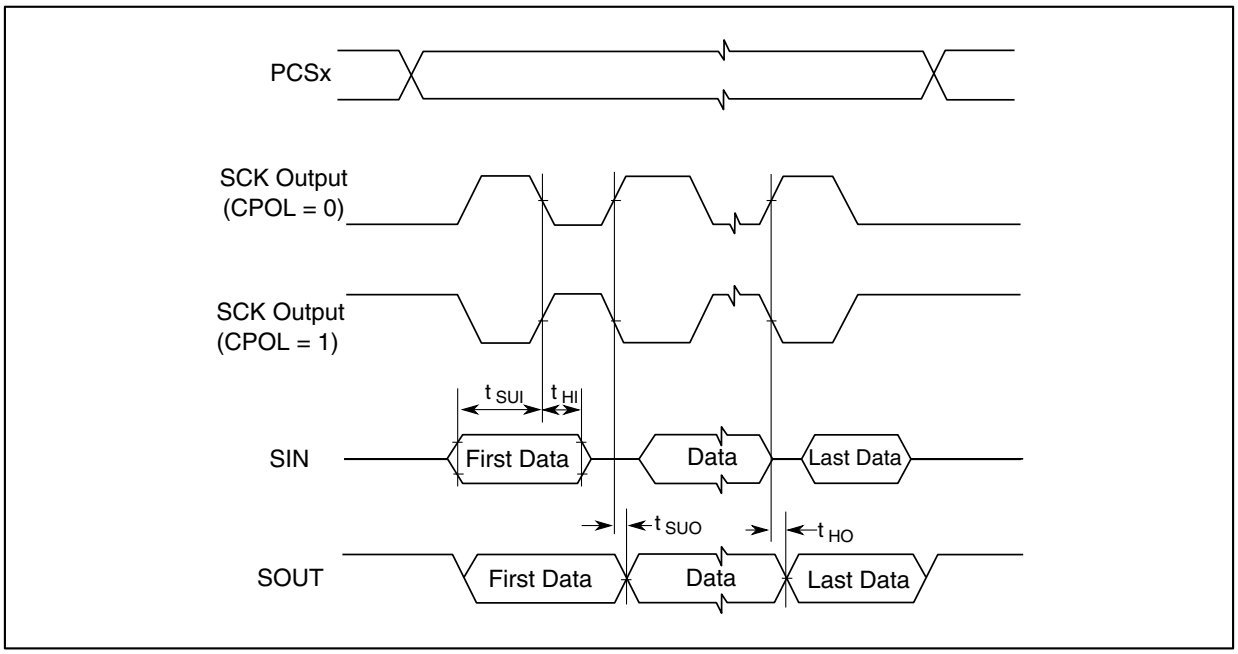


Figure 33. DSPI CMOS master mode – classic timing, CPHA = 1

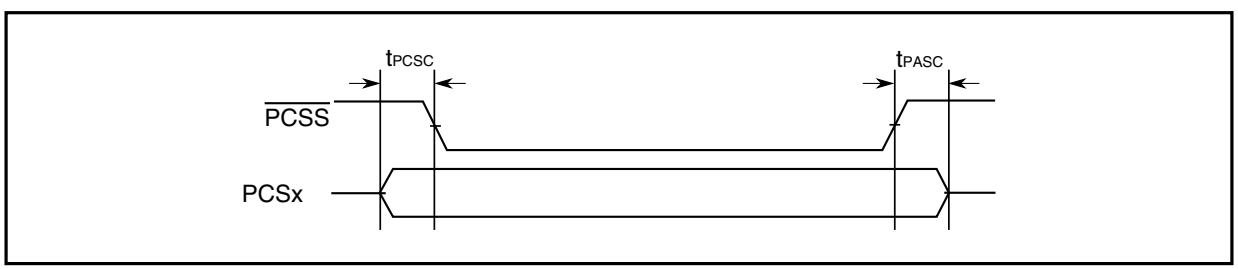


Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.2 DSPI CMOS Master Mode – Modified Timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK}$ – 5	$1/2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	50 pF	31 – ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	50 pF	62 – ($P^{11} \times t_{SYS}$, 6)	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							

Table continues on the next page...

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} – 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

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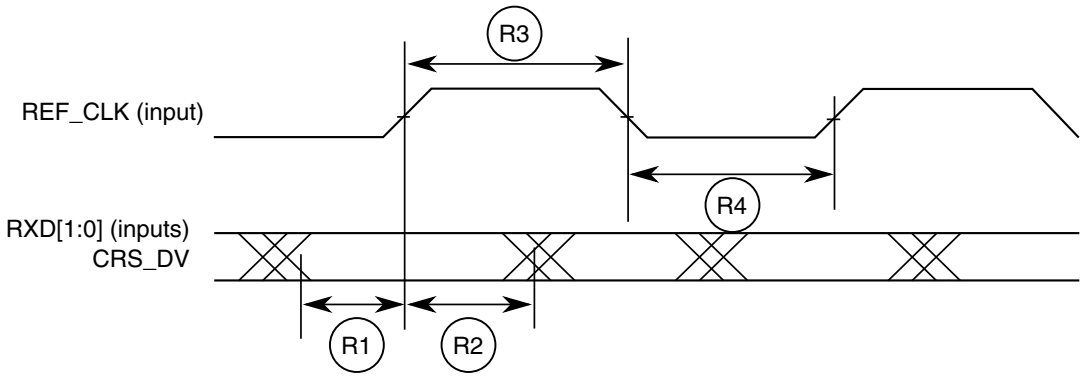

Figure 45. RMII receive signal timing diagram

3.13.10.6 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

Table 53. RMII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
R5	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately