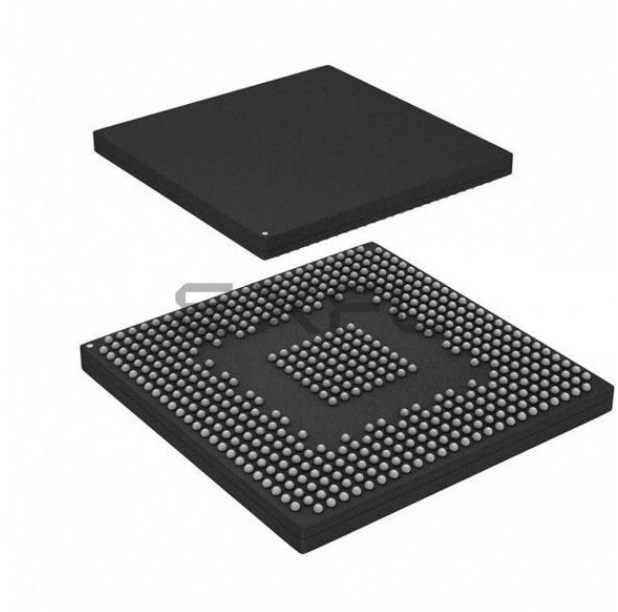

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777cck3mmo3r

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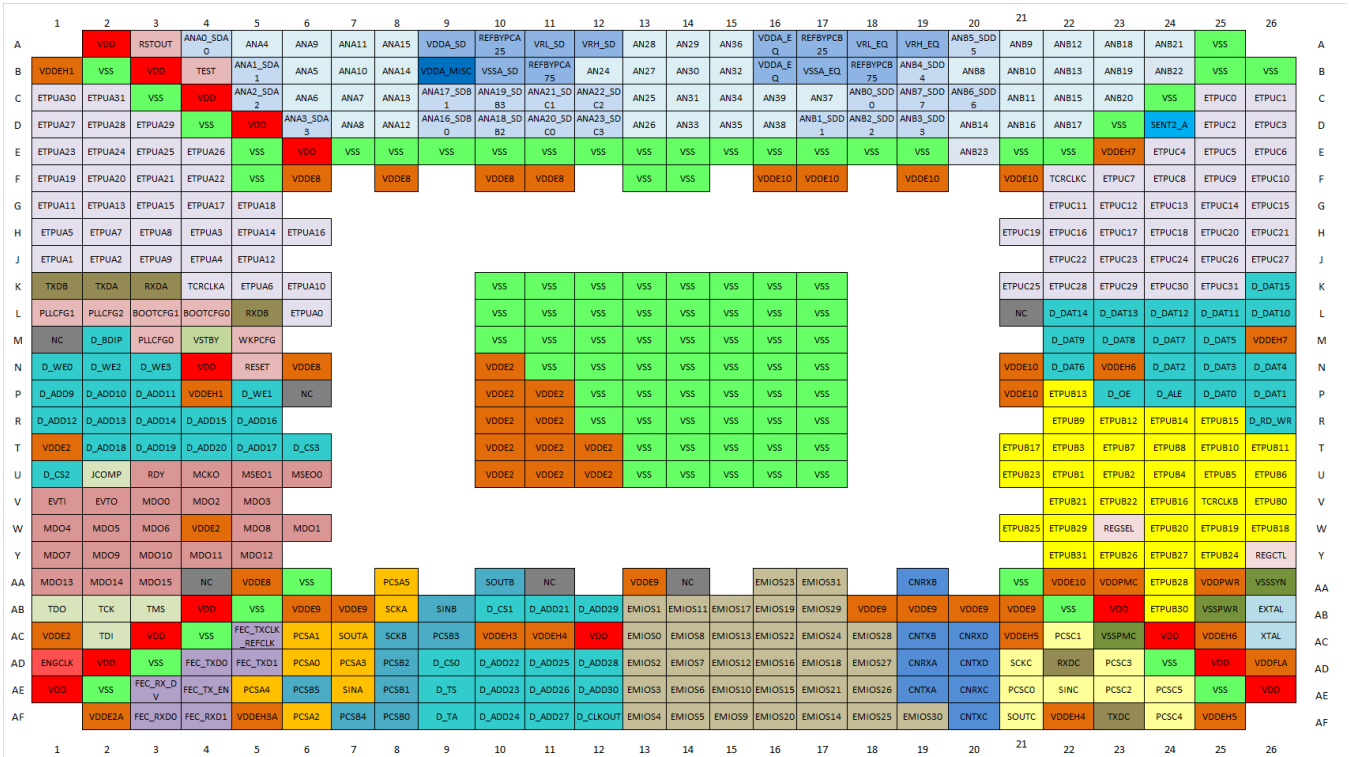

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0_SDA0	ANA4	ANA9	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN29	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB5_SDD5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN30	AN32	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB4_SDD4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA7	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA22_SDC2	AN25	AN31	AN34	AN39	AN37	ANB0_SDD0	ANB7_SDD7	ANB6_SDD6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA8	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA23_SDC3	AN26	AN33	AN35	AN38	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB14	ANB16	ANB17	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				NC	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	NC	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	NC				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	NC	VDDE8	VSS		PCSA5		SOUTB	NC		VDDE9	NC		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDDPMC	ETPUB28	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5777C 516-ball MAPBGA (full diagram)

3 Electrical characteristics

The following information includes details about power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Absolute maximum ratings

Absolute maximum specifications are stress ratings only. Functional operation at these maxima is not guaranteed.

CAUTION

Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

See Operating conditions for functional operation specifications.

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 5 shows output DC electrical characteristics.

2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

The following table shows the EBI CLKOUT, address, and control signal pad electrical characteristics. These pads can also be used for GPIO.

Table 10. GPIO and EBI CLKOUT, address, and control signal pad output buffer electrical characteristics (FC pads)

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications: valid for 3.0 V < V_{DDEx} < 3.6 V							
C_{DRV}	External bus load capacitance	PCR[DSC] = 01b		—	—	10	pF
		PCR[DSC] = 10b		—	—	20	
		PCR[DSC] = 11b		—	—	30	
f_{MAX_EBI}	External bus maximum operating frequency	C_{DRV} = 10/20/30 pF		—	—	66	MHz
GPIO and EBI Mode Output Specifications							
I_{OH_EBI}	GPIO and external bus pad output high current	V_{OH} = 0.8 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	30	—	—	mA
			PCR[DSC] = 10b	22	—	—	
			PCR[DSC] = 01b	13	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OH} = 0.8 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	16	—	—	
			PCR[DSC] = 10b	12	—	—	
			PCR[DSC] = 01b	7	—	—	
			PCR[DSC] = 00b	1	—	—	
I_{OL_EBI}	GPIO and external bus pad output low current	V_{OL} = 0.2 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	54	—	—	mA
			PCR[DSC] = 10b	25	—	—	
			PCR[DSC] = 01b	16	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OL} = 0.2 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	17	—	—	
			PCR[DSC] = 10b	14	—	—	
			PCR[DSC] = 01b	8	—	—	
			PCR[DSC] = 00b	1	—	—	
$t_{R\_F\_EBI}$	GPIO and external bus pad output transition time (rise/fall)	PCR[DSC] = 11b	C_L = 30 pF	—	—	1.5	ns
			C_L = 50 pF	—	—	2.4	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	1.5	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	1.85	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	45	
t_{PD_EBI}	GPIO and external bus pad output propagation delay time	PCR[DSC] = 11b	C_L = 30 pF	—	—	4.2	ns
			C_L = 50 pF	—	—	5.5	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	4.2	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	4.4	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	59	

Table 13. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL1PHISPJ}\rvert$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[2]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 14 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 14. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	—	V_{REF} – 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.1	2.8	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.2	2.9	
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	80	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	77	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	74	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	71	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	71	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	70	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	68	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	65	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	62	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be “clipped.”
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5*V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range $3.6\ V < V_{DDA\_SD} < 4.0\ V$: SNR parameter degrades by 3 dB. SDADC is functional in the range $3.0\ V < V_{RH\_SD} < 4.0\ V$: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the SDADC module.

16. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.9 Temperature Sensor

The following table describes the Temperature Sensor electrical characteristics.

Table 19. Temperature Sensor electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy	–40°C < T_J < 150°C	–5	—	5	°C
I_{TEMP_SENS}	V_{DDA_EQA} power supply current, per Temp Sensor	—	—	—	700	µA

3.10 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to the SIPI interface on the chip. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.10.1 LFAST interface timing diagrams

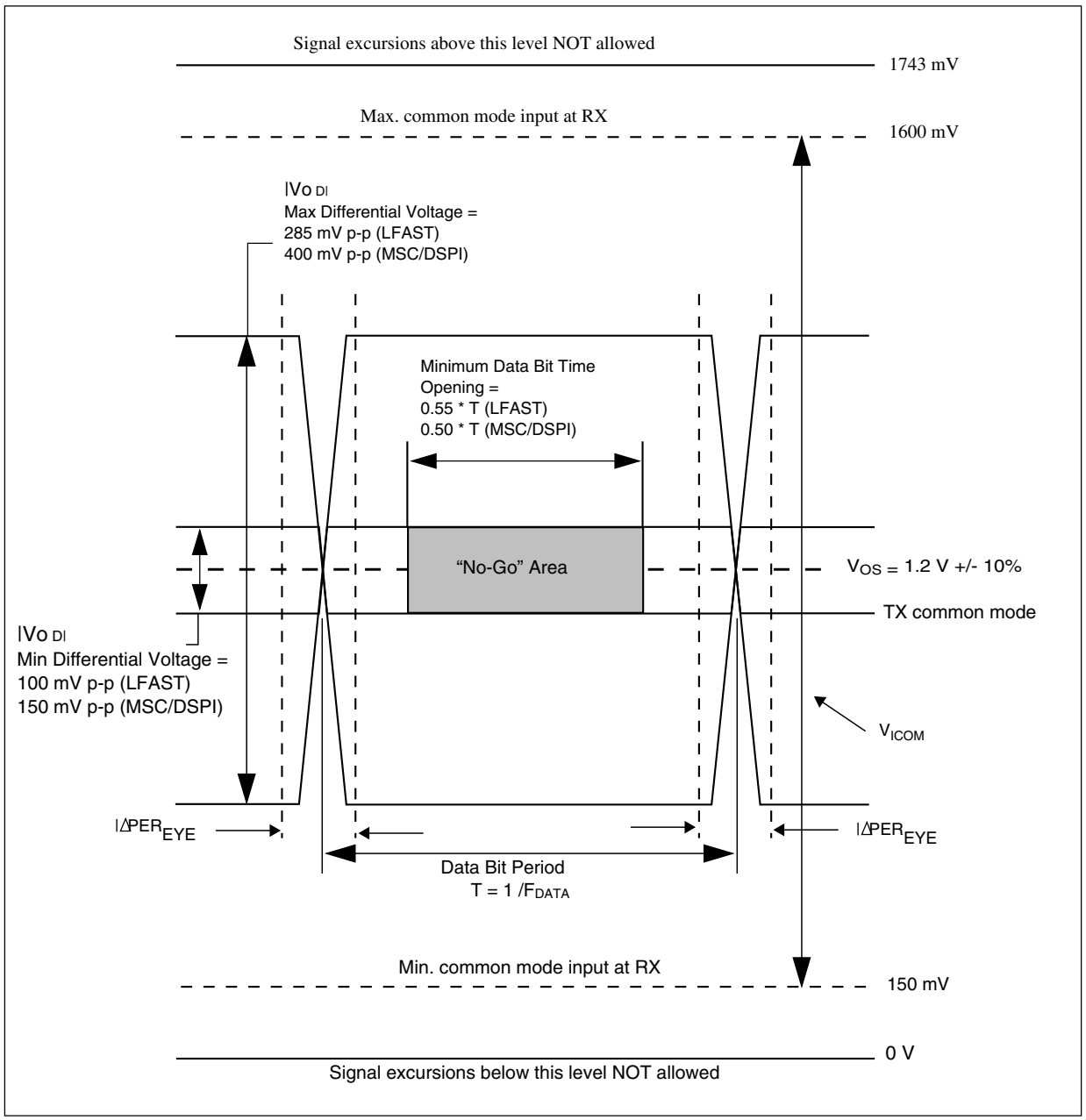

Figure 8. LFAST and MSC/DSPI LVDS timing definition

Table 26. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	p-MOS	3 A - 20 V	SQ2301ES / FDC642P or equivalent: low threshold p-MOS, Vth < 2.0 V, Rdson @ 4.5 V < 100 mΩ, Cg < 5 nF
D1	Schottky	2 A - 20 V	SS8P3L or equivalent: Vishay™ low Vf Schottky diode
L	Inductor	3−4 µH - 1.5 A	Buck shielded coil low ESR
CI	Capacitor	22 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.1 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF capacitor in parallel)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to the p-MOS source)
R	Resistor	2.0-4.7 kΩ	Pullup for power p-MOS gate
CB	Capacitor	22 µF - 20 V	Ceramic, connect 100 nF capacitor in parallel (as close as possible to package to reduce current loop from V_{DDPWR} to V_{SSPWR})

The following diagram shows the SMPS configuration connection.

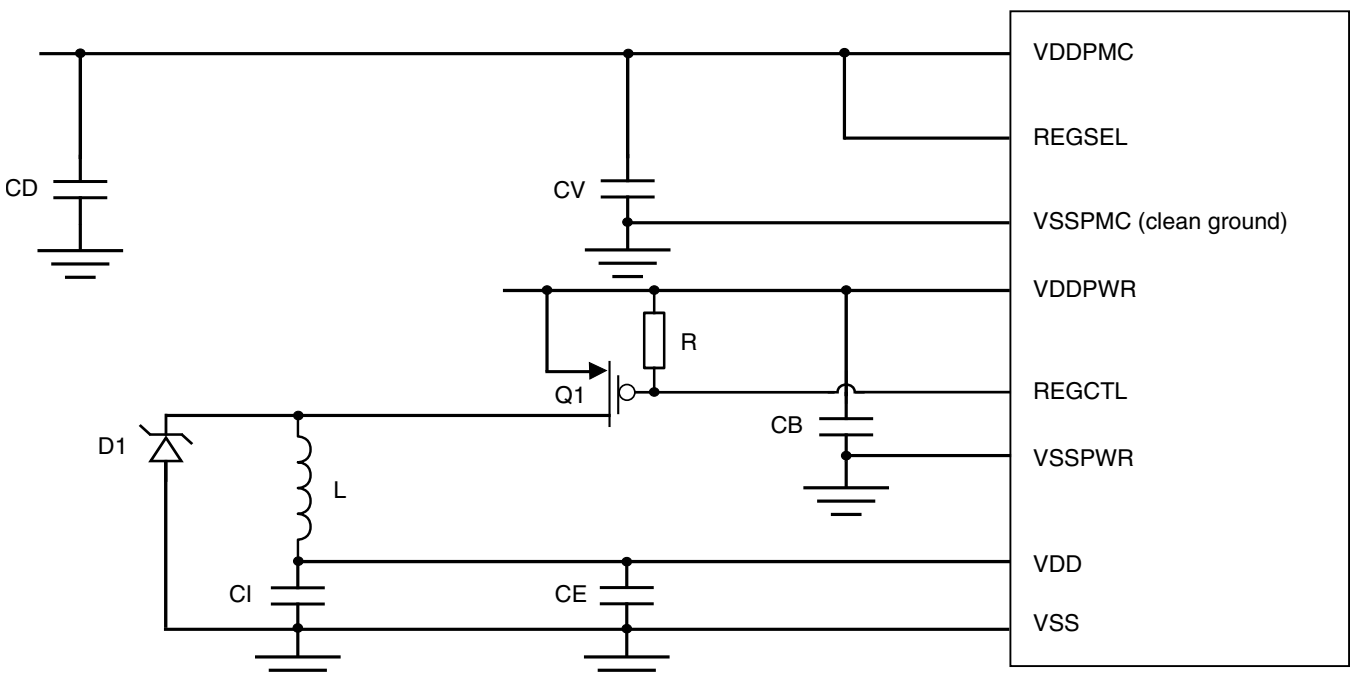

Figure 13. SMPS configuration

NOTE

The REGSEL pin is tied to V_{DDPMC} to select SMPS. If REGSEL is 0, the chip boots with the linear regulator.

See Power sequencing requirements for details about V_{DDPMC} and V_{DDPWR}.

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
   - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

   During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

   During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

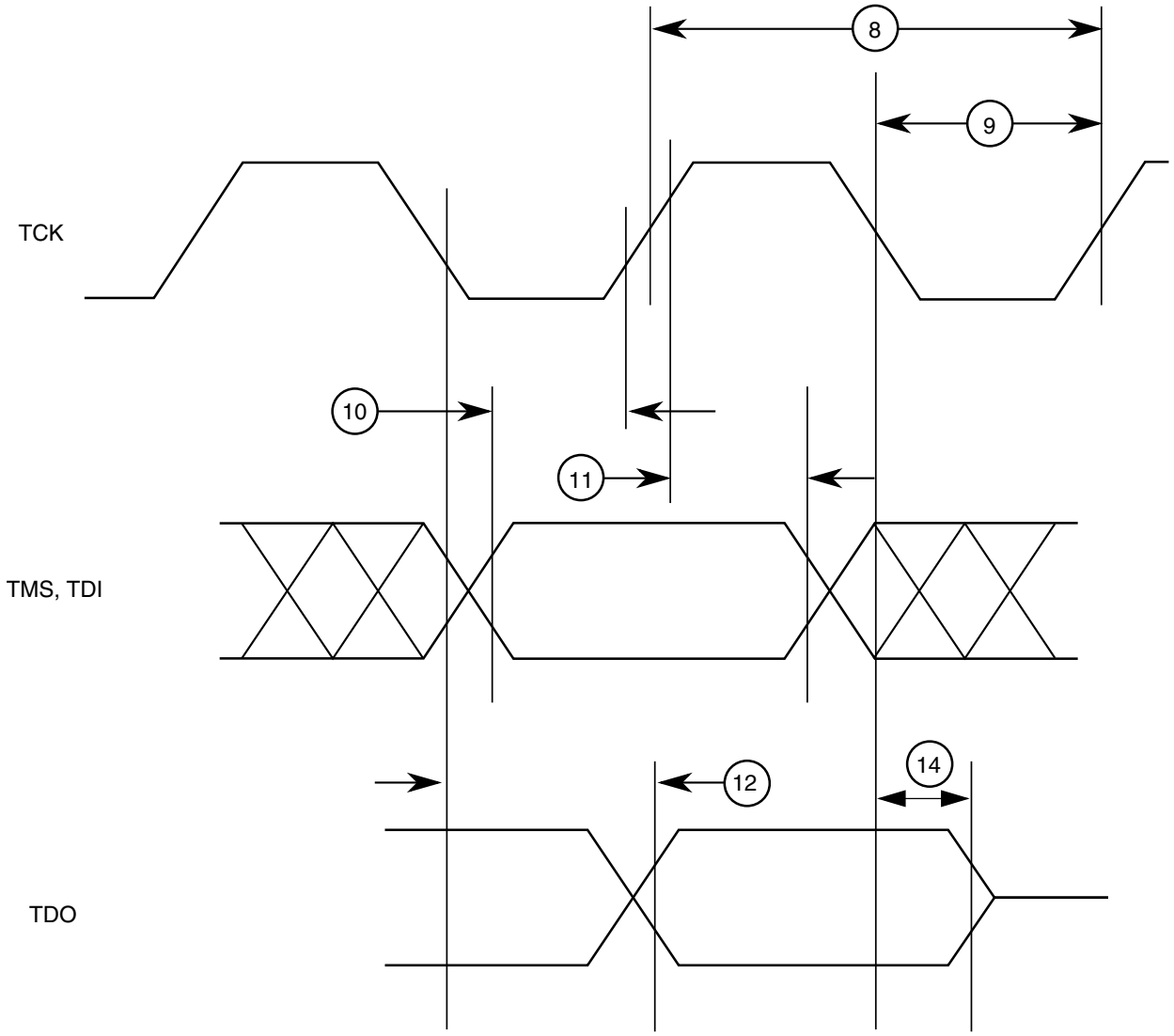

Figure 24. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External Bus Interface (EBI) timing

Table 38. Bus operation timing[1]

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	—
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	—
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	—

Table continues on the next page...

3.13.9 DSPI timing with CMOS and LVDS pads

NOTE

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 42. Timing specifications are shown in Table 43, Table 44, Table 45, Table 46, and Table 47.

Table 42. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1, 2]
CMOS (Master mode)	Full duplex – Classic timing (Table 43)	17
	Full duplex – Modified timing (Table 44)	30
	Output only mode (SCK/SOUT/PCS) (Table 43 and Table 44)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 47)	30
LVDS (Master mode)	Full duplex – Modified timing (Table 45)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 46)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.13.9.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.13.9.1.1 DSPI CMOS Master Mode — Classic Timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

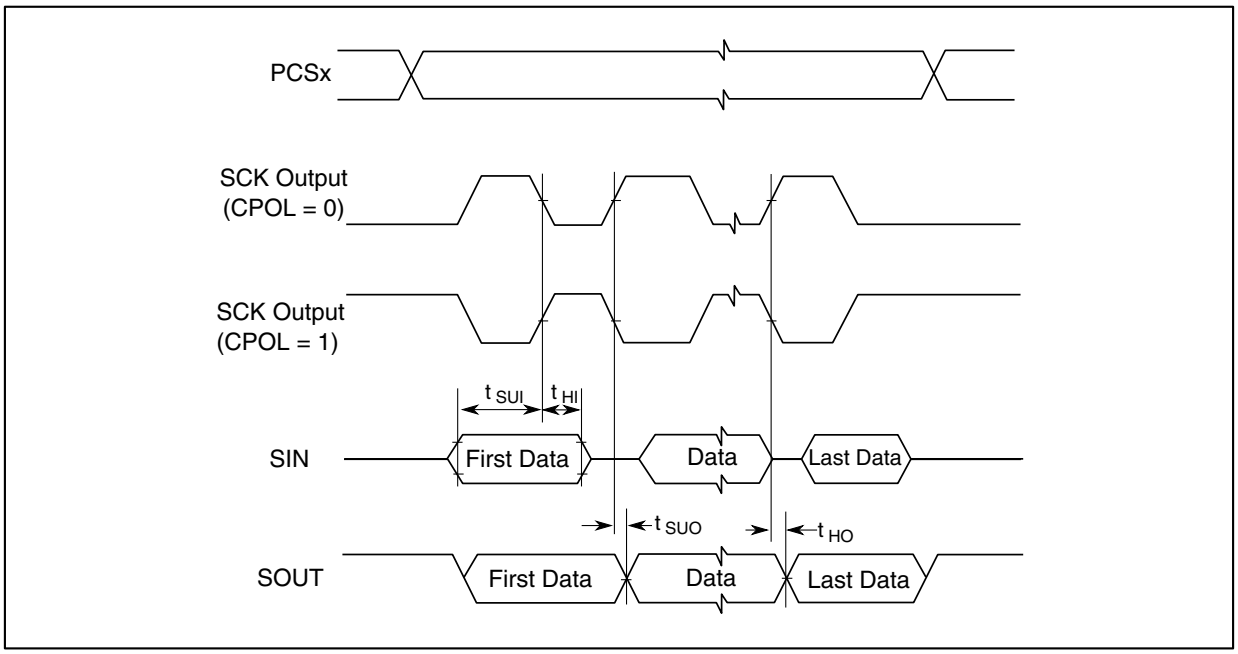

Figure 33. DSPI CMOS master mode – classic timing, CPHA = 1

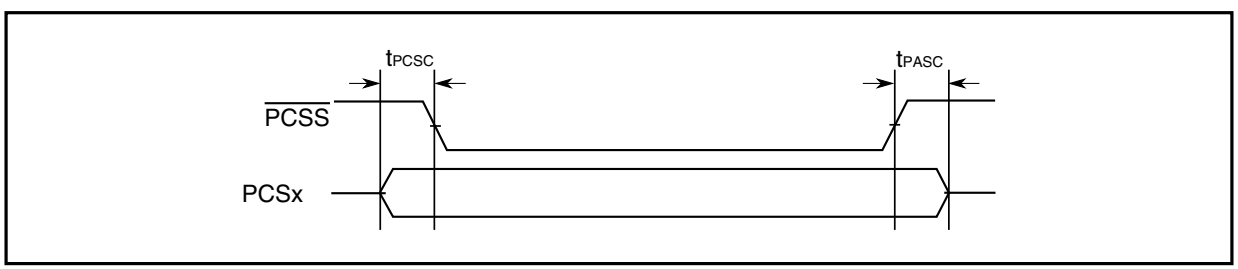

Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.2 DSPI CMOS Master Mode – Modified Timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

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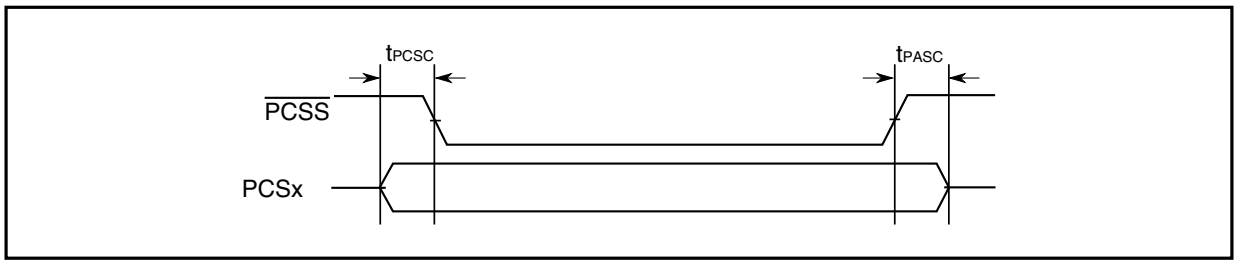

Figure 37. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.3 DSPI LVDS Master Mode – Modified Timing

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 25 pF differential	33.3	—	ns
2	t_{CSC}	PCS to SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	25 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=10b	50 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=01b	50 pF	($N^4 \times t_{SYS}$, [5]) – 32	—	ns
3	t_{ASC}	After SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
			PCS: PCR[SRC]=10b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
			PCS: PCR[SRC]=01b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
4	t_{SDC}	SCK duty cycle[7]	LVDS	15 pF to 25 pF differential	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ +2	ns
7	t_{SUI}	**SIN setup time**					
		SIN setup time to SCK CPHA = 0[8]	LVDS	15 pF to 25 pF differential	23 – ($P^9 \times t_{SYS}$, [5])	—	ns
		SIN setup time to SCK CPHA = 1[8]	LVDS	15 pF to 25 pF differential	23	—	ns
8	t_{HI}	**SIN hold time**					
		SIN hold time from SCK CPHA = 0[8]	LVDS	0 pF differential	–1 + ($P^9 \times t_{SYS}$, [5])	—	ns
		SIN hold time from SCK CPHA = 1[8]	LVDS	0 pF differential	–1	—	ns

Table continues on the next page...

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	**SOUT data valid time (after SCK edge)**					
		SOUT data valid time from SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}[5]	ns
		SOUT data valid time from SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	**SOUT data hold time (after SCK edge)**					
		SOUT data hold time after SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	–7.5 + t_{SYS}[5]	—	ns
		SOUT data hold time after SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min tSYS = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

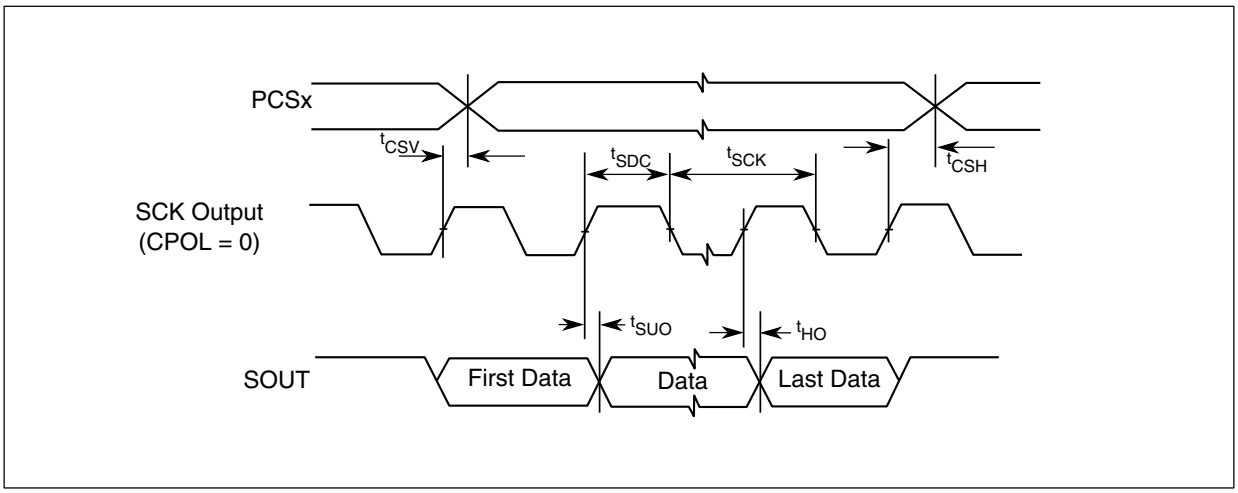

Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately