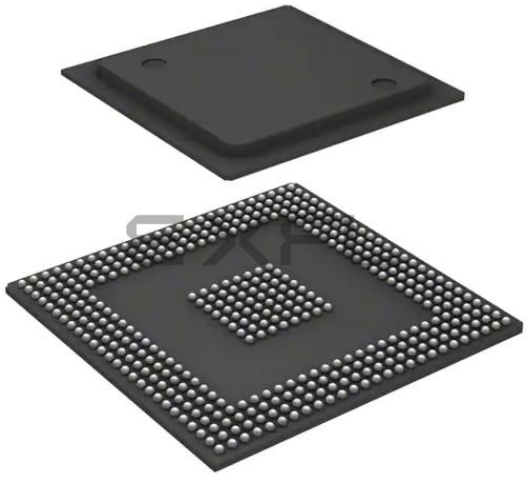

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777cdk3mme3

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability

1.2 Block diagram

The following figure shows a top-level block diagram of the MPC5777C. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch.

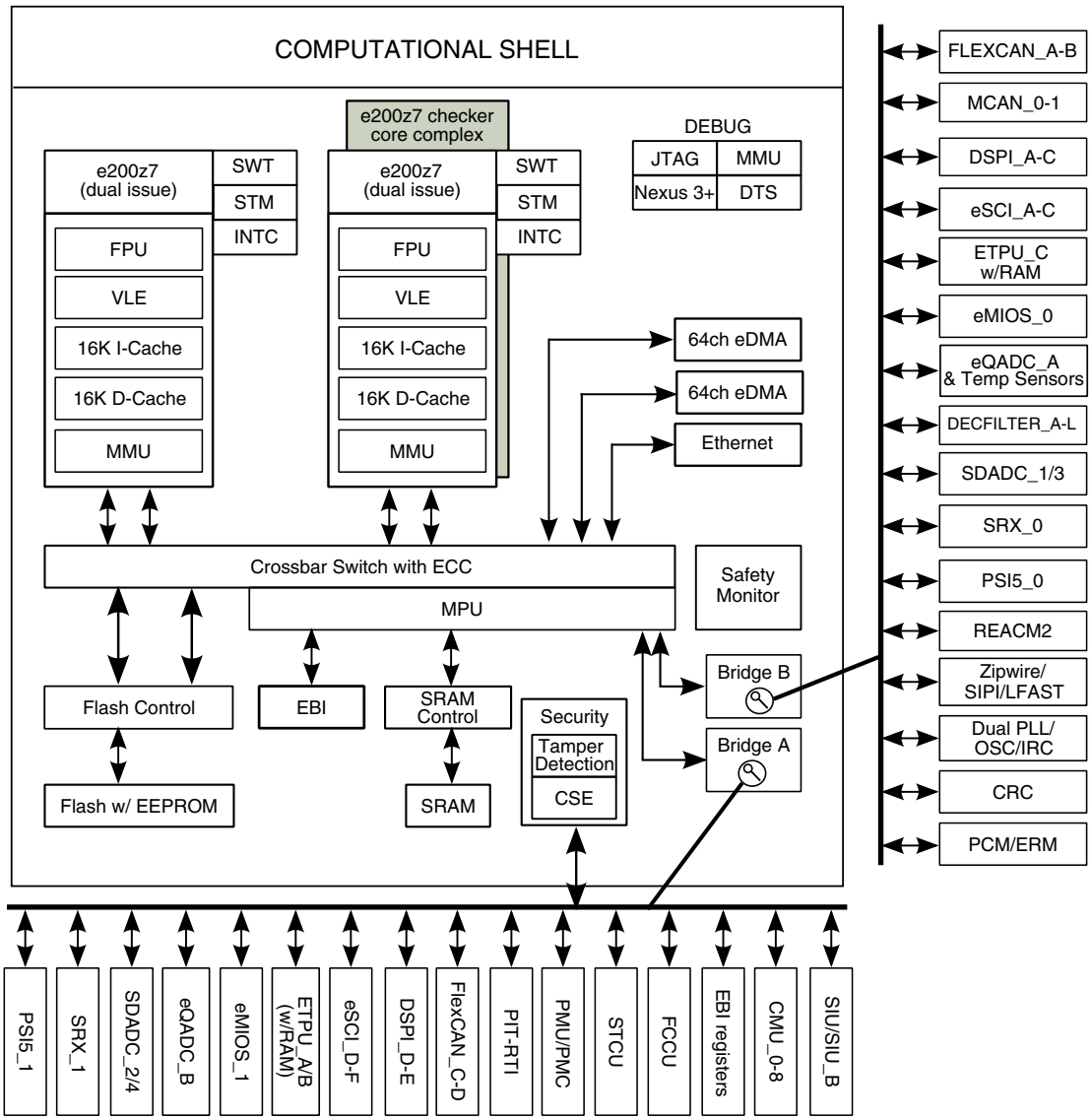

Figure 1. MPC5777C block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.

13. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
14. Full device lifetime without performance degradation
15. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
16. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
17. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
18. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

3.5 DC electrical specifications

NOTE

I_{DDA_MISC} is the sum of current consumption of IRC, I_{TRNG}, and I_{STBY} in the 5 V domain. IRC current is provided in the IRC specifications.

NOTE

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

Table 4. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD}	Operating current on the V_{DD} core logic supply[1]	LVD/HVD enabled, V_{DD} = 1.2 V to 1.32 V	—	0.65	1.35	A
		LVD/HVD disabled, V_{DD} = 1.2 V to 1.38 V	—	0.65	1.4	
I_{DD_PE}	Operating current on the V_{DD} supply for flash memory program/erase	—	—	—	85	mA
I_{DDPMC}	Operating current on the V_{DDPMC} supply[2]	Flash memory read	—	—	40	mA
		Flash memory program/erase	—	—	70	
		PMC only	—	—	35	
	Operating current on the V_{DDPMC} supply (internal core regulator bypassed)	Flash memory read	—	—	10	mA
		Flash memory program/erase	—	—	40	
		PMC only	—	—	5	
I_{REGCTL}	Core regulator DC current output on V_{REGCTL} pin	—	—	—	25	mA
I_{STBY}	Standby RAM supply current (T_J = 150°C)	1.08 V	—	—	1140	µA
		1.25 V to 5.5 V	—	—	1170	
I_{DD_PWR}	Operating current on the V_{DDPWR} supply	—	—	—	50	mA
I_{BG_REF}	Bandgap reference current consumption[3]		—	—	600	µA
I_{TRNG}	True Random Number Generator current	—	—	—	2.1	mA

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 5 shows output DC electrical characteristics.

2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

The following table shows the EBI CLKOUT, address, and control signal pad electrical characteristics. These pads can also be used for GPIO.

Table 10. GPIO and EBI CLKOUT, address, and control signal pad output buffer electrical characteristics (FC pads)

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications: valid for 3.0 V < V_{DDEx} < 3.6 V							
C_{DRV}	External bus load capacitance	PCR[DSC] = 01b		—	—	10	pF
		PCR[DSC] = 10b		—	—	20	
		PCR[DSC] = 11b		—	—	30	
f_{MAX_EBI}	External bus maximum operating frequency	C_{DRV} = 10/20/30 pF		—	—	66	MHz
GPIO and EBI Mode Output Specifications							
I_{OH_EBI}	GPIO and external bus pad output high current	V_{OH} = 0.8 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	30	—	—	mA
			PCR[DSC] = 10b	22	—	—	
			PCR[DSC] = 01b	13	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OH} = 0.8 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	16	—	—	
			PCR[DSC] = 10b	12	—	—	
			PCR[DSC] = 01b	7	—	—	
			PCR[DSC] = 00b	1	—	—	
I_{OL_EBI}	GPIO and external bus pad output low current	V_{OL} = 0.2 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	54	—	—	mA
			PCR[DSC] = 10b	25	—	—	
			PCR[DSC] = 01b	16	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OL} = 0.2 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	17	—	—	
			PCR[DSC] = 10b	14	—	—	
			PCR[DSC] = 01b	8	—	—	
			PCR[DSC] = 00b	1	—	—	
$t_{R\_F\_EBI}$	GPIO and external bus pad output transition time (rise/fall)	PCR[DSC] = 11b	C_L = 30 pF	—	—	1.5	ns
			C_L = 50 pF	—	—	2.4	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	1.5	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	1.85	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	45	
t_{PD_EBI}	GPIO and external bus pad output propagation delay time	PCR[DSC] = 11b	C_L = 30 pF	—	—	4.2	ns
			C_L = 50 pF	—	—	5.5	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	4.2	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	4.4	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	59	

Table 14. External oscillator (XOSC) electrical specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

1. This value is determined by the crystal manufacturer and board design.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
4. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating in a "low" transconductance range. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating in a "medium" or "high" transconductance range, the integrated load capacitor value is selected via software to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
5. Select a "low," "medium," or "high" setting using the UTEST Miscellaneous DCF client's XOSC_LF_EN and XOSC_EN_HIGH fields. "Low" is the setting commonly used for crystals at 8 MHz, "medium" is commonly used for crystals greater than 8 MHz to 20 MHz, and "high" is commonly used for crystals greater than 20 MHz to 40 MHz. However, the user must characterize carefully to determine the best g_m setting for the intended application because crystal load capacitance, board layout, and other factors affect the g_m value that is needed. The user may need an additional Rshunt to optimize g_m depending on the system environment. Use of overtone crystals is not recommended.
6. Amplitude on the EXTAL pin after startup is determined by the ALC block (that is, the Automatic Level Control Circuit). The function of the ALC is to provide high drive current during oscillator startup, while reducing current after oscillation to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
7. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 7.

Table 15. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
00000	1.8
00001	2.8
00010	3.7
00011	4.6
00100	5.6
00101	6.5
00110	7.4
00111	8.4
01000	9.3
01001	10.2
01010	11.2
01011	12.1
01100	13.0
01101	13.9

Table continues on the next page...

Table 15. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
01110	14.9
01111	15.8

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the die and package capacitances given by C_{S_XTAL}/C_{S_EXTAL} in Table 14.

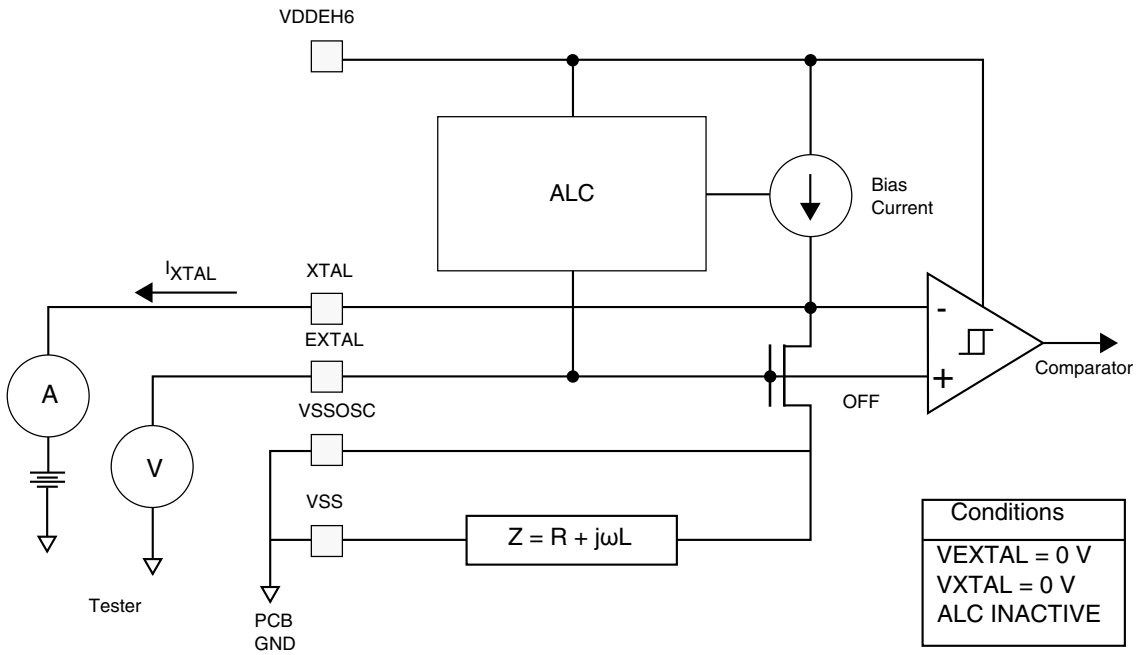

Figure 7. Test circuit

Table 16. Internal RC (IRC) oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRC target frequency	—	—	16	—	MHz
δf_{var_T}	IRC frequency variation	T < 150 °C	–8	—	8	%

3.8 Analog-to-Digital Converter (ADC) electrical specifications

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

The SMPS regulator characteristics appear in the following table.

Table 27. SMPS electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SMPS_{CLOCK}$	SMPS oscillator frequency	Trimmed	825	1000	1220	kHz
$SMPS_{SLOPE}$	SMPS soft-start ramp slope	—	0.01	0.025	0.05	V/µs
$SMPS_{EFF}$	SMPS typical efficiency	—	—	70	—	%

3.11.2 Power management integration

To ensure correct functionality of the device, use the following recommended integration scheme for LDO mode.

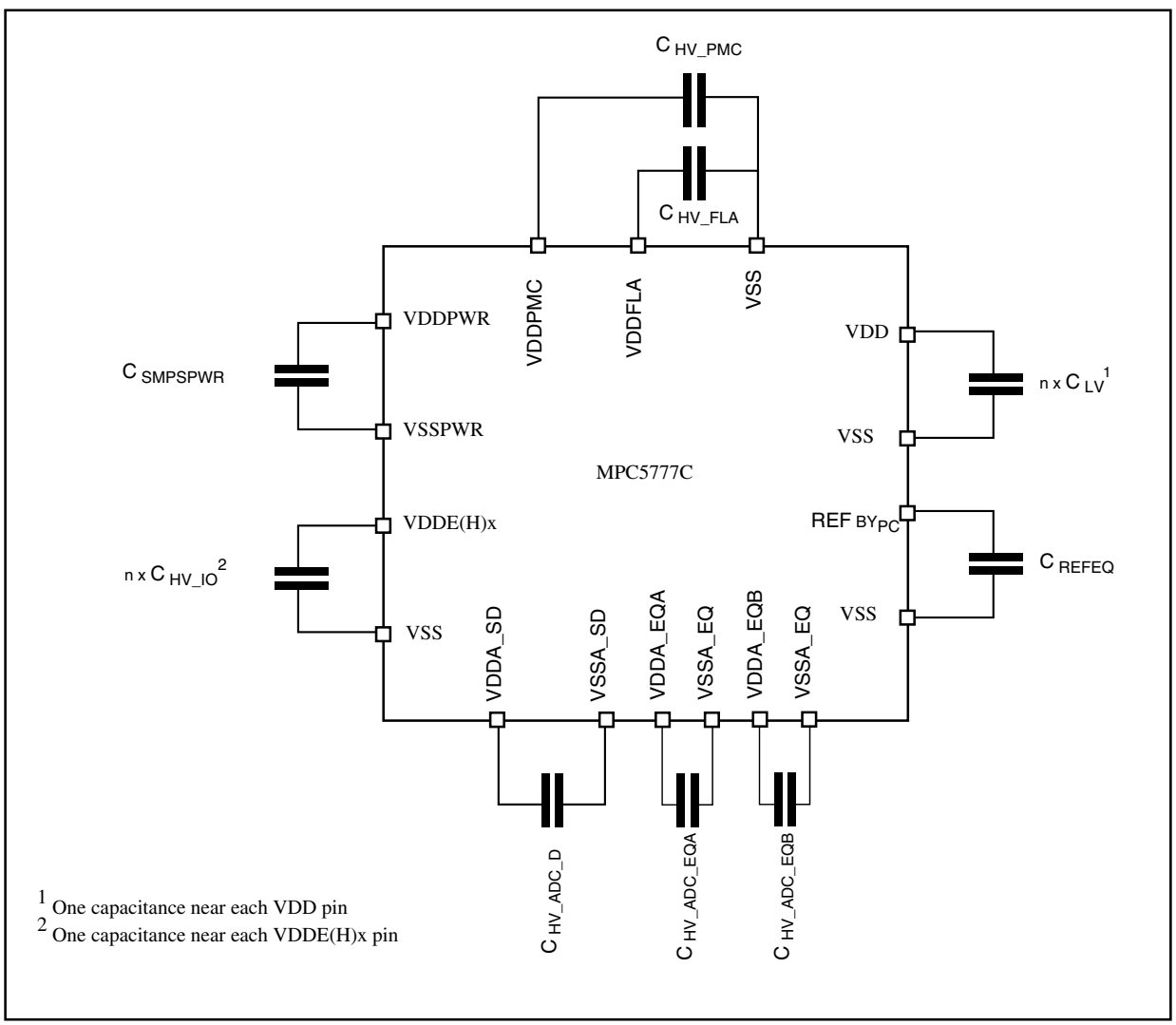

Figure 14. Recommended supply pin circuits

Table 29. Voltage monitor electrical characteristics[1, 2] (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR_HV	HV V_{DDPMC} supply power on reset threshold	Rising voltage (powerup)	N/A	No	Enab.	2444	2600	2756	mV
		Falling voltage (power down)				2424	2580	2736	
LVD_HV	HV internal V_{DDPMC} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2946	3010	3066	
		Falling voltage (trimmed)				2934	2998	3044	
HVD_HV	HV internal V_{DDPMC} supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	5696	5860	5968	mV
		Falling voltage				5666	5830	5938	
LVD_FLASH	FLASH supply low voltage monitoring[6]	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2956	3010	3053	
		Falling voltage (trimmed)				2944	2998	3041	
HVD_FLASH	FLASH supply high voltage monitoring[6]	Rising voltage	4bit	Yes	Disab.	3456	3530	3584	mV
		Falling voltage				3426	3500	3554	
LVD_IO	Main I/O V_{DDEH1} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	3250	3350	3488	mV
		Falling voltage (untrimmed)				3220	3320	3458	
		Rising voltage (trimmed)				3347	3420	3468	
		Falling voltage (trimmed)				3317	3390	3438	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	µs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	µs

1. LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed; LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.
2. HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed; HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.
3. POR098_c threshold is an untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
6. V_{DDFLA} range is guaranteed when internal flash memory regulator is used.

3.11.4 Power sequencing requirements

Requirements for power sequencing include the following.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

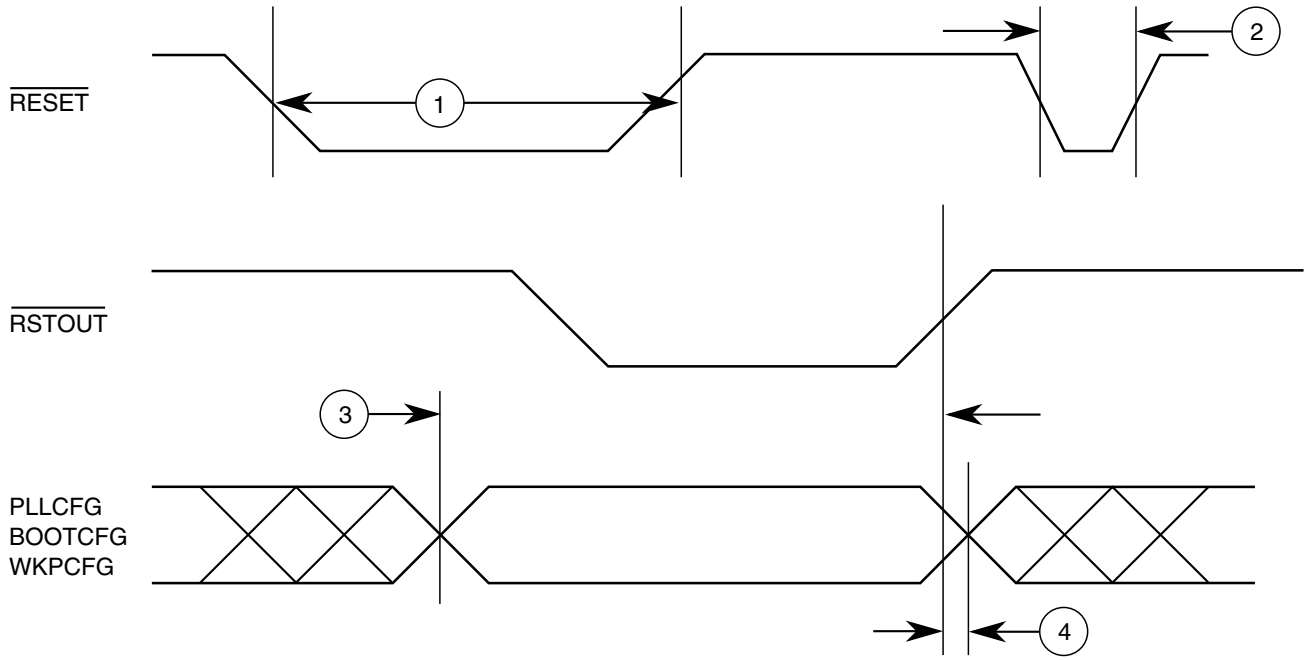

Figure 18. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

Table 37. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{RDY}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

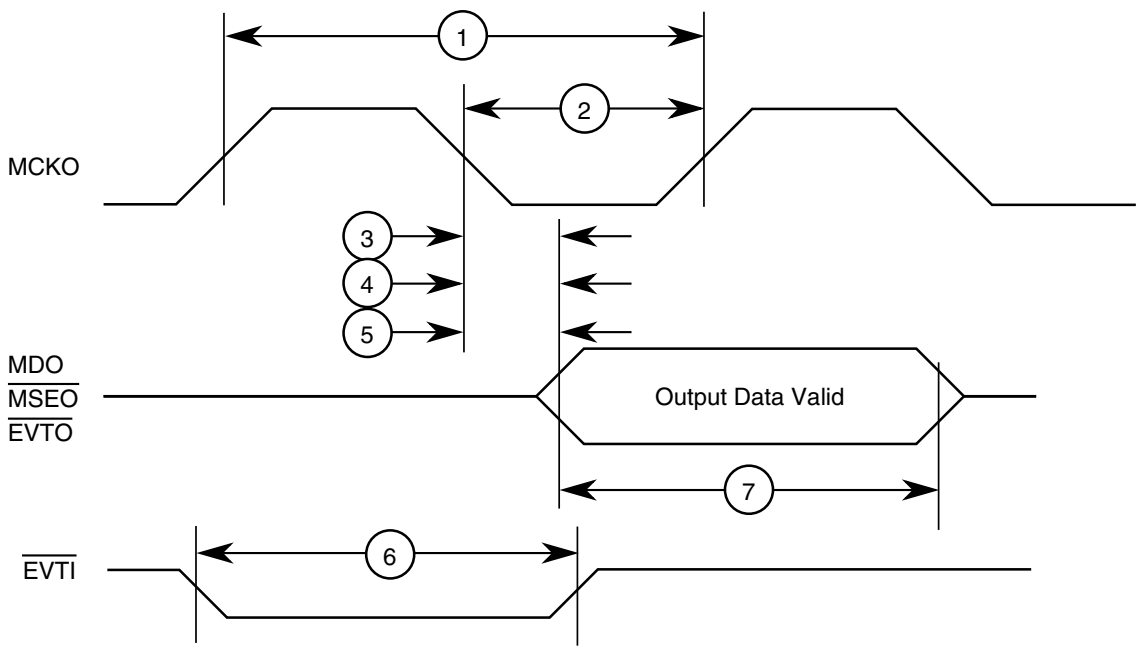

Figure 23. Nexus timings

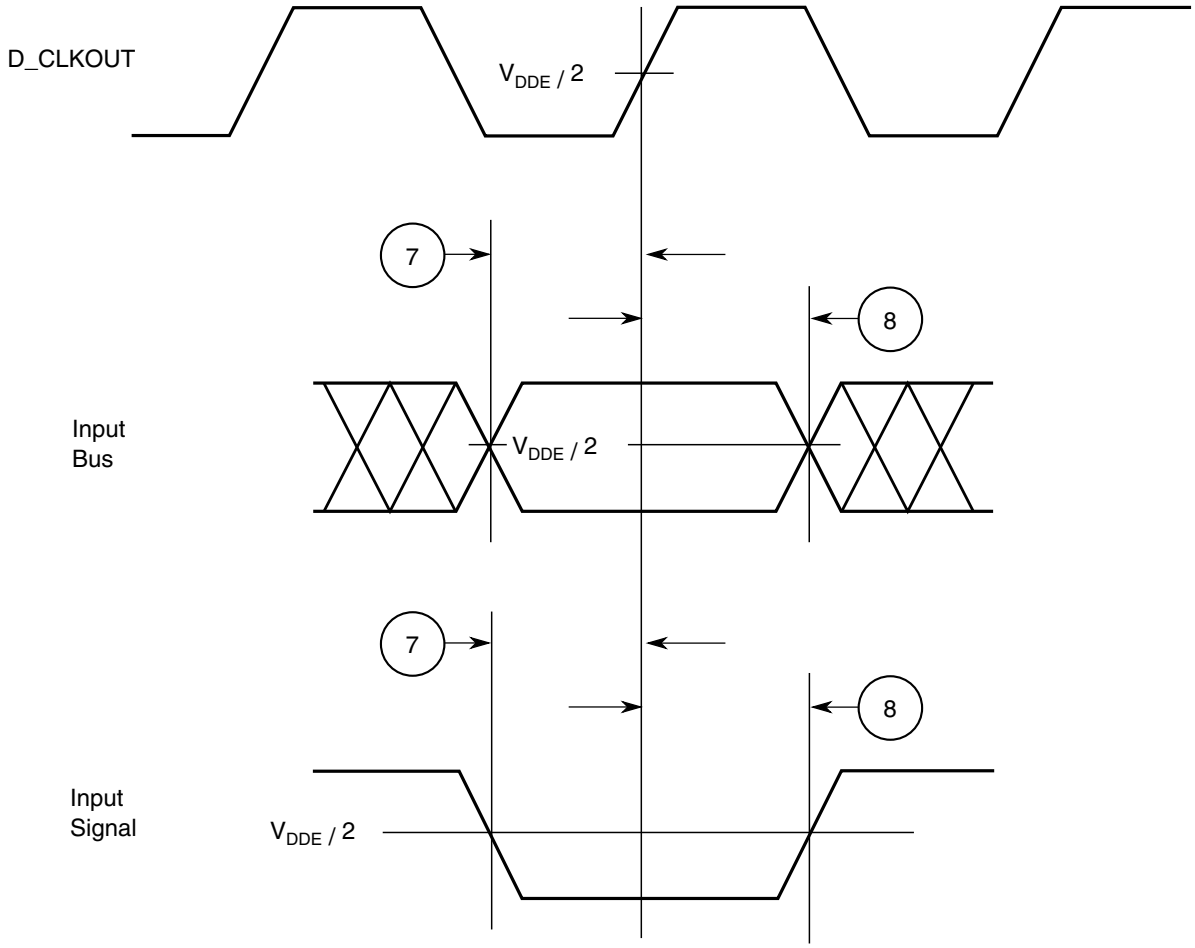

Figure 27. Synchronous input timing

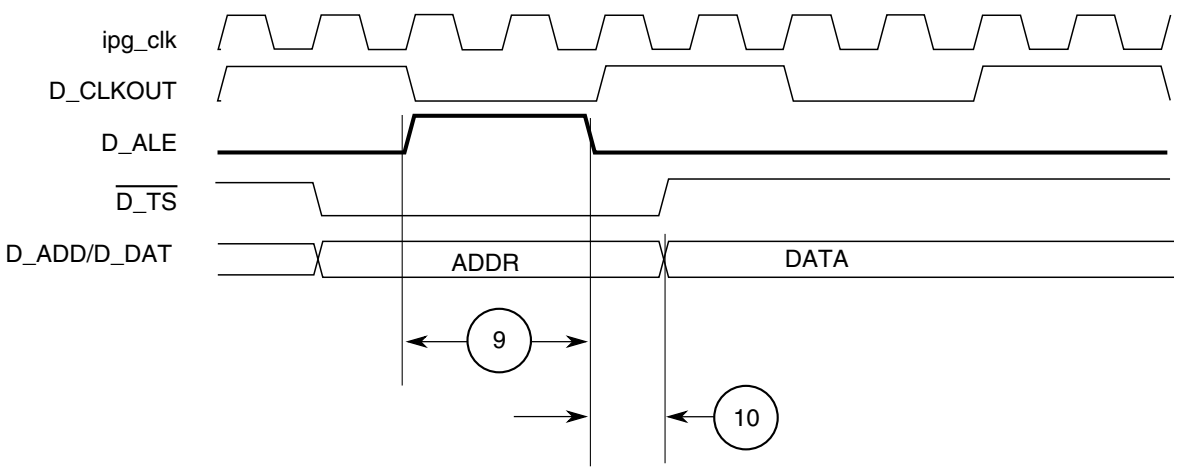

Figure 28. ALE signal timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

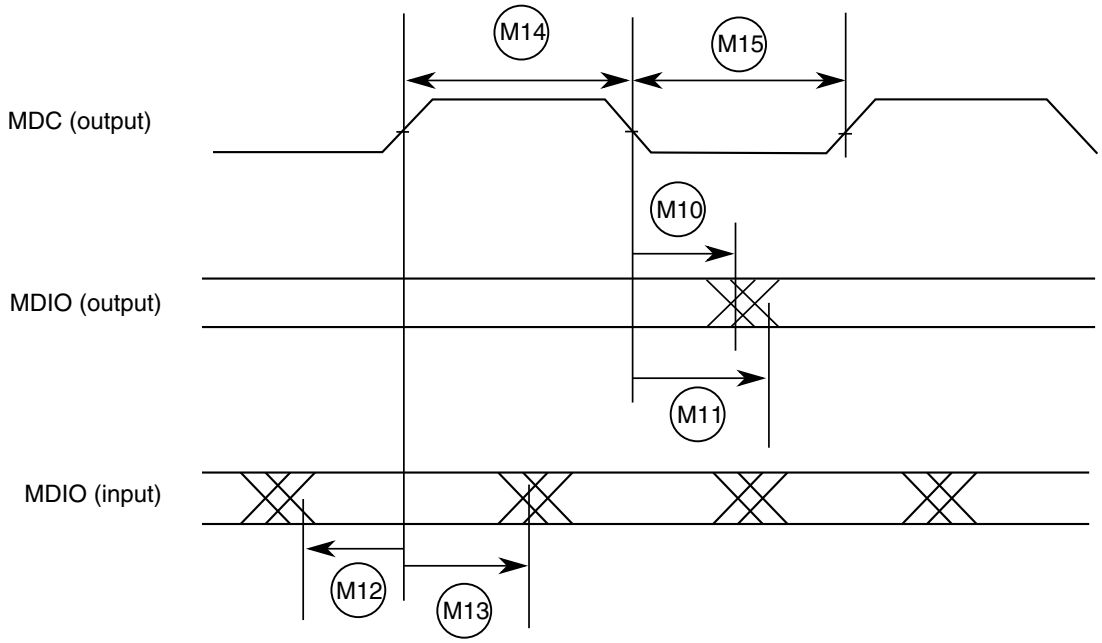

Figure 44. MII serial management channel timing diagram

3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 52. RMII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.

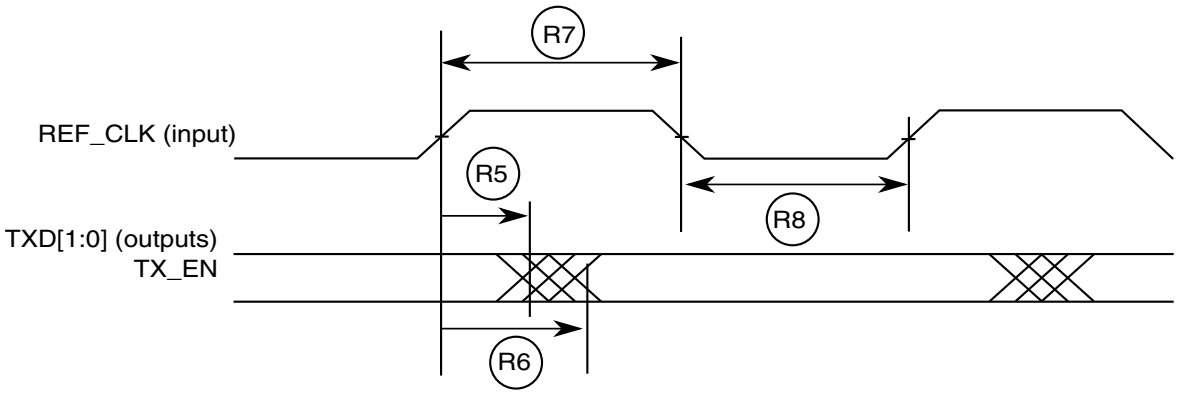

Figure 46. RMII transmit signal timing diagram

4 Package information

To find the package drawing for each package, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
416-ball MAPBGA	98ASA00562D
516-ball MAPBGA	98ASA00623D

4.1 Thermal characteristics

Table 54. Thermal characteristics, 416-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.8	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	19.6	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.1	°C/W
Junction to Board [4]	$R_{\Theta JB}$	9.5	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 55. Thermal characteristics, 516-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.5	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	20.0	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.5	°C/W
Junction to Board [4]	$R_{\Theta JB}$	8.8	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.1 General notes for thermal characteristics

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

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