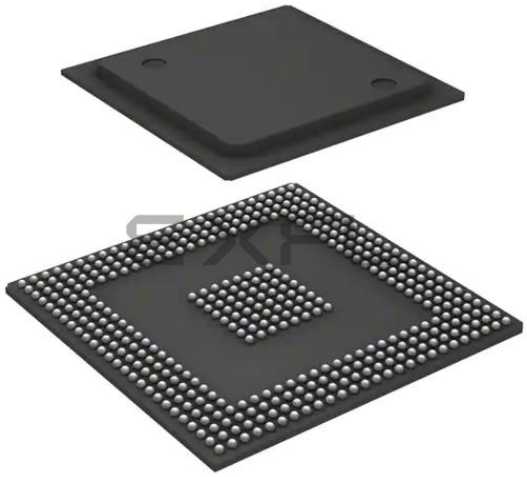

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z7 |
| Core Size | 32-Bit Tri-Core |
| Speed | 264MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI |
| Peripherals | DMA, LVD, POR, Zipwire |
| Number of I/O | - |
| Program Memory Size | 8MB (8M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16b Sigma-Delta, eQADC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 416-BGA |
| Supplier Device Package | 416-MAPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777cdk3mme3r |

**Table 1. Absolute maximum ratings (continued)**

| Symbol | Parameter | Conditions[1] | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| MSL | Moisture sensitivity level[11] | — | — | 3 | — |

1. Voltages are referred to $V_{SS}$ if not specified otherwise
2. Allowed 1.45 V – 1.5 V for 60 seconds cumulative time at maximum $T_J$ = 150 °C; remaining time as defined in note 3 and note 4
3. Allowed 1.375 V – 1.45 V for 10 hours cumulative time at maximum $T_J$ = 150 °C; remaining time as defined in note 4
4. 1.32 V – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum $T_J$ = 150 °C
5. Allowed 5.5 V – 6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J$ = 150 °C; remaining time at or below 5.5 V
6. Allowed 3.6 V – 4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J$ = 150 °C; remaining time at or below 3.6 V
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DDEx}/V_{DDEHx}$ power segment is defined as one or more GPIO pins located between two $V_{DDEx}/V_{DDEHx}$ supply pins.
9. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.
10. Solder profile per IPC/JEDEC J-STD-020D
11. Moisture sensitivity per JEDEC test method A112

## 3.2 Electromagnetic interference (EMI) characteristics

Test reports with EMC measurements to IC-level IEC standards are available on request.

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to nxp.com and perform a keyword search for "radiated emissions."

## 3.3 Electrostatic discharge (ESD) characteristics

**Table 2. ESD Ratings[1, 2]**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $V_{HBM}$ | ESD for Human Body Model (HBM) | All pins | 2000 | V |
| $V_{CDM}$ | ESD for Charged Device Model (CDM) | Corner pins | 750 | V |
| | | Non-corner pins | 500 | |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

13. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
14. Full device lifetime without performance degradation
15. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
16. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
17. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DDEx}/V_{DDEHx}$ power segment is defined as one or more GPIO pins located between two $V_{DDEx}/V_{DDEHx}$ supply pins.
18. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

## 3.5 DC electrical specifications

**NOTE**

$I_{DDA\_MISC}$ is the sum of current consumption of IRC, $I_{TRNG}$, and $I_{STBY}$ in the 5 V domain. IRC current is provided in the IRC specifications.

**NOTE**

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

**Table 4. DC electrical specifications**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{DD}$ | Operating current on the $V_{DD}$ core logic supply[1] | LVD/HVD enabled, $V_{DD}$ = 1.2 V to 1.32 V | — | 0.65 | 1.35 | A |
| | | LVD/HVD disabled, $V_{DD}$ = 1.2 V to 1.38 V | — | 0.65 | 1.4 | |
| $I_{DD\_PE}$ | Operating current on the $V_{DD}$ supply for flash memory program/erase | — | — | — | 85 | mA |
| $I_{DDPMC}$ | Operating current on the $V_{DDPMC}$ supply[2] | Flash memory read | — | — | 40 | mA |
| | | Flash memory program/erase | — | — | 70 | |
| | | PMC only | — | — | 35 | |
| | Operating current on the $V_{DDPMC}$ supply (internal core regulator bypassed) | Flash memory read | — | — | 10 | mA |
| | | Flash memory program/erase | — | — | 40 | |
| | | PMC only | — | — | 5 | |
| $I_{REGCTL}$ | Core regulator DC current output on $V_{REGCTL}$ pin | — | — | — | 25 | mA |
| $I_{STBY}$ | Standby RAM supply current ($T_J$ = 150°C) | 1.08 V | — | — | 1140 | µA |
| | | 1.25 V to 5.5 V | — | — | 1170 | |
| $I_{DD\_PWR}$ | Operating current on the $V_{DDPWR}$ supply | — | — | — | 50 | mA |
| $I_{BG\_REF}$ | Bandgap reference current consumption[3] | | — | — | 600 | µA |
| $I_{TRNG}$ | True Random Number Generator current | — | — | — | 2.1 | mA |

1. $I_{DD}$ measured on an application-specific pattern with all cores enabled at full frequency, $T_J$ = 40°C to 150°C. Flash memory program/erase current on the $V_{DD}$ supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of $h_{FE}$ of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

## 3.6 I/O pad specifications

The following table describes the different pad types on the chip.

**Table 5. I/O pad specification descriptions**

| Pad type | Description |
|---|---|
| General-purpose I/O pads | General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads |
| EBI pads | Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads |
| LVDS pads | Low Voltage Differential Signal interface pads |
| Input-only pads | Low-input-leakage pads that are associated with the ADC channels |

**NOTE**

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

**NOTE**

Throughout the I/O pad specifications, the symbol $V_{DDEx}$ represents all $V_{DDEx}$ and $V_{DDEHx}$ segments.

### 3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

**Table 13. PLL1 electrical characteristics**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{PLL1IN}$ | PLL1 input clock[1] | — | 38 | — | 78 | MHz |
| $\Delta_{PLL1IN}$ | PLL1 input clock duty cycle[1] | — | 35 | — | 65 | % |
| $f_{PLL1VCO}$ | PLL1 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL1PHI}$ | PLL1 output clock PHI | — | 4.762 | — | 264 | MHz |
| $t_{PLL1LOCK}$ | PLL1 lock time | — | — | — | 100 | µs |
| $\lvert\Delta_{PLL1PHISPJ}\rvert$ | PLL1_PHI single period peak-to-peak jitter | $f_{PLL1PHI}$ = 200 MHz, 6-sigma | — | — | 500[2] | ps |
| $f_{PLL1MOD}$ | PLL1 modulation frequency | — | — | — | 250 | kHz |
| $\lvert\delta_{PLL1MOD}\rvert$ | PLL1 modulation depth (when enabled) | Center spread | 0.25 | — | 2 | % |
| | | Down spread | 0.5 | — | 4 | % |
| $I_{PLL1}$ | PLL1 consumption | FINE LOCK state | — | — | 6 | mA |

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. Noise on the $V_{DD}$ supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the $V_{DD}$ supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

## 3.7.2 Oscillator electrical specifications

**NOTE**

All oscillator specifications in Table 14 are valid for $V_{DDEH6}$ = 3.0 V to 5.5 V.

**Table 14. External oscillator (XOSC) electrical specifications**

| Symbol | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $f_{XTAL}$ | Crystal frequency range | — | 8 | 40 | MHz |
| $t_{cst}$ | Crystal start-up time[1, 2] | $T_J$ = 150 °C | — | 5 | ms |
| $t_{rec}$ | Crystal recovery time[3] | — | — | 0.5 | ms |
| $V_{IHEXT}$ | EXTAL input high voltage (external reference) | $V_{REF}$ = 0.28 * $V_{DDEH6}$ | $V_{REF}$ + 0.6 | — | V |
| $V_{ILEXT}$ | EXTAL input low voltage (external reference) | $V_{REF}$ = 0.28 * $V_{DDEH6}$ | — | $V_{REF}$ – 0.6 | V |
| $C_{S\_EXTAL}$ | Total on-chip stray capacitance on EXTAL pin[4] | 416-ball MAPBGA | 2.3 | 3.0 | pF |
| | | 516-ball MAPBGA | 2.1 | 2.8 | |
| $C_{S\_XTAL}$ | Total on-chip stray capacitance on XTAL pin[4] | 416-ball MAPBGA | 2.3 | 3.0 | pF |
| | | 516-ball MAPBGA | 2.2 | 2.9 | |
| $g_m$ | Oscillator transconductance[5] | Low | 3 | 10 | mA/V |
| | | Medium | 10 | 27 | |
| | | High | 12 | 35 | |

*Table continues on the next page...*

5. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than $V_{RH}$ and $000 for values less than $V_{RL}$. Other channels are not affected by non-disruptive conditions.
6. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
7. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.
8. Condition applies to two adjacent pins at injection limits.
9. Performance expected with production silicon.
10. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.
11. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
12. TUE does not apply to differential conversions.
13. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
14. Guaranteed 10-bit monotonicity.
15. At $V_{RH\_EQ} - V_{RL\_EQ} = 5.12$ V, one LSB = 1.25 mV.

## 3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

**NOTE**

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

**Table 18. SDADC electrical specifications**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IN}$ | ADC input signal | — | 0 | — | $V_{DDA\_SD}$ | V |
| $V_{IN\_PK2PK}$[1] | Input range peak to peak<br>$V_{IN\_PK2PK} = V_{INP}$[2] – $V_{INM}$,[3] | Single ended<br>$V_{INM} = V_{RL\_SD}$ | $V_{RH\_SD}$/GAIN | | | V |
| | | Single ended<br>$V_{INM} = 0.5*V_{RH\_SD}$<br>GAIN = 1 | ±0.5*$V_{RH\_SD}$ | | | |
| | | Single ended<br>$V_{INM} = 0.5*V_{RH\_SD}$<br>GAIN = 2,4,8,16 | ±$V_{RH\_SD}$/GAIN | | | |
| | | Differential<br>$0 < V_{IN} < V_{DDEx}$ | ±$V_{RH\_SD}$/GAIN | | | |
| $f_{ADCD\_M}$ | SD clock frequency[4] | — | 4 | 14.4 | 16 | MHz |
| $f_{ADCD\_S}$ | Conversion rate | — | — | — | 333 | Ksps |
| — | Oversampling ratio | Internal modulator | 24 | — | 256 | — |
| RESOLUTION | SD register resolution[5] | 2's complement notation | 16 | | | bit |

*Table continues on the next page...*

## Table 18. SDADC electrical specifications (continued)

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $SNR_{DIFF150}$ | Signal to noise ratio in differential mode, 150 Ksps output rate | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 1 | 80 | — | — | dB |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 2 | 77 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 4 | 74 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 8 | 71 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 16 | 68 | — | — | |
| $SNR_{DIFF333}$ | Signal to noise ratio in differential mode, 333 Ksps output rate | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 1 | 71 | — | — | dB |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 2 | 70 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 4 | 68 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 8 | 65 | — | — | |
| | | 4.5 V < $V_{DDA\_SD}$ < 5.5 V[8, 9]<br>$V_{RH\_SD}$ = $V_{DDA\_SD}$<br>GAIN = 16 | 62 | — | — | |

*Table continues on the next page...*

**NOTE**

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, $V_{DDPMC}$ and $V_{DDPWR}$ must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. $V_{DDPWR}$ is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, $V_{DDFLA}$ must also be star routed and shorted to $V_{DDPWR}$ and $V_{DDPMC}$. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal $V_{DDFLA}$ regulator. Consequently, $V_{DDFLA}$ is supplied externally.
2. $V_{DDA\_MISC}$: IRC operation is required to provide the clock for chip startup.
   - The $V_{DDPMC}$, $V_{DD}$, and $V_{DDEH1}$ (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, $V_{DDA\_MISC}$ must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both $V_{DDEH1}$ and $V_{DDA\_MISC}$. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple $V_{DDEx}$ supplies can be powered up in any order.

   During any time when $V_{DD}$ is powered up but $V_{DDEx}$ is not yet powered up: pad outputs are unpowered.

   During any time when $V_{DDEx}$ is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up $V_{DDA\_EQ}$ before $V_{DD}$. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, $V_{DDPMC}$ and $V_{DDPWR}$ supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

# 3.12 Flash memory specifications

## 3.12.1 Flash memory program and erase specifications

**NOTE**

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

**Table 30. Flash memory program and erase specifications**

| Symbol | Characteristic[1] | Typ[2] | Factory Programming[3, 4] | | Field Update | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life[5] | Lifetime Max[6] | | |
| | | | 20°C ≤$T_A$ ≤30°C | -40°C ≤$T_J$ ≤150°C | -40°C ≤$T_J$ ≤150°C | ≤ 1,000 cycles | ≤ 250,000 cycles | |
| $t_{dwpgm}$ | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | | µs |
| $t_{ppgm}$ | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | | µs |
| $t_{qppgm}$ | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | | µs |
| $t_{16kers}$ | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | | ms |
| $t_{16kpgm}$ | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | | ms |
| $t_{32kers}$ | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | | ms |
| $t_{32kpgm}$ | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | | ms |
| $t_{64kers}$ | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | | ms |
| $t_{64kpgm}$ | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | | ms |
| $t_{256kers}$ | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| $t_{256kpgm}$ | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ $T_J$ ≤ 150°C, full spec voltage.

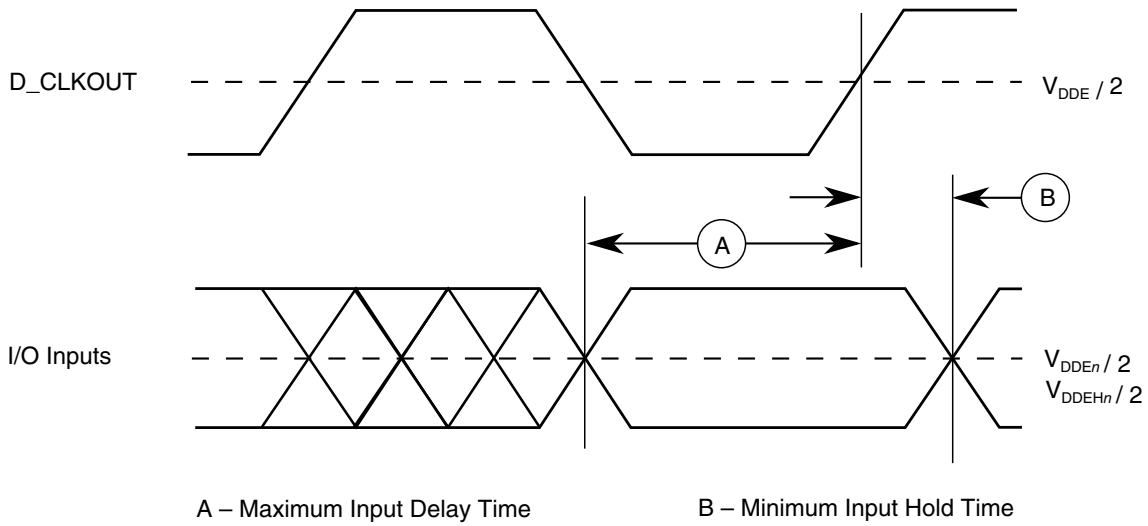



**Figure 17. Generic input setup/hold timing**

## 3.13.2 Reset and configuration pin timing

**Table 35. Reset and configuration pin timing[1]**

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $\overline{\text{RESET}}$ Pulse Width | $t_{RPW}$ | 10 | — | $t_{cyc}$[2] |
| 2 | $\overline{\text{RESET}}$ Glitch Detect Pulse Width | $t_{GPW}$ | 2 | — | $t_{cyc}$[2] |
| 3 | PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid | $t_{RCSU}$ | 10 | — | $t_{cyc}$[2] |
| 4 | PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid | $t_{RCH}$ | 0 | — | $t_{cyc}$[2] |

1. Reset timing specified at: $V_{DDEH}$ = 3.0 V to 5.25 V, $V_{DD}$ = 1.08 V to 1.32 V, TA = TL to TH.
2. For further information on $t_{cyc}$, see Table 3.

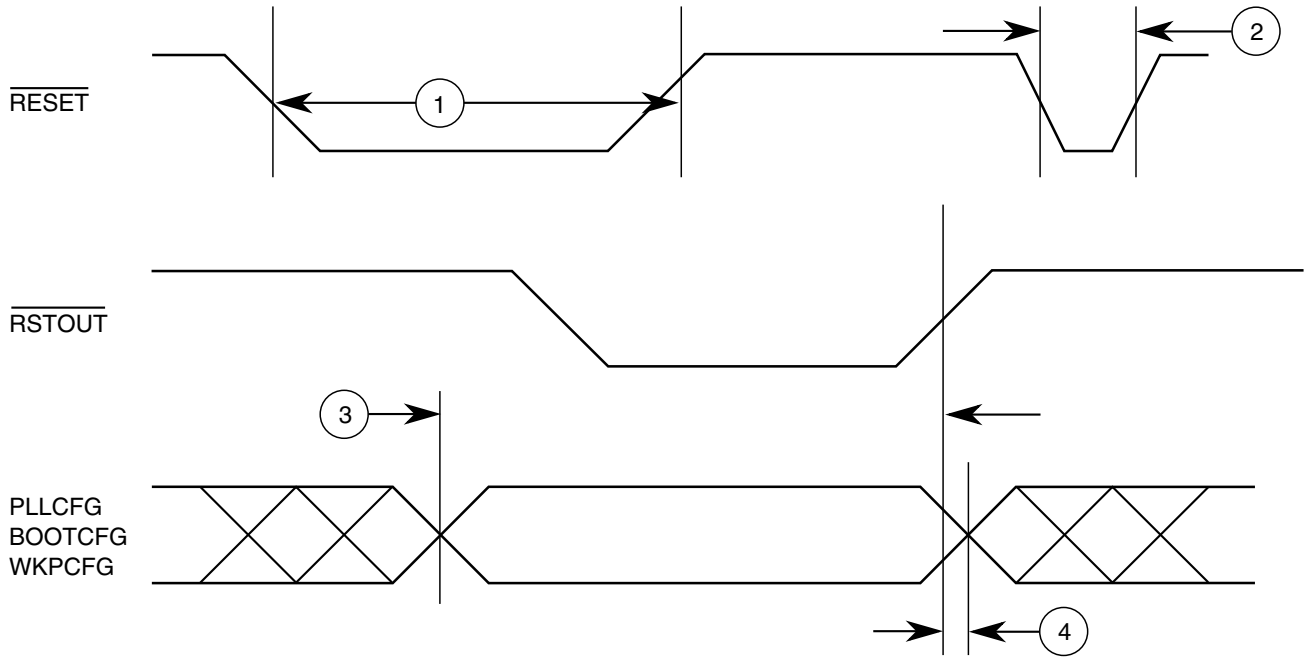



**Figure 18. Reset and configuration pin timing**

## 3.13.3 IEEE 1149.1 interface timing

### Table 36. JTAG pin AC electrical characteristics[1]

| # | Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | $t_{JCYC}$ | TCK cycle time | 100 | — | ns |
| 2 | $t_{JDC}$ | TCK clock pulse width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK rise and fall times (40%–70%) | — | 3 | ns |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | TMS, TDI data setup time | 5 | — | ns |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | TMS, TDI data hold time | 5 | — | ns |
| 6 | $t_{TDOV}$ | TCK low to TDO data valid | — | 16[2] | ns |
| 7 | $t_{TDOI}$ | TCK low to TDO data invalid | 0 | — | ns |
| 8 | $t_{TDOHZ}$ | TCK low to TDO high impedance | — | 15 | ns |
| 9 | $t_{JCMPPW}$ | JCOMP assertion time | 100 | — | ns |
| 10 | $t_{JCMPS}$ | JCOMP setup time to TCK low | 40 | — | ns |
| 11 | $t_{BSDV}$ | TCK falling edge to output valid | — | 600[3] | ns |
| 12 | $t_{BSDVZ}$ | TCK falling edge to output valid out of high impedance | — | 600 | ns |
| 13 | $t_{BSDHZ}$ | TCK falling edge to output high impedance | — | 600 | ns |
| 14 | $t_{BSDST}$ | Boundary scan input valid to TCK rising edge | 15 | — | ns |
| 15 | $t_{BSDHT}$ | TCK rising edge to boundary scan input invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

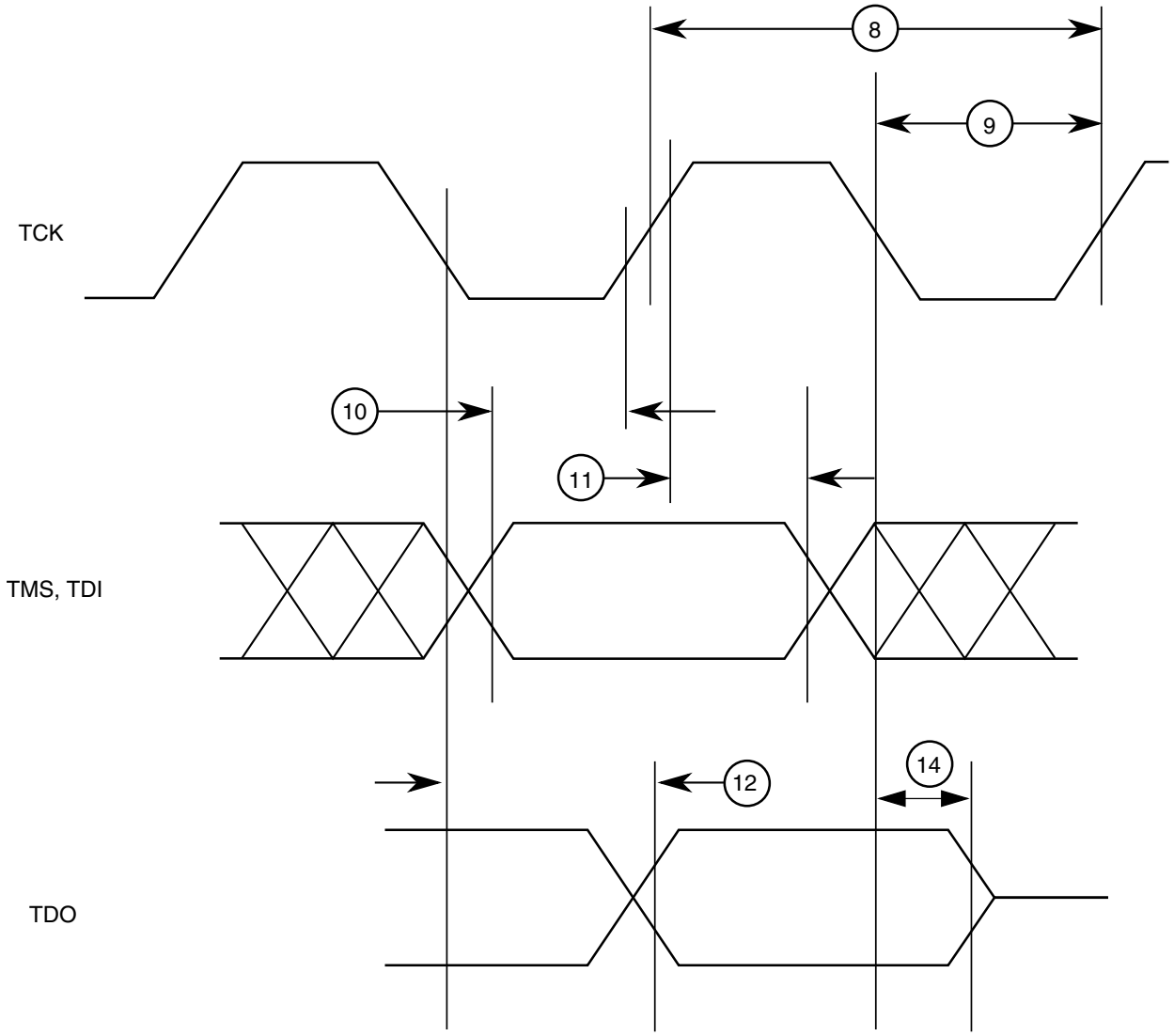



**Figure 24. Nexus TCK, TDI, TMS, TDO Timing**

## 3.13.5 External Bus Interface (EBI) timing

**Table 38. Bus operation timing[1]**

| Spec | Characteristic | Symbol | 66 MHz (Ext. bus freq.)[2, 3] | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| 1 | D_CLKOUT Period | $t_C$ | 15.2 | — | ns | Signals are measured at 50% $V_{DDE}$. |
| 2 | D_CLKOUT Duty Cycle | $t_{CDC}$ | 45% | 55% | $t_C$ | — |
| 3 | D_CLKOUT Rise Time | $t_{CRT}$ | — | —[4] | ns | — |
| 4 | D_CLKOUT Fall Time | $t_{CFT}$ | — | —[4] | ns | — |

*Table continues on the next page...*

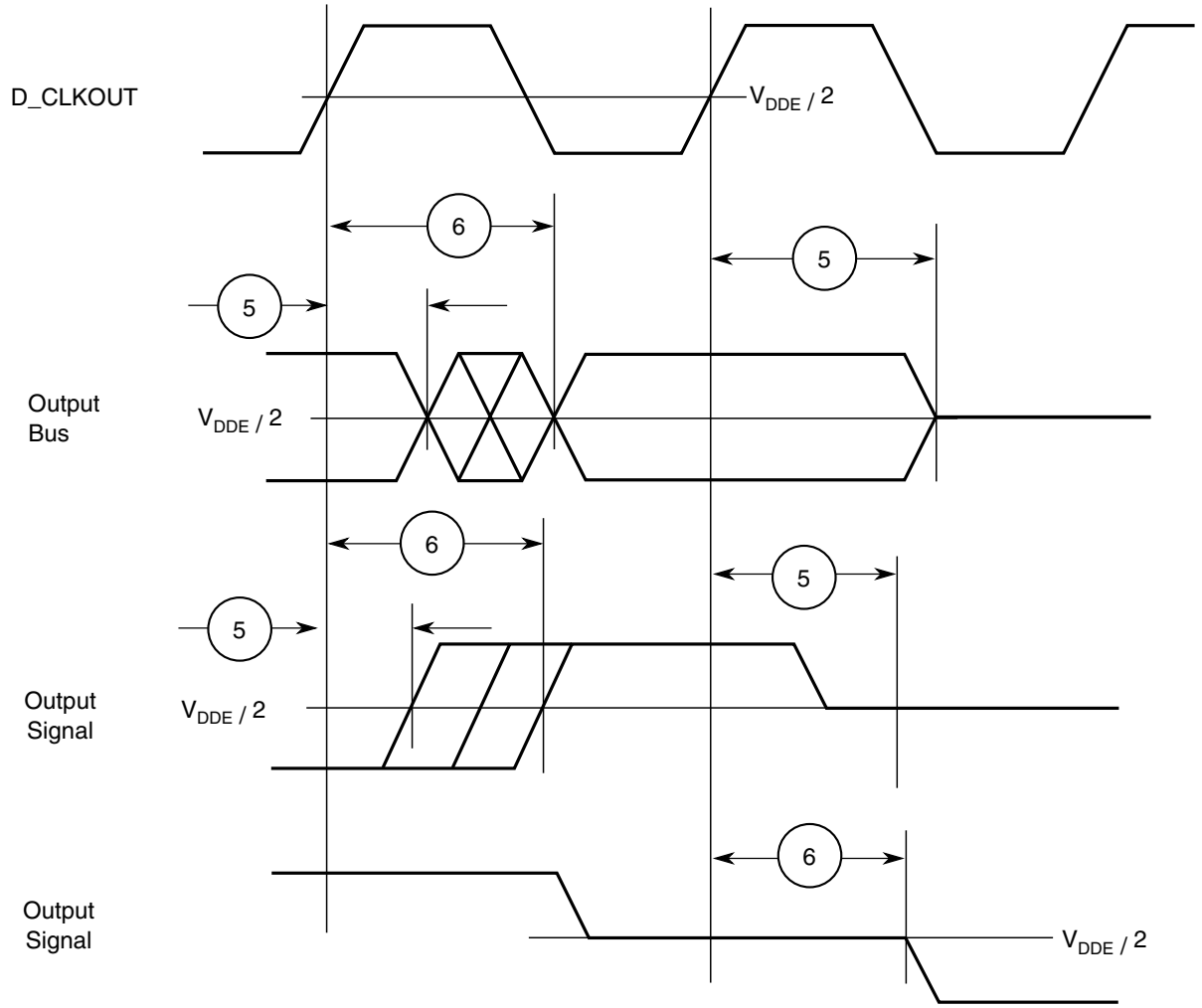



**Figure 26. Synchronous output timing**

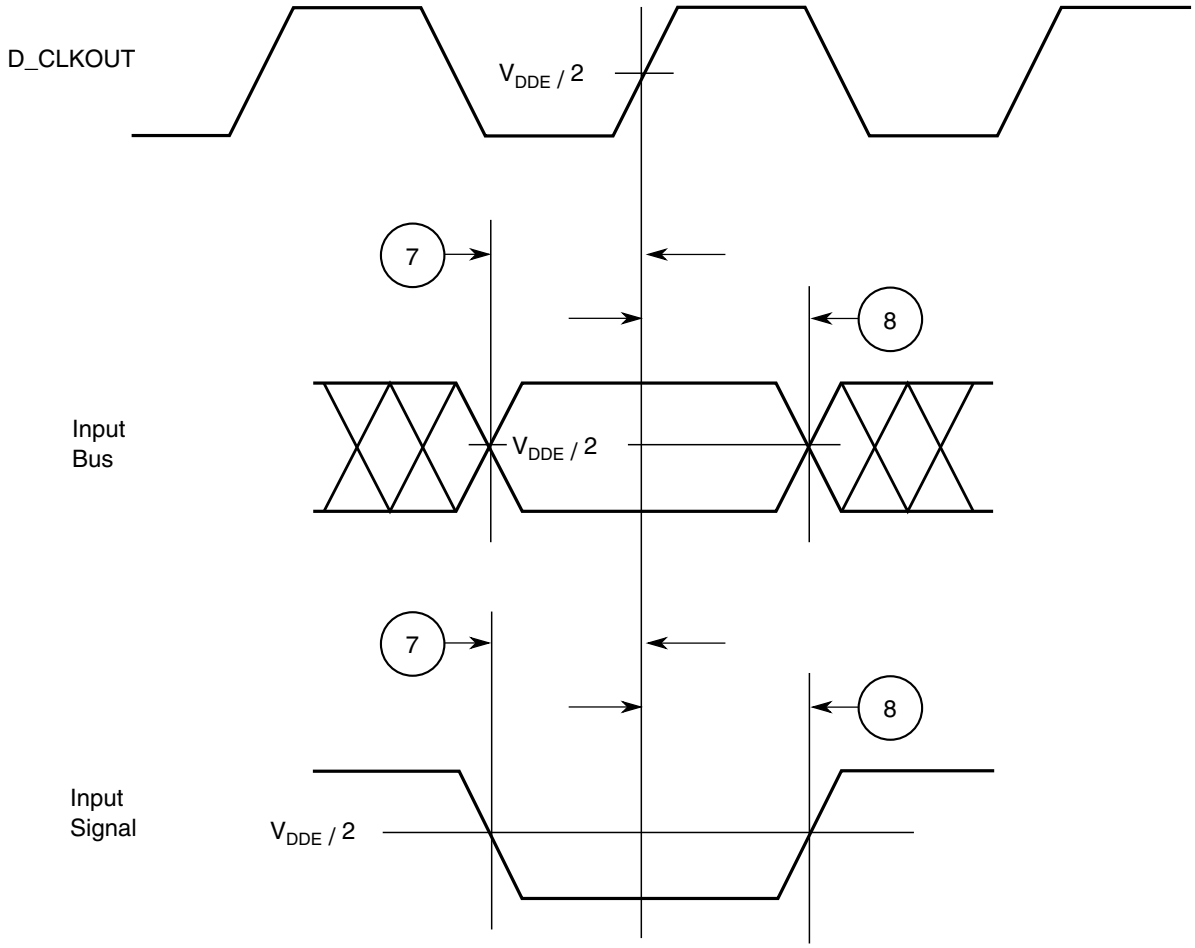



**Figure 27. Synchronous input timing**

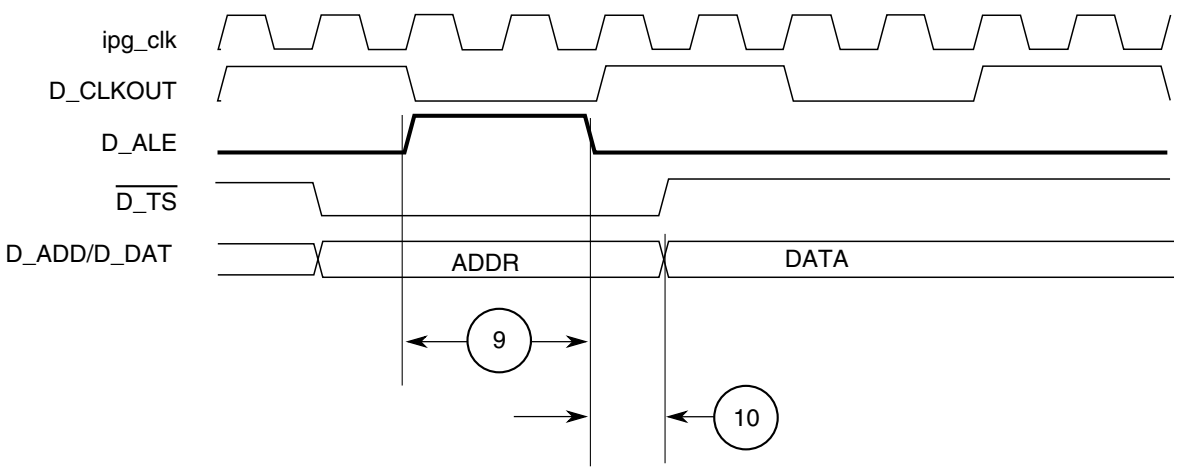



**Figure 28. ALE signal timing**

## 3.13.6 External interrupt timing (IRQ/NMI pin)

### Table 39. External Interrupt timing[1]

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | IRQ/NMI Pulse Width Low | $t_{IPWL}$ | 3 | — | $t_{cyc}$[2] |
| 2 | IRQ/NMI Pulse Width High | $t_{IPWH}$ | 3 | — | $t_{cyc}$[2] |
| 3 | IRQ/NMI Edge to Edge Time[3] | $t_{ICYC}$ | 6 | — | $t_{cyc}$[2] |

1. IRQ/NMI timing specified at $V_{DD}$ = 1.08 V to 1.32 V, $V_{DDEH}$ = 3.0 V to 5.5 V, $T_A = T_L$ to $T_H$.
2. For further information on $t_{cyc}$, see Table 3.
3. Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

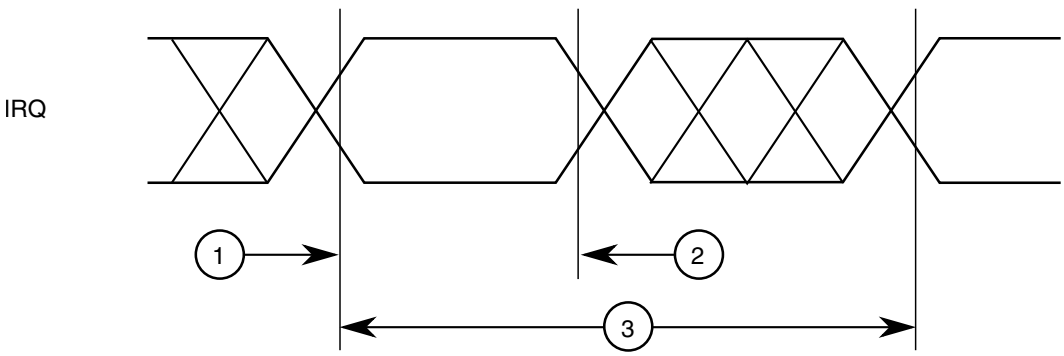



**Figure 29. External interrupt timing**

## 3.13.7 eTPU timing

### Table 40. eTPU timing[1]

| Spec | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | eTPU Input Channel Pulse Width | $t_{ICPW}$ | 4 | — | $t_{CYC\_ETPU}$[2] |
| 2 | eTPU Output Channel Pulse Width | $t_{OCPW}$ | 1[3] | — | $t_{CYC\_ETPU}$[2] |

1. eTPU timing specified at $V_{DD}$ = 1.08 V to 1.32 V, $V_{DDEH}$ = 3.0 V to 5.5 V, $T_A = T_L$ to $T_H$, and $C_L$ = 200 pF with SRC = 0b00.
2. For further information on $t_{CYC\_ETPU}$, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

## 3.13.9 DSPI timing with CMOS and LVDS pads

**NOTE**

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 42. Timing specifications are shown in Table 43, Table 44, Table 45, Table 46, and Table 47.

**Table 42. DSPI channel frequency support**

| DSPI use mode | | Max usable frequency (MHz)[1, 2] |
|---|---|---|
| CMOS (Master mode) | Full duplex – Classic timing (Table 43) | 17 |
| | Full duplex – Modified timing (Table 44) | 30 |
| | Output only mode (SCK/SOUT/PCS) (Table 43 and Table 44) | 30 |
| | Output only mode TSB mode (SCK/SOUT/PCS) (Table 47) | 30 |
| LVDS (Master mode) | Full duplex – Modified timing (Table 45) | 30 |
| | Output only mode TSB mode (SCK/SOUT/PCS) (Table 46) | 40 |

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

### 3.13.9.1 DSPI master mode full duplex timing with CMOS and LVDS pads

#### 3.13.9.1.1 DSPI CMOS Master Mode — Classic Timing

**Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]**

| # | Symbol | Characteristic | Condition[2] | | Value[3] | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Pad drive[4] | Load ($C_L$) | Min | Max | |
| 1 | $t_{SCK}$ | SCK cycle time | PCR[SRC]=11b | 25 pF | 33.0 | — | ns |
| | | | PCR[SRC]=10b | 50 pF | 80.0 | — | |
| | | | PCR[SRC]=01b | 50 pF | 200.0 | — | |
| 2 | $t_{CSC}$ | PCS to SCK delay | PCR[SRC]=11b | 25 pF | ($N^5 \times t_{SYS}$, [6]) – 16 | — | ns |
| | | | PCR[SRC]=10b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 16 | — | |
| | | | PCR[SRC]=01b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 18 | — | |
| | | | PCS: PCR[SRC]=01b<br>SCK: PCR[SRC]=10b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 45 | — | |

*Table continues on the next page...*

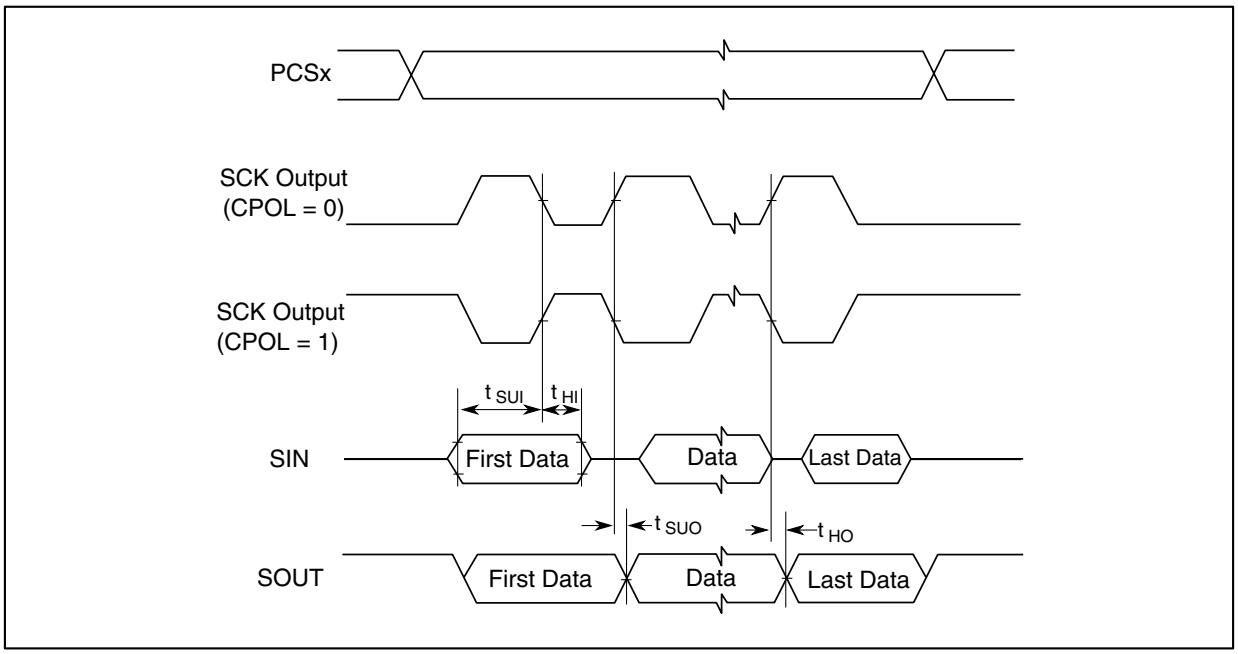



**Figure 33. DSPI CMOS master mode – classic timing, CPHA = 1**

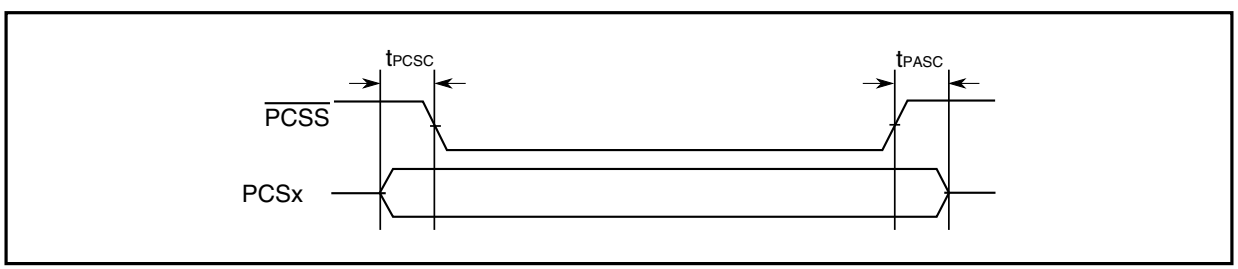



**Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)**

### 3.13.9.1.2 DSPI CMOS Master Mode – Modified Timing

**Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]**

| # | Symbol | Characteristic | Condition[2] | | Value[3] | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Pad drive[4] | Load ($C_L$) | Min | Max | |
| 1 | $t_{SCK}$ | SCK cycle time | PCR[SRC]=11b | 25 pF | 33.0 | — | ns |
| | | | PCR[SRC]=10b | 50 pF | 80.0 | — | |
| | | | PCR[SRC]=01b | 50 pF | 200.0 | — | |
| 2 | $t_{CSC}$ | PCS to SCK delay | PCR[SRC]=11b | 25 pF | ($N^5 \times t_{SYS}$, [6]) – 16 | — | ns |
| | | | PCR[SRC]=10b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 16 | — | |
| | | | PCR[SRC]=01b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 18 | — | |
| | | | PCS: PCR[SRC]=01b<br>SCK: PCR[SRC]=10b | 50 pF | ($N^5 \times t_{SYS}$, [6]) – 45 | — | |

*Table continues on the next page...*

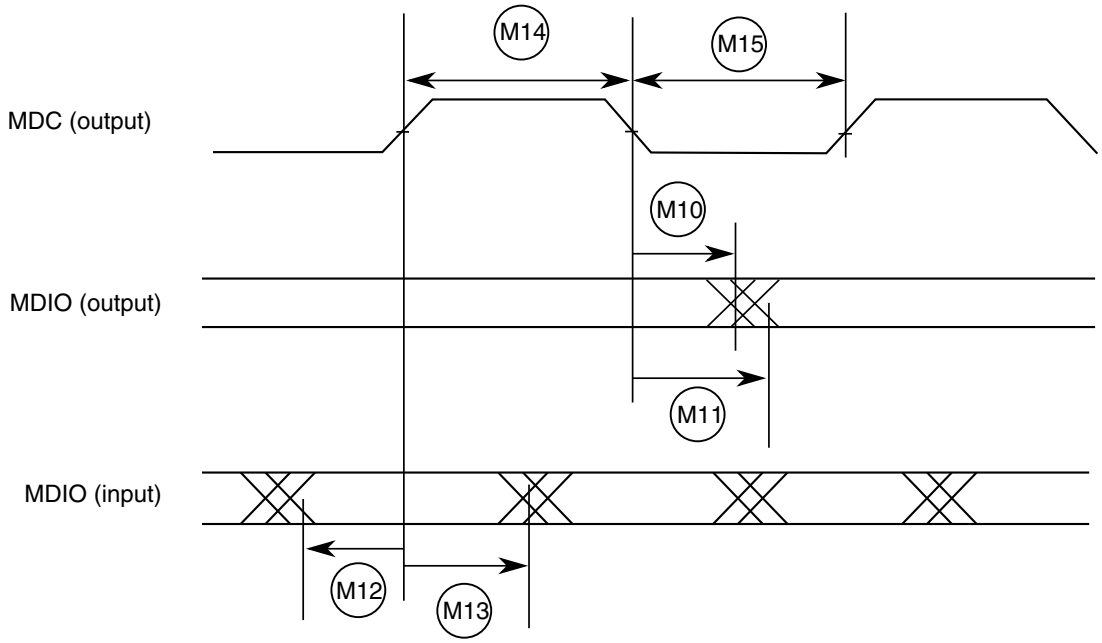



**Figure 44. MII serial management channel timing diagram**

### 3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

**Table 52. RMII receive signal timing[1]**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| R1 | RXD[1:0], CRS_DV to REF_CLK setup | 4 | — | ns |
| R2 | REF_CLK to RXD[1:0], CRS_DV hold | 2 | — | ns |
| R3 | REF_CLK pulse width high | 35% | 65% | REF_CLK period |
| R4 | REF_CLK pulse width low | 35% | 65% | REF_CLK period |

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.

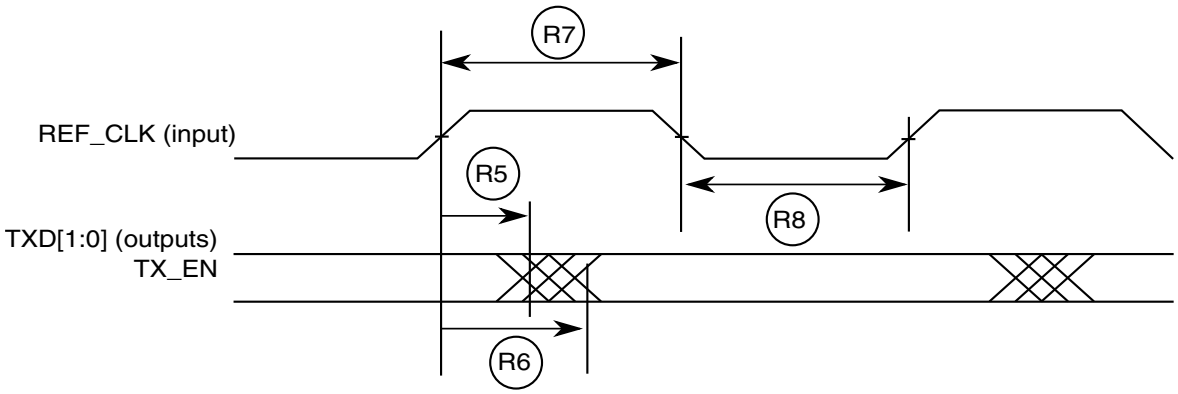



**Figure 46. RMII transmit signal timing diagram**

# 4 Package information

To find the package drawing for each package, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 416-ball MAPBGA | 98ASA00562D |
| 516-ball MAPBGA | 98ASA00623D |

## 4.1 Thermal characteristics

**Table 54. Thermal characteristics, 416-ball MAPBGA package**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Junction to Ambient [1, 2] Natural Convection (Single layer board) | $R_{\Theta JA}$ | 28.8 | °C/W |
| Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p) | $R_{\Theta JA}$ | 19.6 | °C/W |
| Junction to Ambient (@200 ft./min., Single layer board) | $R_{\Theta JMA}$ | 21.3 | °C/W |
| Junction to Ambient (@200 ft./min., Four layer board 2s2p) | $R_{\Theta JMA}$ | 15.1 | °C/W |
| Junction to Board [4] | $R_{\Theta JB}$ | 9.5 | °C/W |
| Junction to Case [5] | $R_{\Theta JC}$ | 4.8 | °C/W |
| Junction to Package Top [6] Natural Convection | $\Psi_{JT}$ | 0.2 | °C/W |

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter ($\Psi_{JPB}$) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} x P_D)$$

where:

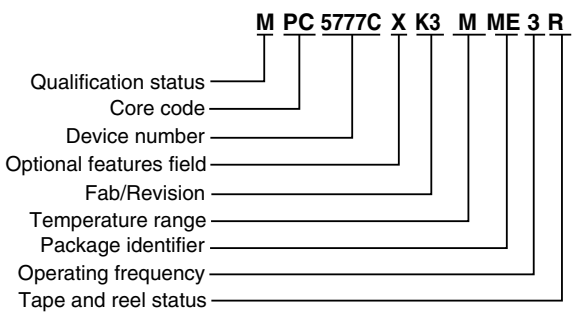
$T_T$ = thermocouple temperature on bottom of the package (°C)

$\Psi_{JT}$ = thermal characterization parameter (°C/W)

$P_D$ = power dissipation in the package (W)

# 5 Ordering information

Figure 47 and Table 56 describe orderable part numbers for the MPC5777C.




**Temperature range**
M = –40 °C to 125 °C

**Operating frequency**
3 = 2 x 264 MHz

**Package identifier**
ME = 416 MAPBGA Pb-Free
MO = 516 MAPBGA Pb-Free

**Tape and reel status**
R = Tape and reel
(blank) = Trays

**Qualification status**
P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

**Optional features field**
(blank) = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
A = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
R = ISO-compliant CAN FD not available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
C = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
D = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
L = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
S = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes RSA-enhanced security firmware
T = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes RSA-enhanced security firmware

**Note:** Not all options are available on all devices.

**Figure 47. MPC5777C Orderable part number description**

**Table 56. Example orderable part numbers**

| Part number[1] | Package description | Speed (MHz)[2] | Operating temperature[3] | |
|---|---|---|---|---|
| | | | Min ($T_L$) | Max ($T_H$) |
| SPC5777CCK3MME3 | MPC5777C 416 package<br>Lead-free (Pb-free) | 264 | –40 °C | 125 °C |
| SPC5777CK3MME3 | MPC5777C 416 package<br>Lead-free (Pb-free) | 264 | –40 °C | 125 °C |
| SPC5777CCK3MMO3 | MPC5777C 516 package<br>Lead-free (Pb-free) | 264 | –40 °C | 125 °C |
| SPC5777CK3MMO3 | MPC5777C 516 package<br>Lead-free (Pb-free) | 264 | –40 °C | 125 °C |

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by $T_L$; the highest ambient operating temperature is referenced by $T_H$.

# 6 Document revision history

The following table summarizes revisions to this document since the previous release.

**Table 57. Revision history**

| Revision | Date | Description of changes |
|---|---|---|
| 11 | 04/2017 | In Figure 47 of Ordering information, added codes and firmware version information in definition of "Optional features field"<br>• At end of line for *(blank)*, added "version 2.07"<br>• Added line for *A*<br>• At end of line for *R*, added "version 2.08"<br>• At end of line for *C*, added "version 2.07"<br>• Added line for *D*<br>• At end of line for *L*, added "version 2.08" |