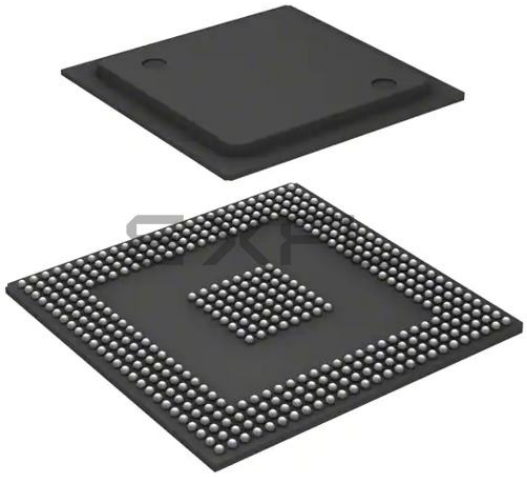

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck3mme3r

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads
EBI pads	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

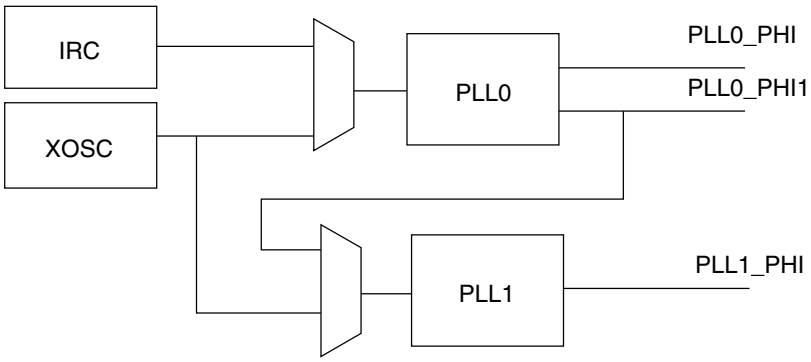

Figure 6. PLL integration

3.7.1 PLL electrical specifications

Table 12. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1, 2]	—	8	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	PLL0 output frequency	—	4.762	—	200	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 200 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[3]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	7.5	mA

1. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz to 20 MHz.
2. PLL0IN clock retrieved directly from either internal IRC or external XOSC clock. Input characteristics are granted when using internal IRC or external oscillator is used in functional mode.
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

Table 13. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL1PHISPJ}\rvert$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[2]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 14 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 14. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	—	V_{REF} – 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.1	2.8	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.2	2.9	
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	

Table continues on the next page...

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	80	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	77	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	74	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	71	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	71	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	70	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	68	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	65	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	62	—	—	

Table continues on the next page...

Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the SDADC module.

16. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.9 Temperature Sensor

The following table describes the Temperature Sensor electrical characteristics.

Table 19. Temperature Sensor electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy	–40°C < T_J < 150°C	–5	—	5	°C
I_{TEMP_SENS}	V_{DDA_EQA} power supply current, per Temp Sensor	—	—	—	700	µA

3.10 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to the SIPI interface on the chip. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

Table 29. Voltage monitor electrical characteristics[1, 2] (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR_HV	HV V_{DDPMC} supply power on reset threshold	Rising voltage (powerup)	N/A	No	Enab.	2444	2600	2756	mV
		Falling voltage (power down)				2424	2580	2736	
LVD_HV	HV internal V_{DDPMC} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2946	3010	3066	
		Falling voltage (trimmed)				2934	2998	3044	
HVD_HV	HV internal V_{DDPMC} supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	5696	5860	5968	mV
		Falling voltage				5666	5830	5938	
LVD_FLASH	FLASH supply low voltage monitoring[6]	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2956	3010	3053	
		Falling voltage (trimmed)				2944	2998	3041	
HVD_FLASH	FLASH supply high voltage monitoring[6]	Rising voltage	4bit	Yes	Disab.	3456	3530	3584	mV
		Falling voltage				3426	3500	3554	
LVD_IO	Main I/O V_{DDEH1} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	3250	3350	3488	mV
		Falling voltage (untrimmed)				3220	3320	3458	
		Rising voltage (trimmed)				3347	3420	3468	
		Falling voltage (trimmed)				3317	3390	3438	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	µs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	µs

1. LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed; LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.
2. HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed; HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.
3. POR098_c threshold is an untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
6. V_{DDFLA} range is guaranteed when internal flash memory regulator is used.

3.11.4 Power sequencing requirements

Requirements for power sequencing include the following.

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

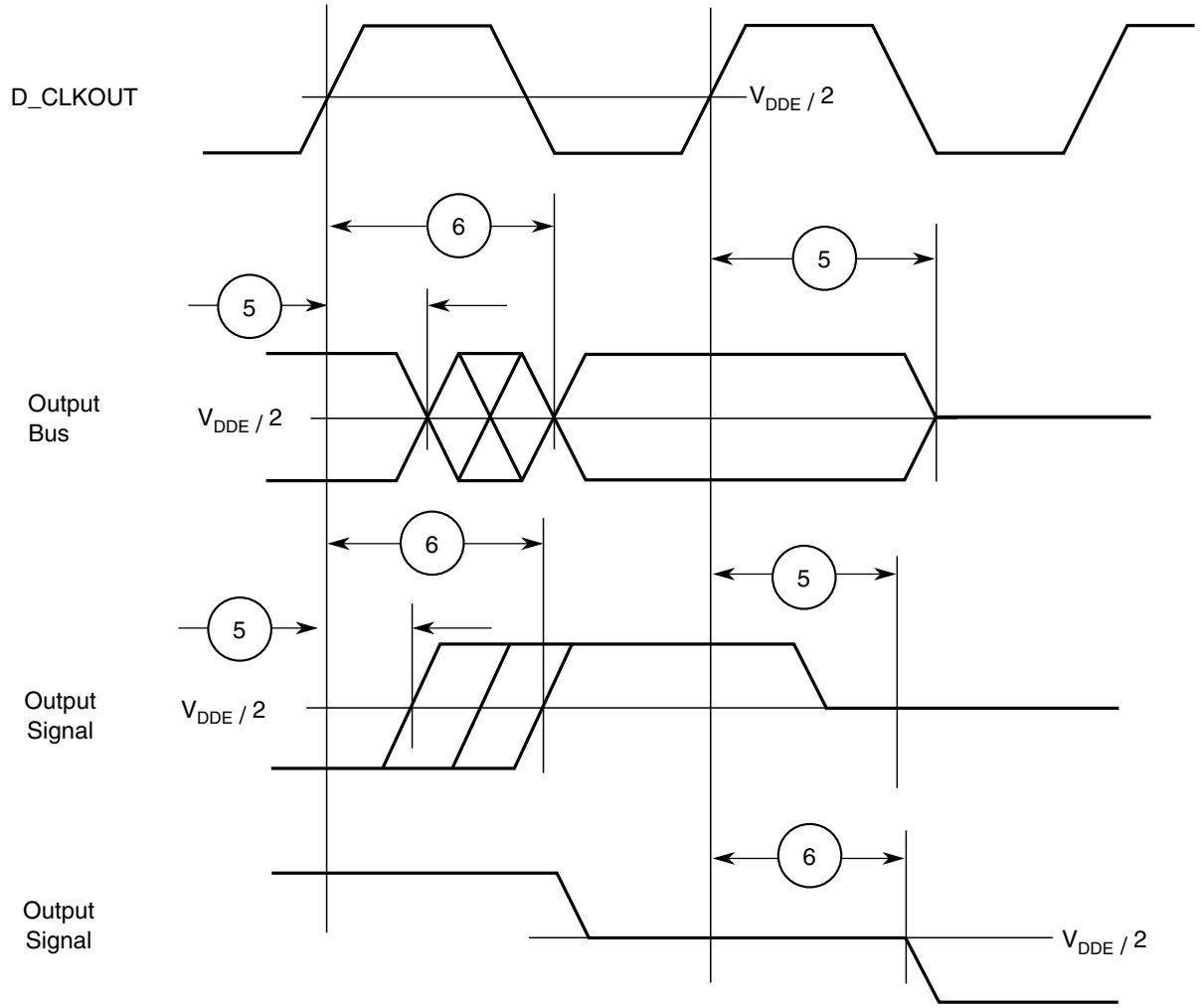

Figure 26. Synchronous output timing

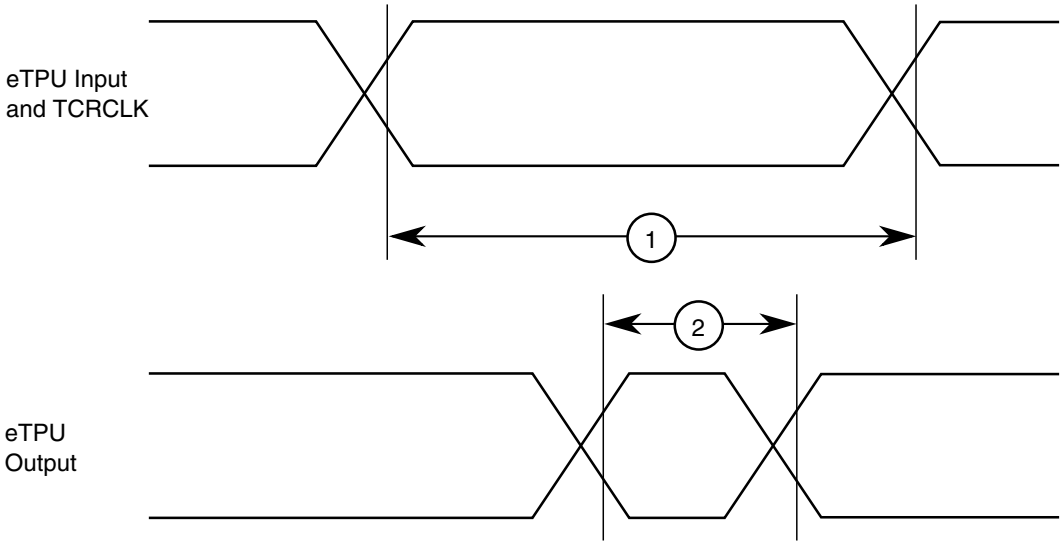

Figure 30. eTPU timing

3.13.8 eMIOS timing

Table 41. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

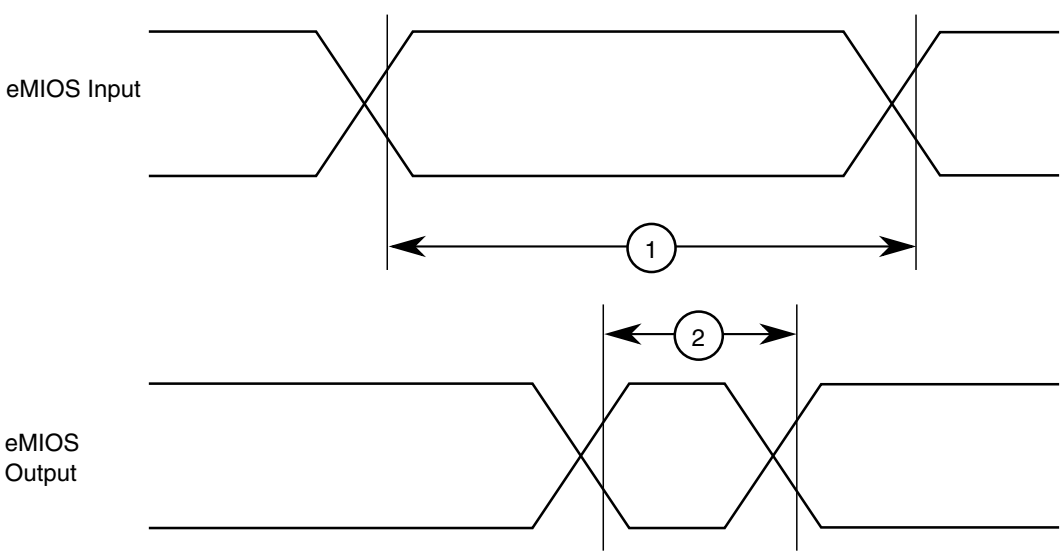

Figure 31. eMIOS timing

SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
8. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
9. PCSx and $\overline{\text{PCSS}}$ using same pad configuration.
10. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

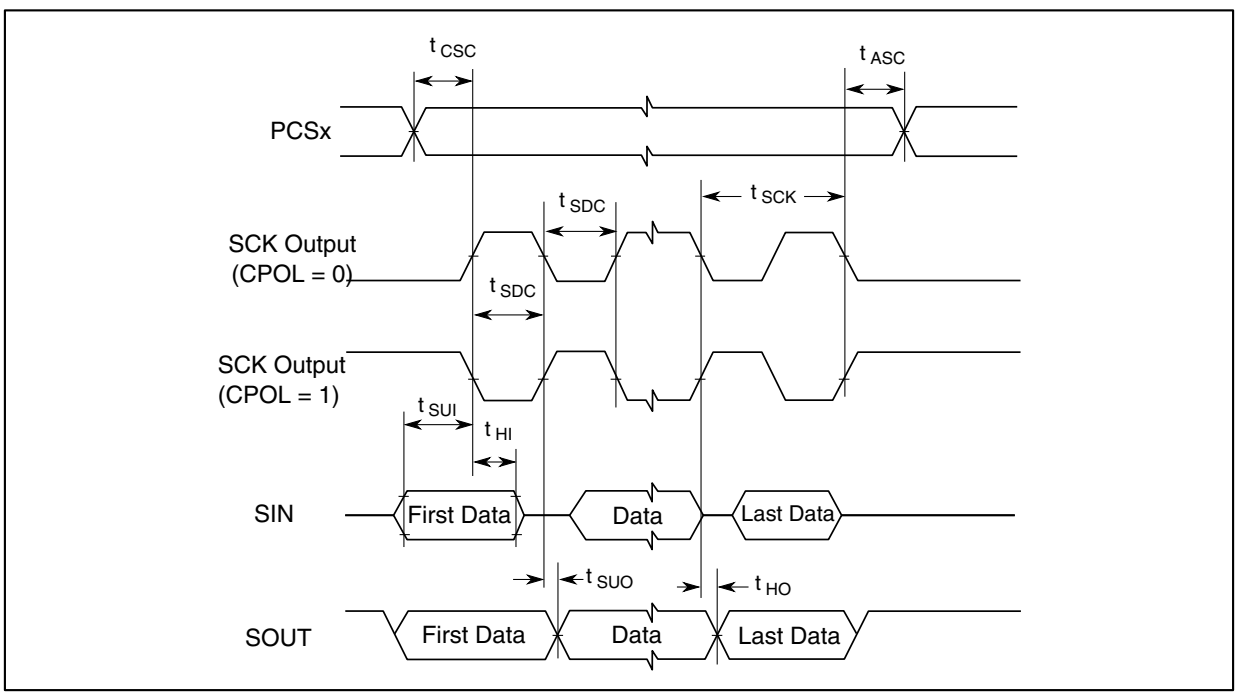

Figure 32. DSPI CMOS master mode – classic timing, CPHA = 0

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} – 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

Table continues on the next page...

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2] (continued)

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
3	t_{CSH}	PCS hold after SCK[6]	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	–33	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–35	—	ns
4	t_{SDC}	SCK duty cycle[7]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	ns
			PCR[SRC]=01b	50 pF	—	18.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	ns
			PCR[SRC]=01b	50 pF	–21.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

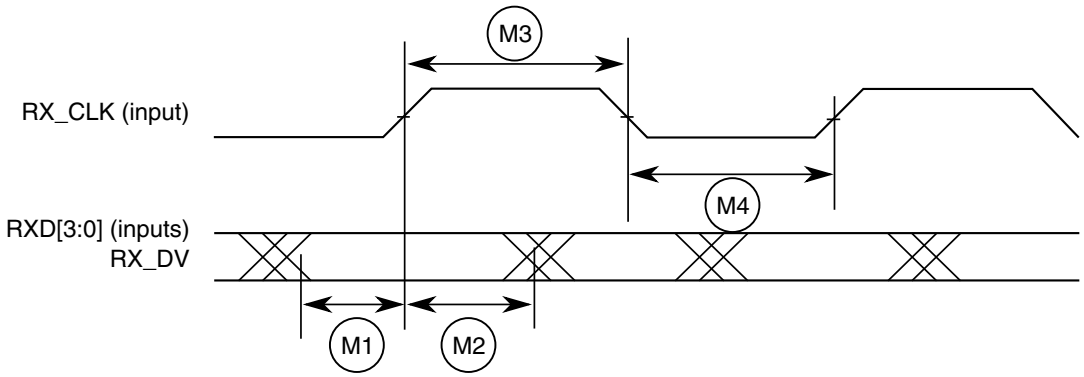

Figure 41. MII receive signal timing diagram

3.13.10.2 MII transmit signal timing (TXD[3:0], TX_EN, and TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of noncompliant MII PHYs.

Refer to the *MPC5777C Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 49. MII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN invalid	4.5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

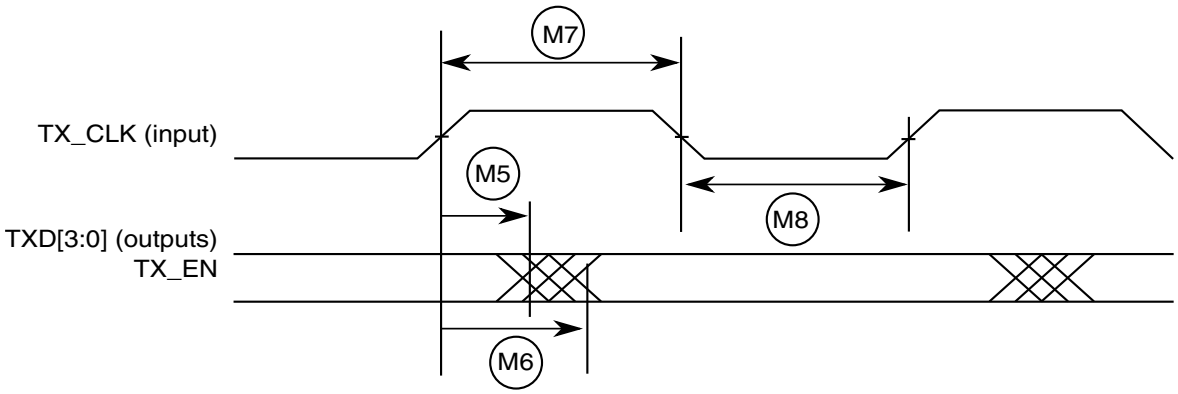

Figure 42. MII transmit signal timing diagram

3.13.10.3 MII async inputs signal timing (CRS)

Table 50. MII async inputs signal timing

Symbol	Characteristic	Value		Unit
		Min	Max	
M9	CRS minimum pulse width	1.5	—	TX_CLK period

Figure 43. MII async inputs timing diagram

3.13.10.4 MII and RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 51. MII serial management channel timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

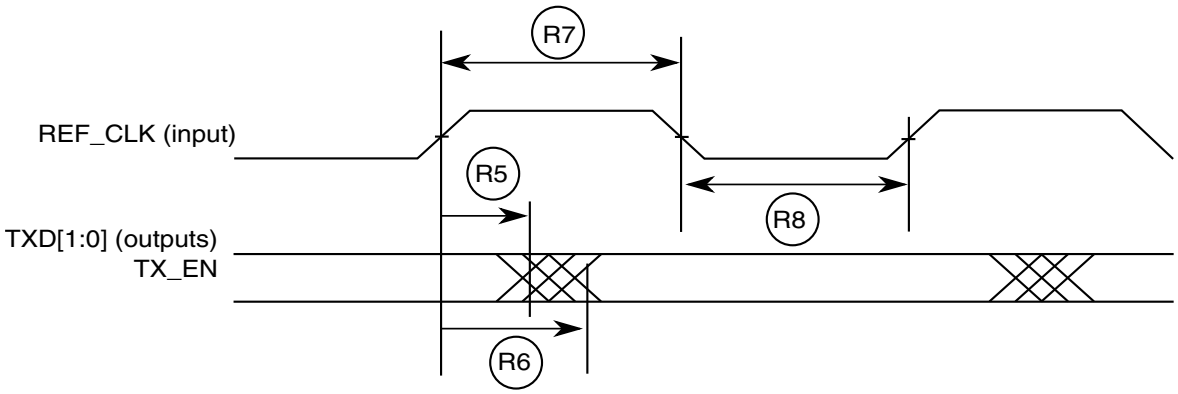

Figure 46. RMII transmit signal timing diagram

4 Package information

To find the package drawing for each package, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
416-ball MAPBGA	98ASA00562D
516-ball MAPBGA	98ASA00623D

4.1 Thermal characteristics

Table 54. Thermal characteristics, 416-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.8	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	19.6	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.1	°C/W
Junction to Board [4]	$R_{\Theta JB}$	9.5	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance: