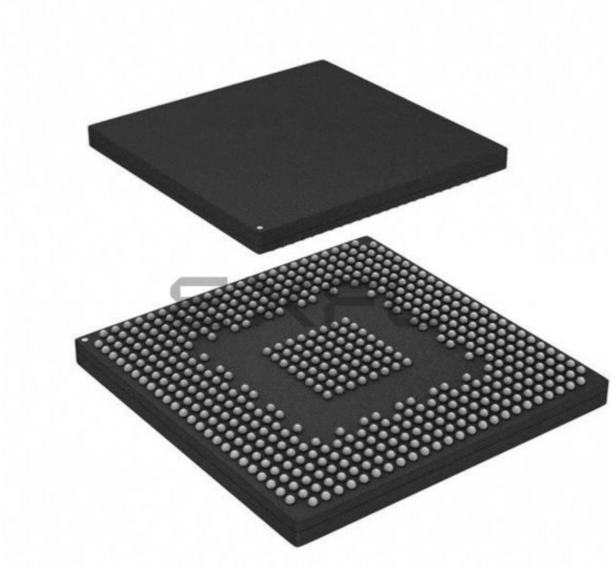

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777clk3mmo3

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB7_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.

3.4 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted.

If the device operating conditions are exceeded, the functionality of the device is not guaranteed.

Table 3. Device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
f_{SYS}	Device operating frequency[1]	—	—	—	264[2]	MHz
f_{PLATF}	Platform operating frequency	—	—	—	132	MHz
f_{ETPU}	eTPU operating frequency	—	—	—	200	MHz
f_{EBI}	EBI operating frequency	—	—	—	66	MHz
f_{PER}	Peripheral block operating frequency	—	—	—	132	MHz
f_{FM_PER}	Frequency-modulated peripheral block operating frequency	—	—	—	132	MHz
t_{CYC}	Platform clock period	—	—	—	$1/f_{PLATF}$	ns
t_{CYC_ETPU}	eTPU clock period	—	—	—	$1/f_{ETPU}$	ns
t_{CYC_PER}	Peripheral clock period	—	—	—	$1/f_{PER}$	ns
Temperature						
T_J	Junction operating temperature range	Packaged devices	–40.0	—	150.0	°C
T_A (T_L to T_H)	Ambient operating temperature range	Packaged devices	–40.0	—	125.0[3]	°C
Voltage						
V_{DD}	External core supply voltage[4, 5]	LVD/HVD enabled	1.2	—	1.32	V
		LVD/HVD disabled[6, 7, 8, 9]	1.2	—	1.38	
V_{DDA_MISC}	TRNG and IRC supply voltage	—	3.5	—	5.5	V
V_{DDEx}	I/O supply voltage (fast I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEHx}[9]	I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEH1}	eTPU_A, eSCI_A, eSCI_B, and configuration I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
V_{DDPMC}[10]	Power Management Controller (PMC) supply voltage	Full functionality	3.15	—	5.5	V
V_{DDPWR}	SMPS driver supply voltage	Reference to V_{SSPWR}	3.0	—	5.5	V
V_{DDFLA}	Flash core voltage	—	3.15	—	3.6	V
V_{STBY}	RAM standby supply voltage	—	0.95[11]	—	5.5	V

Table continues on the next page...

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
GAIN	ADC gain	Defined through SDADC_MCR[PGAN]. Only integer powers of 2 are valid gain values.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$	Absolute value of the ADC gain error[6, 7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	Conversion offset[6, 7]	Before calibration (applies to all gain settings: 1, 2, 4, 8, 16)	—	10*(1+1/gain)	20	mV
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	80	—	—	dB
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	77	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	74	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	71	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	71	—	—	dB
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	70	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	68	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	65	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	62	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

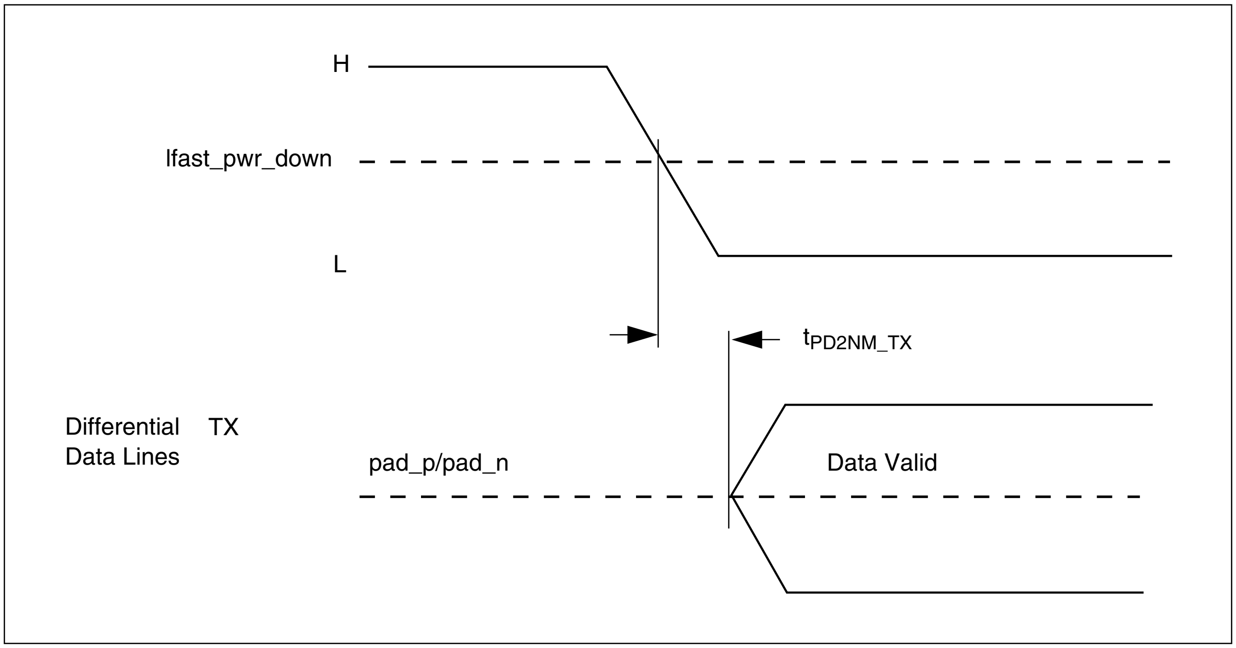

Figure 9. Power-down exit time

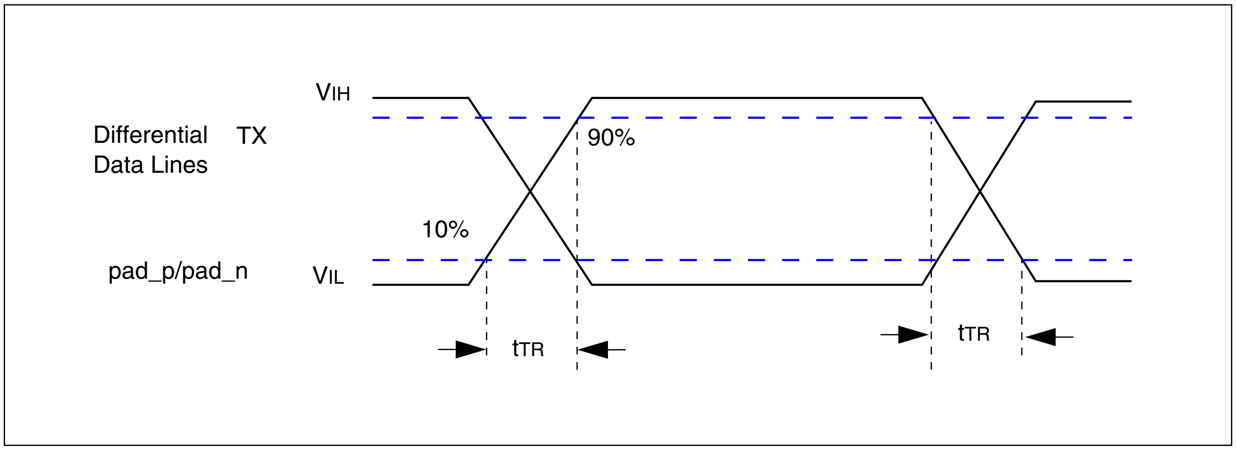

Figure 10. Rise/fall time

3.10.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 20. LVDS pad startup and receiver electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
STARTUP[2,3]						
t_{STRT_BIAS}	Bias current reference startup time[4]	—	—	0.5	4	μs

Table continues on the next page...

Table 26. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	p-MOS	3 A - 20 V	SQ2301ES / FDC642P or equivalent: low threshold p-MOS, Vth < 2.0 V, Rdson @ 4.5 V < 100 mΩ, Cg < 5 nF
D1	Schottky	2 A - 20 V	SS8P3L or equivalent: Vishay™ low Vf Schottky diode
L	Inductor	3−4 µH - 1.5 A	Buck shielded coil low ESR
CI	Capacitor	22 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.1 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF capacitor in parallel)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to the p-MOS source)
R	Resistor	2.0-4.7 kΩ	Pullup for power p-MOS gate
CB	Capacitor	22 µF - 20 V	Ceramic, connect 100 nF capacitor in parallel (as close as possible to package to reduce current loop from V_{DDPWR} to V_{SSPWR})

The following diagram shows the SMPS configuration connection.

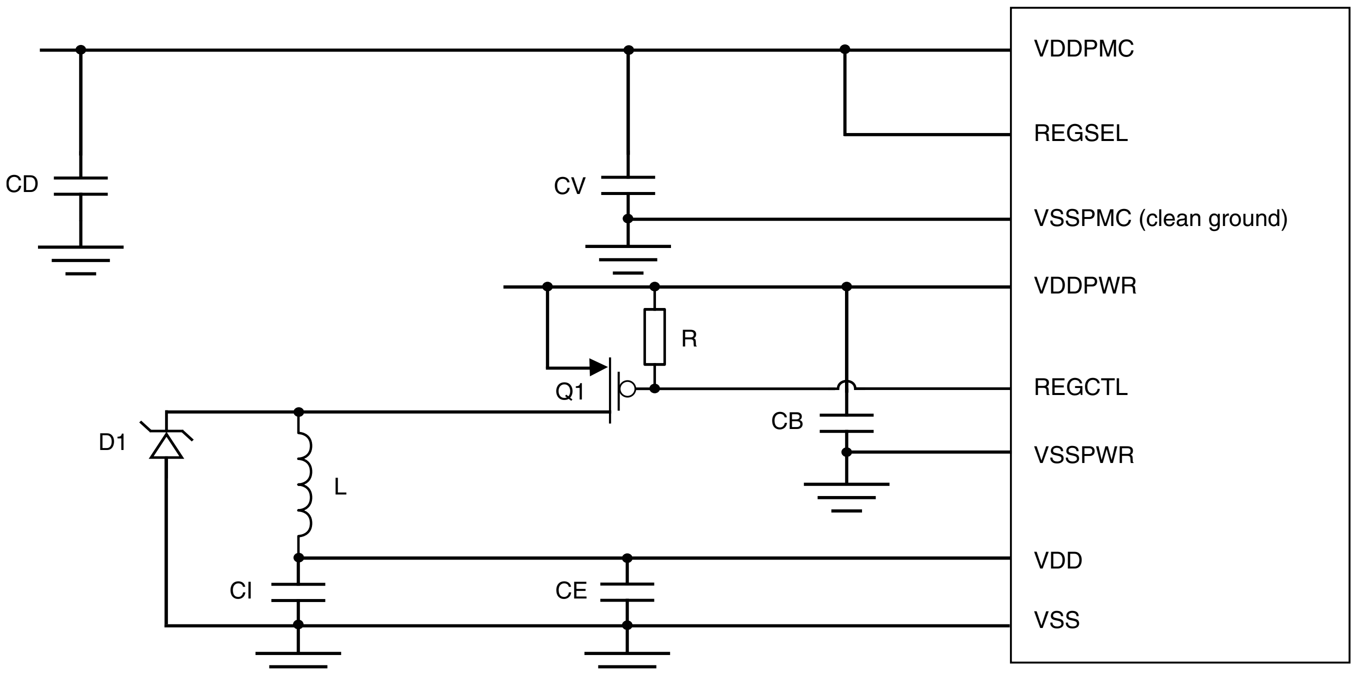

Figure 13. SMPS configuration

NOTE

The REGSEL pin is tied to V_{DDPMC} to select SMPS. If REGSEL is 0, the chip boots with the linear regulator.

See Power sequencing requirements for details about V_{DDPMC} and V_{DDPWR}.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

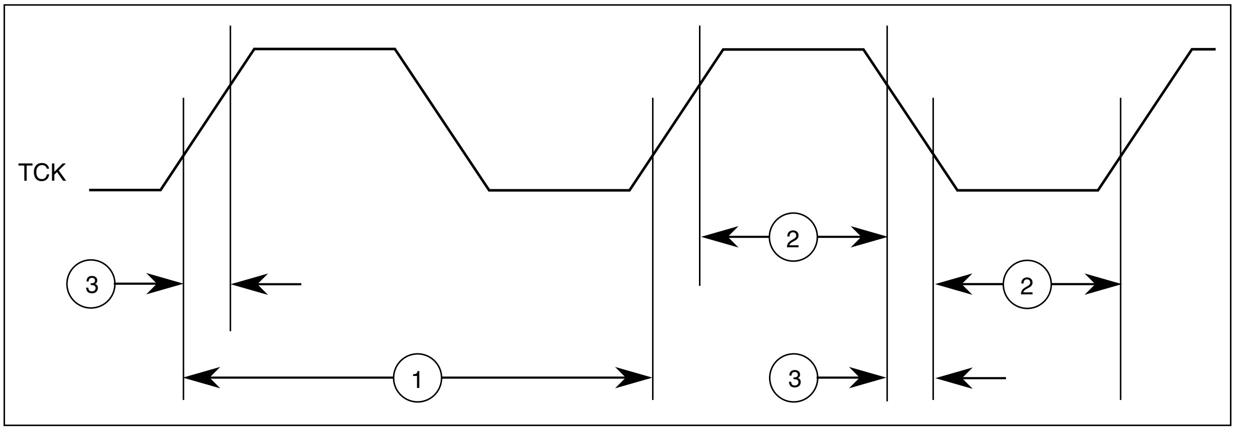

Figure 19. JTAG test clock input timing

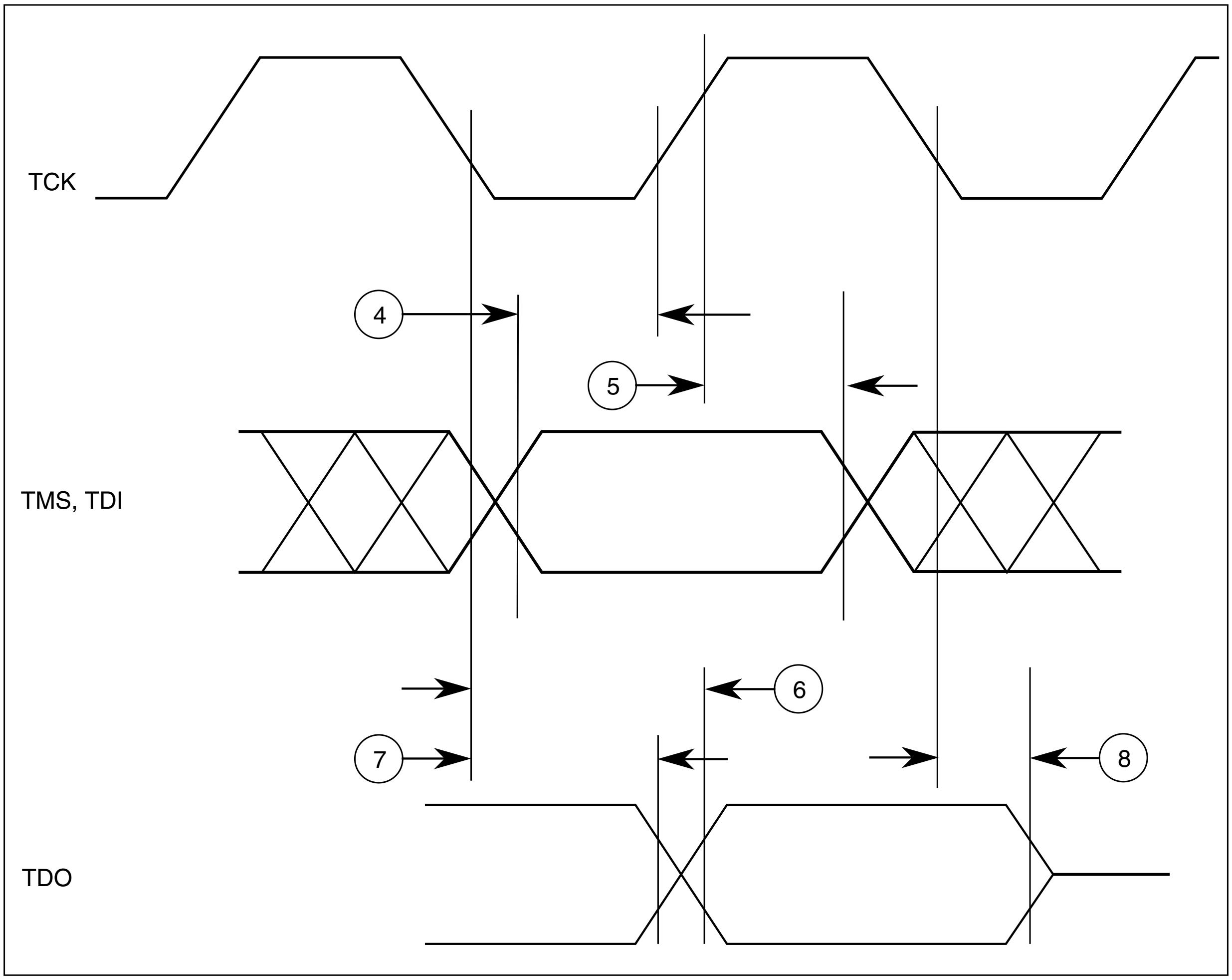

Figure 20. JTAG test access port timing

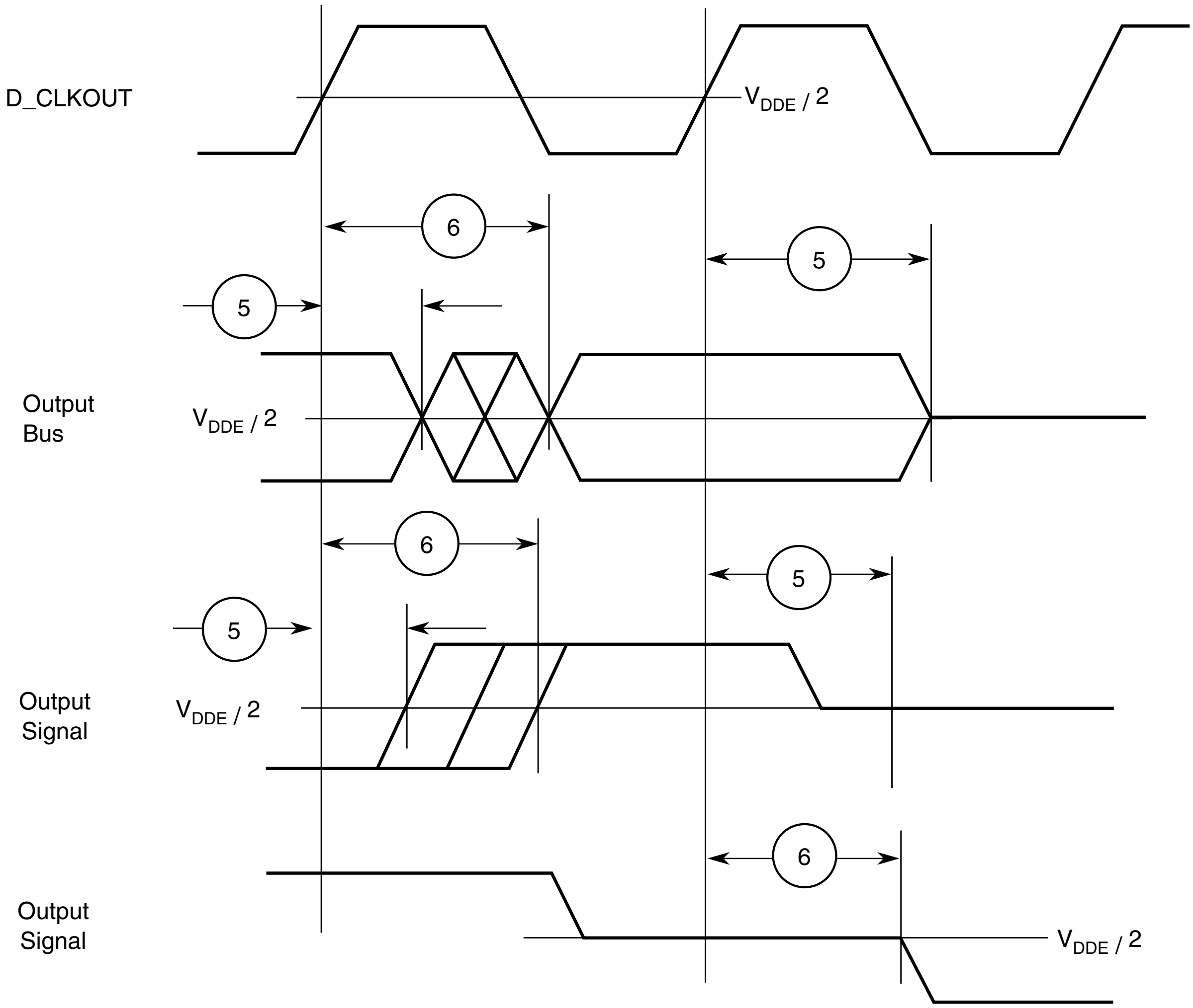

Figure 26. Synchronous output timing

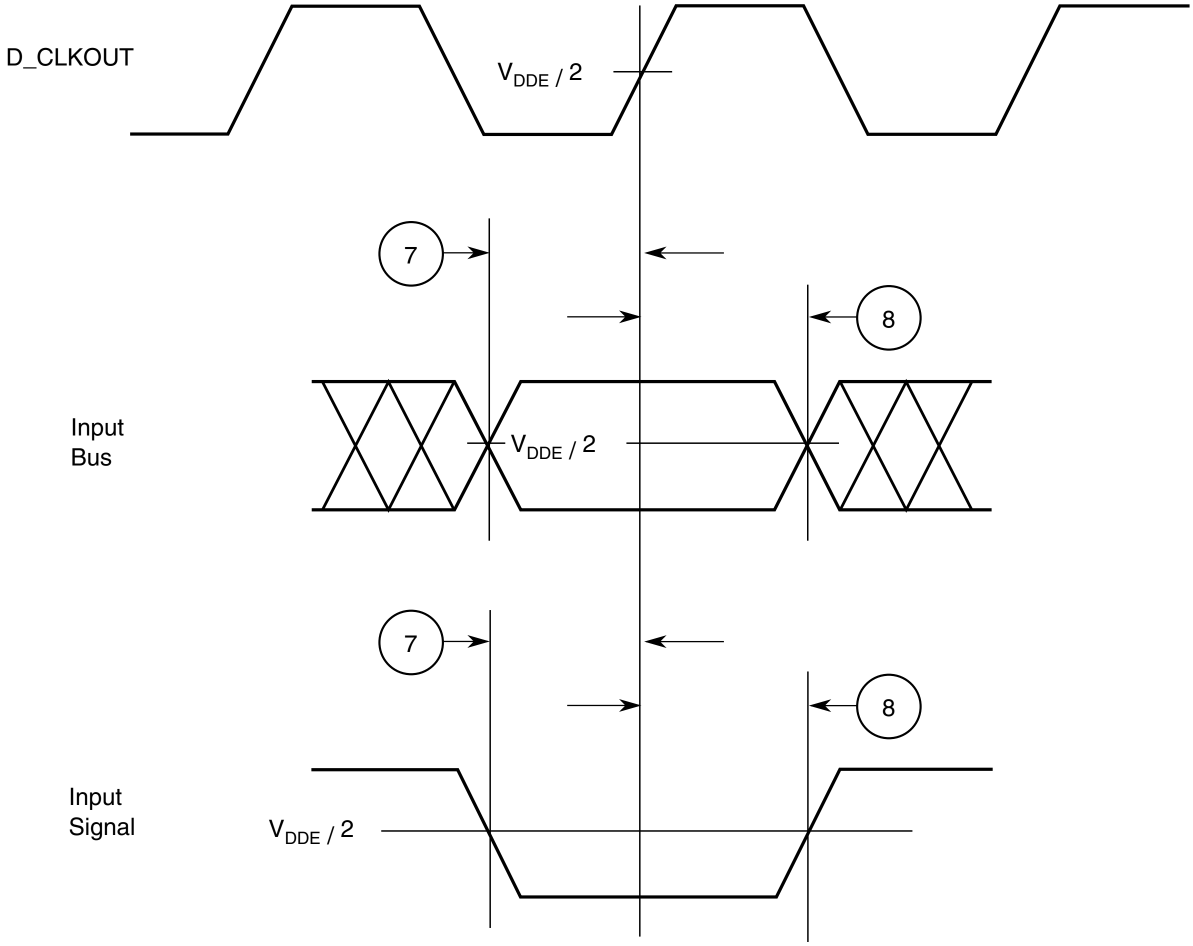

Figure 27. Synchronous input timing

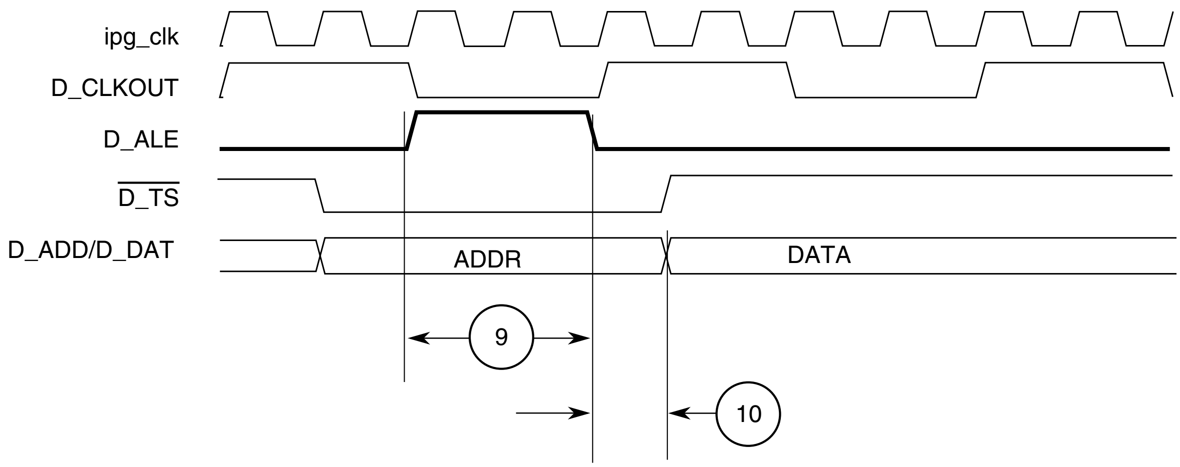

Figure 28. ALE signal timing

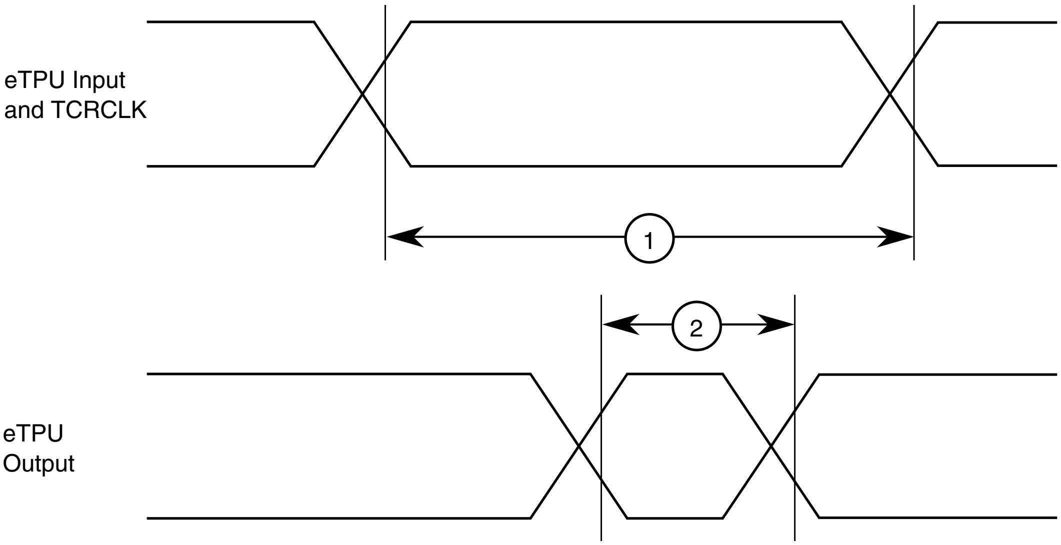

Figure 30. eTPU timing

3.13.8 eMIOS timing

Table 41. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

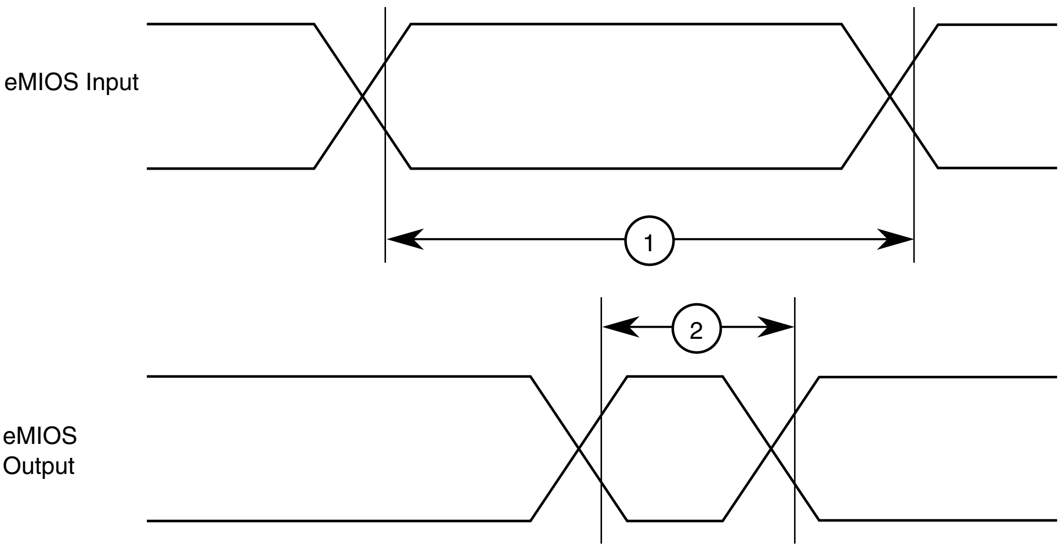

Figure 31. eMIOS timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS}, [6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS}, [6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS}, [6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS}, [6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
10	t_{HO}	SOUT data hold time after SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	$-9.0 + t_{SYS}$[6]	—	ns
			PCR[SRC]=10b	50 pF	$-10.0 + t_{SYS}$[6]	—	
			PCR[SRC]=01b	50 pF	$-21.0 + t_{SYS}$[6]	—	
		SOUT data hold time after SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
8. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
9. PCSx and $\overline{\text{PCSS}}$ using same pad configuration.
10. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
11. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
12. The 0 pF load condition given in the DSPI AC timing applies to theoretical worst-case hold timing. This guarantees worst-case operation, and additional margin can be achieved in the applications by applying a realistic load.
13. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	**SOUT data valid time (after SCK edge)**					
		SOUT data valid time from SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}[5]	ns
		SOUT data valid time from SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	**SOUT data hold time (after SCK edge)**					
		SOUT data hold time after SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	–7.5 + t_{SYS}[5]	—	ns
		SOUT data hold time after SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min tSYS = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

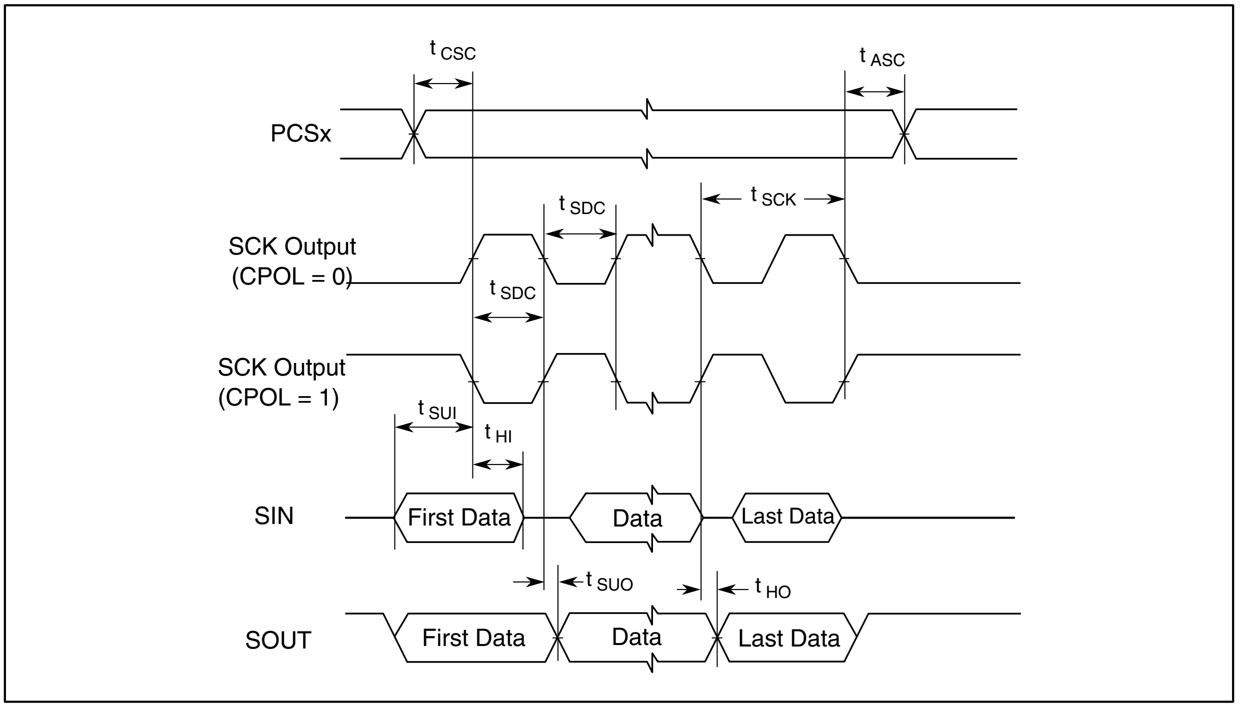

Figure 38. DSPI LVDS master mode – modified timing, CPHA = 0

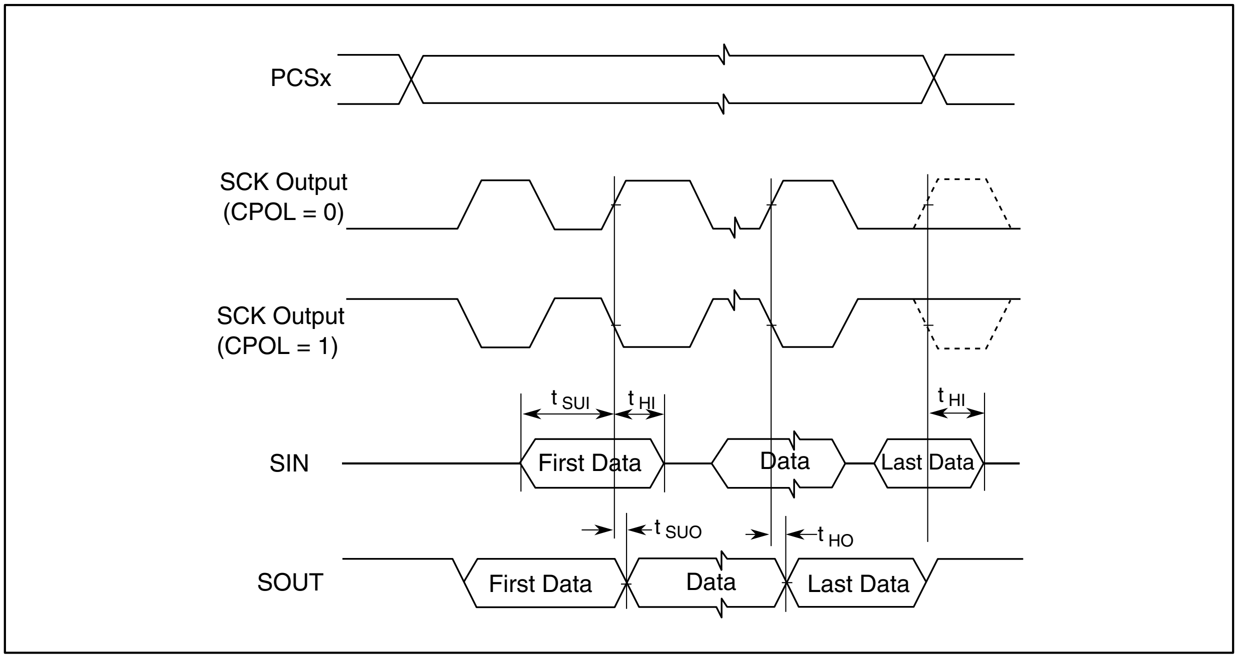

Figure 39. DSPI LVDS master mode – modified timing, CPHA = 1

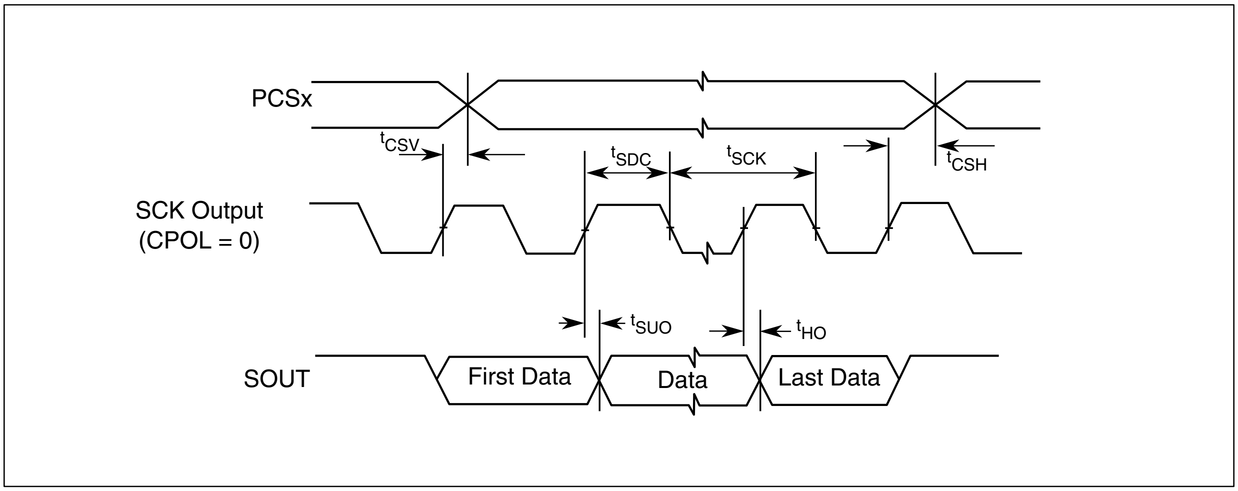

Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

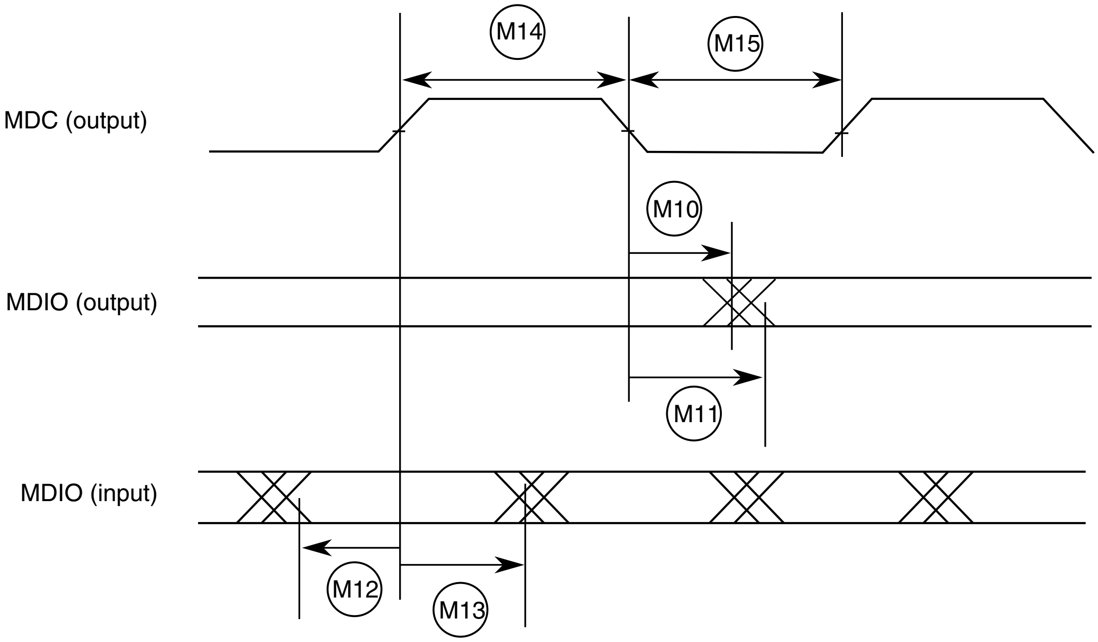

Figure 44. MII serial management channel timing diagram

3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 52. RMII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.

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