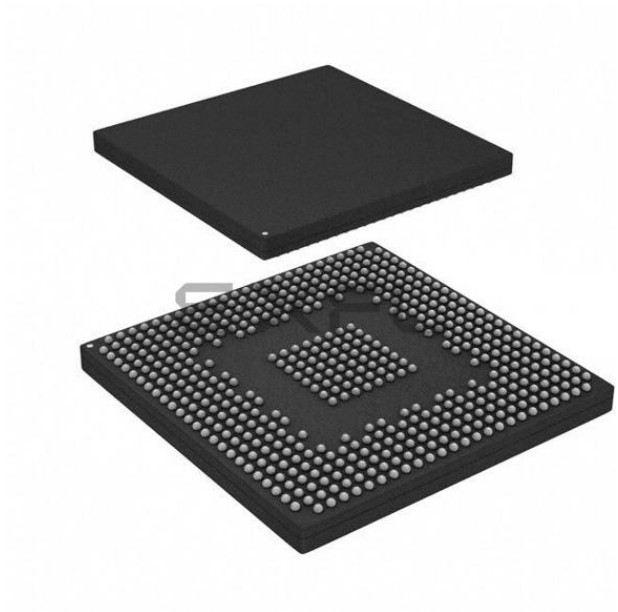

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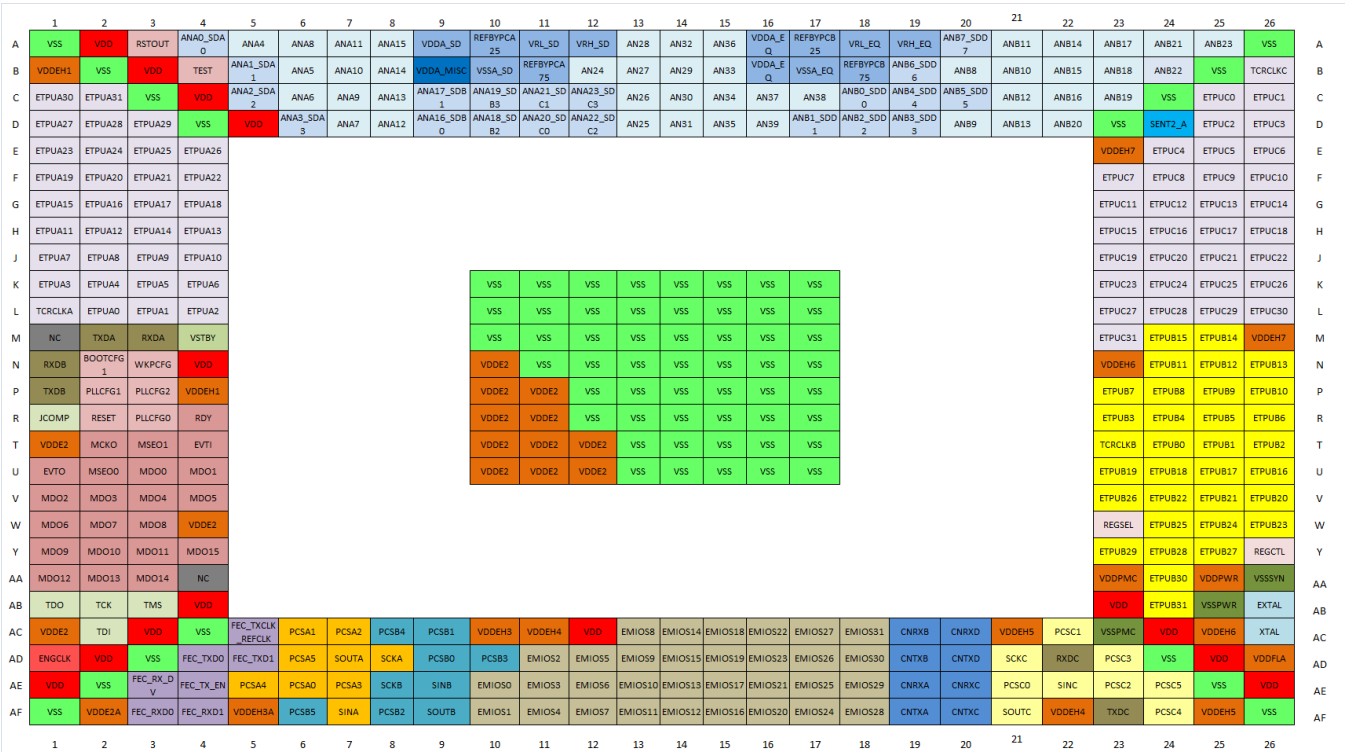
Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777clk3mmo3r



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	AN87_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	AN88	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.

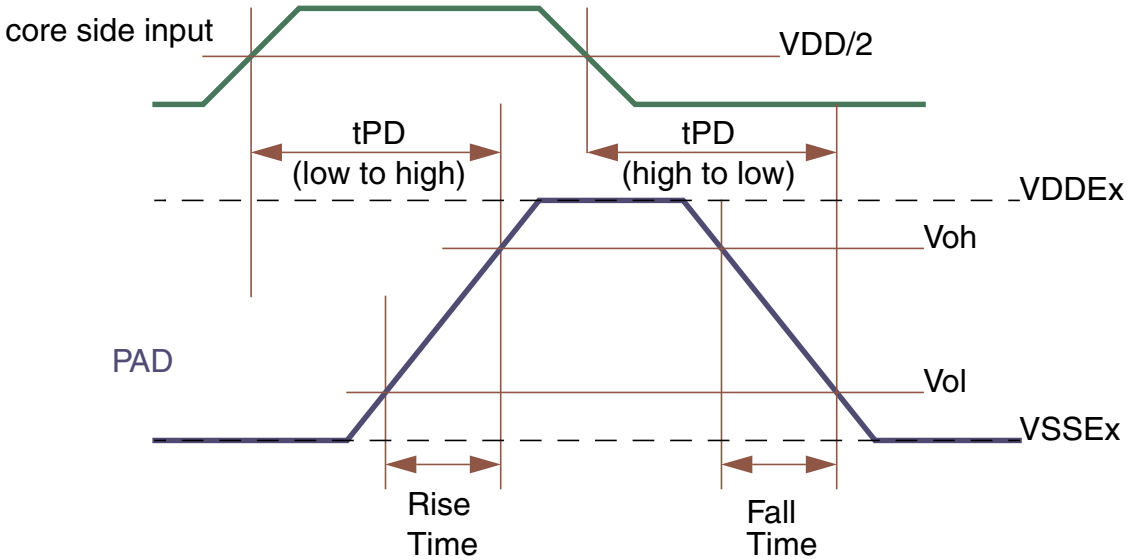


Figure 5. I/O output DC electrical characteristics definition

The following tables specify output DC electrical characteristics.

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1]

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
I_{OH}	GPIO pad output high current	V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	25	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	15	—	—	
		V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	13	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	8	—	—	
I_{OL}	GPIO pad output low current	V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	48	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	22	—	—	
		V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	17	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	10.5	—	—	

Table continues on the next page...

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

Table 13. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL1PHISPJ}\rvert$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[2]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 14 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 14. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	—	V_{REF} – 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.1	2.8	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.2	2.9	
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	

Table continues on the next page...

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF333}$	Signal to noise and distortion ratio in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	59	—	—	
$SINAD_{SE150}$	Signal to noise and distortion ratio in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	54	—	—	

Table continues on the next page...

3.10.1 LFAST interface timing diagrams

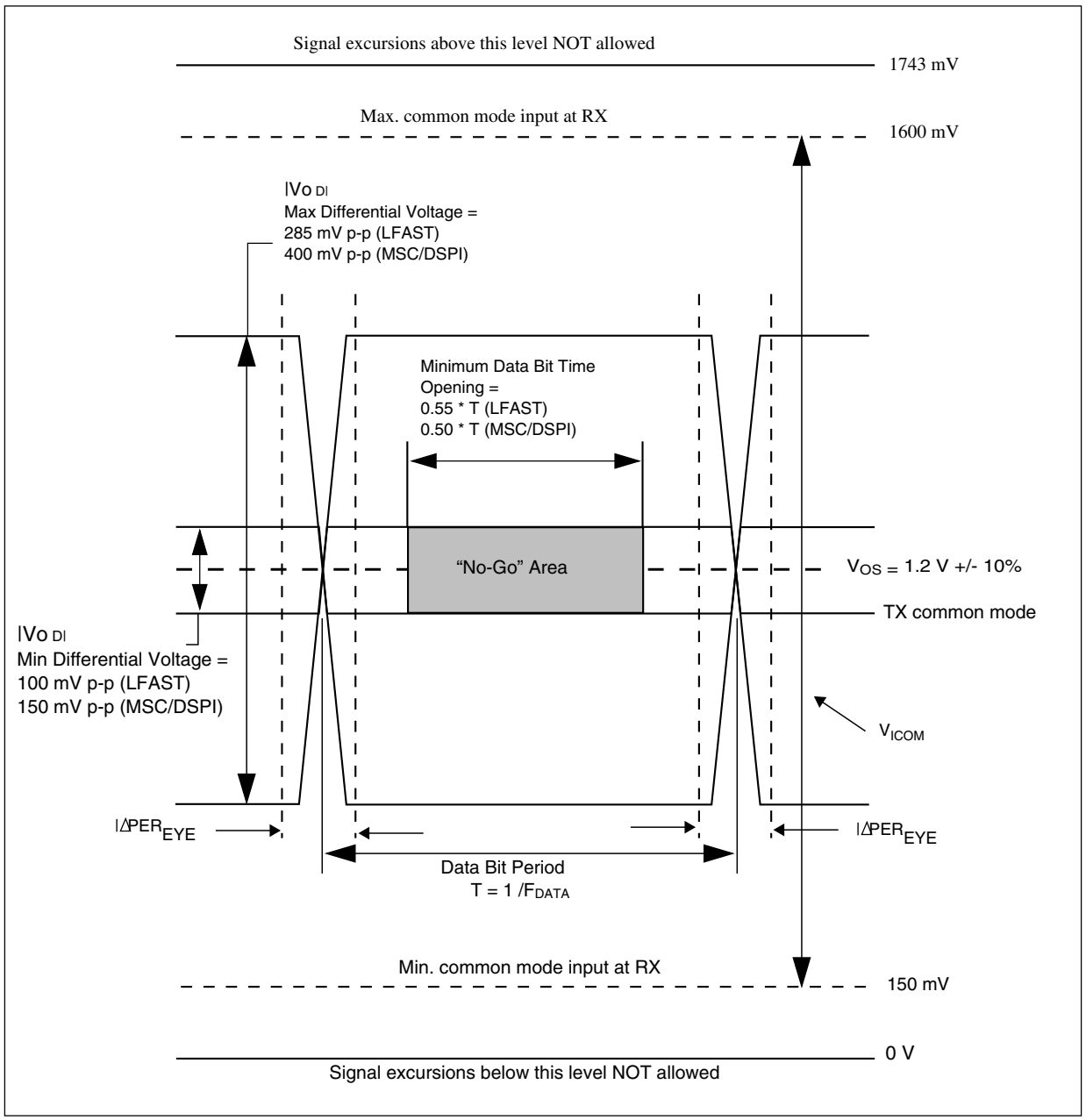


Figure 8. LFAST and MSC/DSPI LVDS timing definition

Table 20. LVDS pad startup and receiver electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to Normal mode)[5]	—	—	0.4	2.75	µs
t_{SM2NM_TX}	Transmitter startup time (Sleep mode to Normal mode)[6]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	Receiver startup time (power down to Normal mode)[7]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to Sleep mode)[8]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[9]	—	1.6[10]	V
$\|\Delta VI\|$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	V_{DDEH} = 3.0 V to 5.5 V	80	125	150	Ω
C_{IN}	Differential input capacitance[11]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules.
3. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
4. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
5. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
6. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
7. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
8. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
9. Absolute min = 0.15 V – (285 mV/2) = 0 V
10. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
11. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in Figure 11.

Table 21. LFAST transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	240	Mbps

Table continues on the next page...

Table 21. LFAST transmitter electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	110	200	285	mV
t_{TR}	Rise/fall time (10% – 90% of swing)[2,3]	—	0.26	—	1.5	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	12.0	pF
		V_{DDE} = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst-case internal capacitance values shown in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load CL.

Table 22. MSC/DSPI LVDS transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing)[2,3]	—	0.8	—	4.0	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	50	pF
		V_{DDE} = 3.0 V	—	—	39	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst-case internal capacitance values given in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load C_L.

3.12.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units [2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.12.3 Flash memory module life specifications

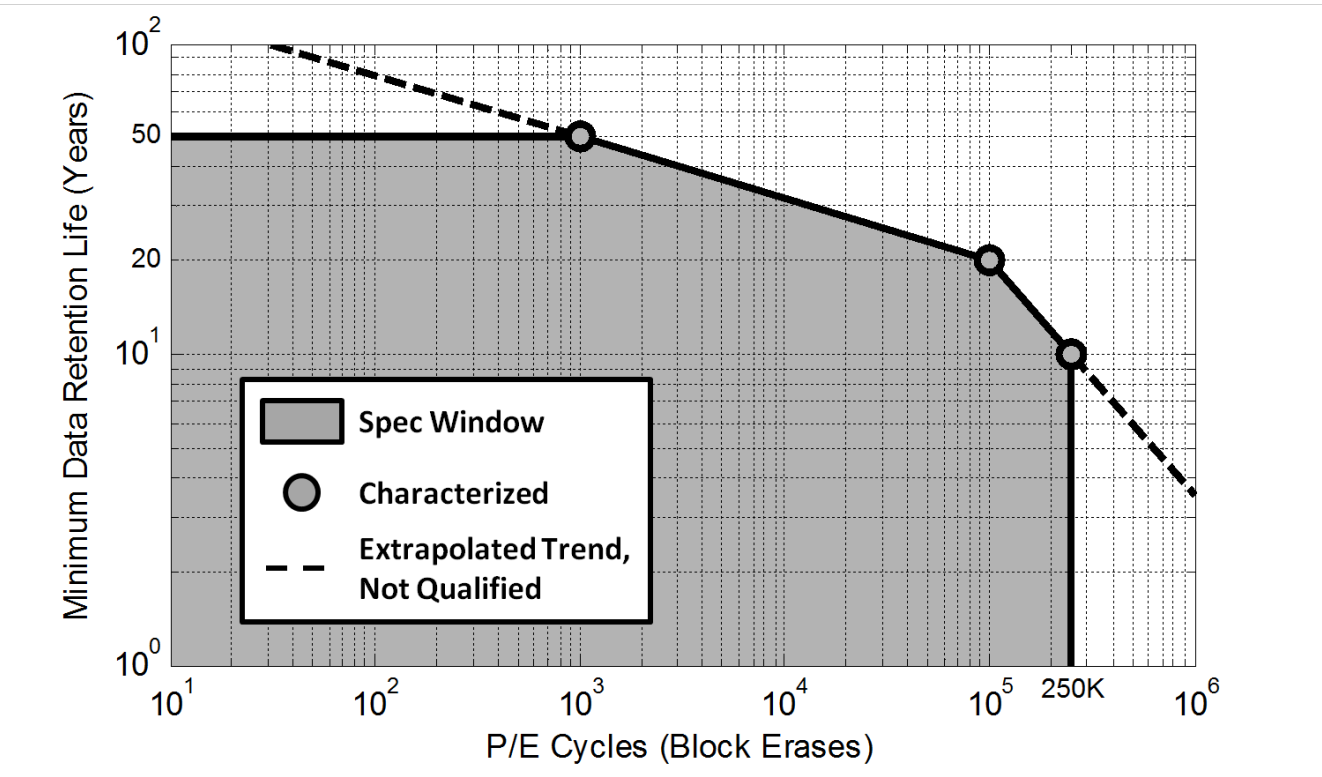
Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

3.12.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.12.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns

Table continues on the next page...

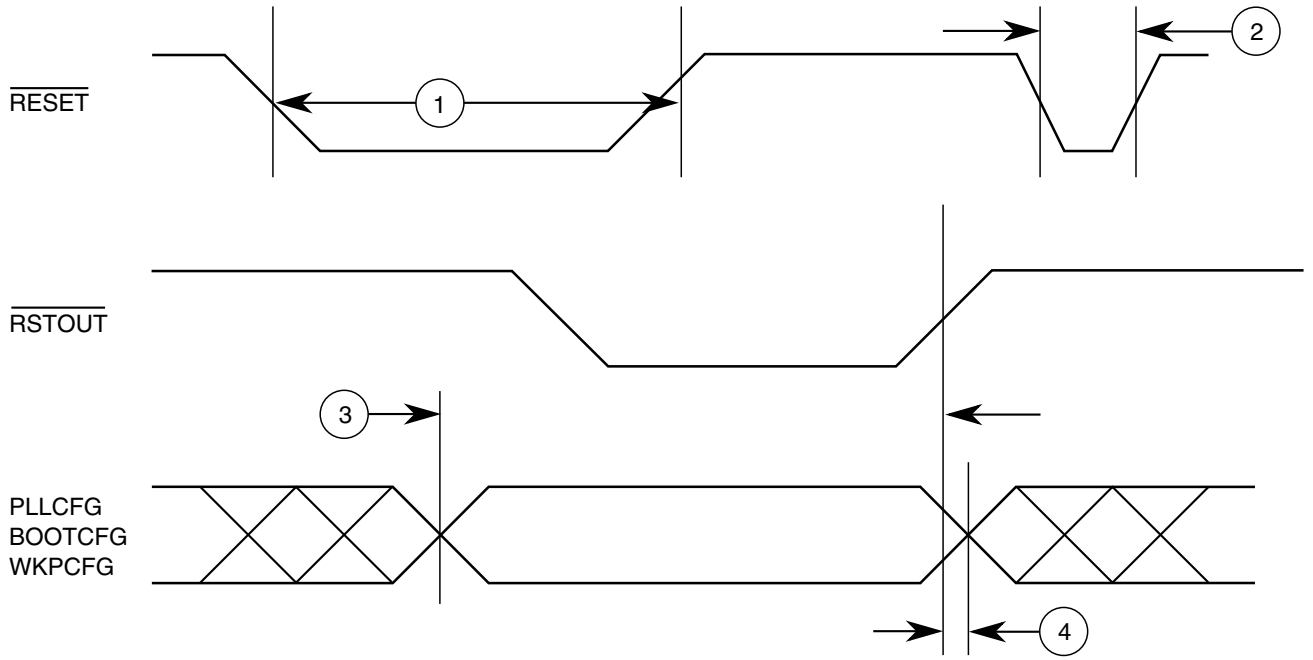


Figure 18. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

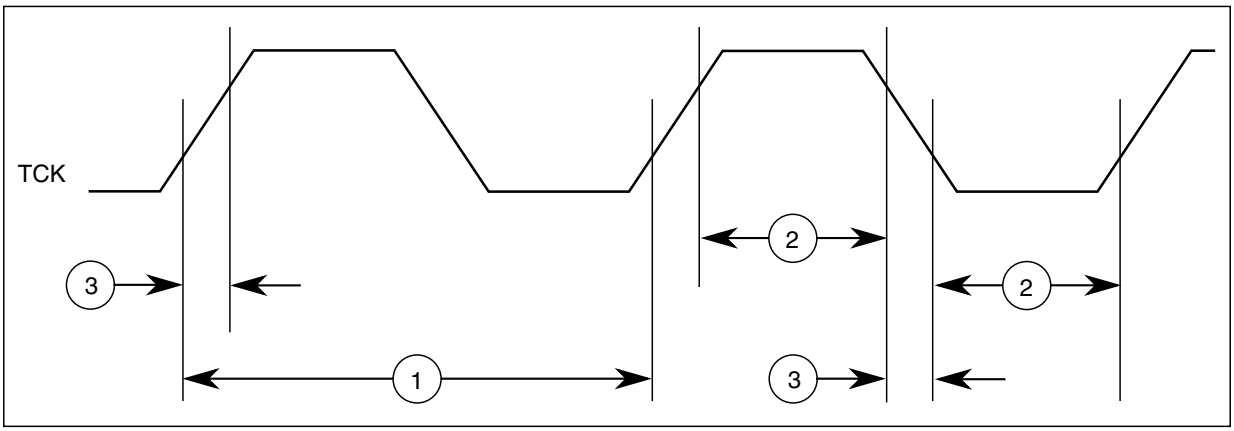


Figure 19. JTAG test clock input timing

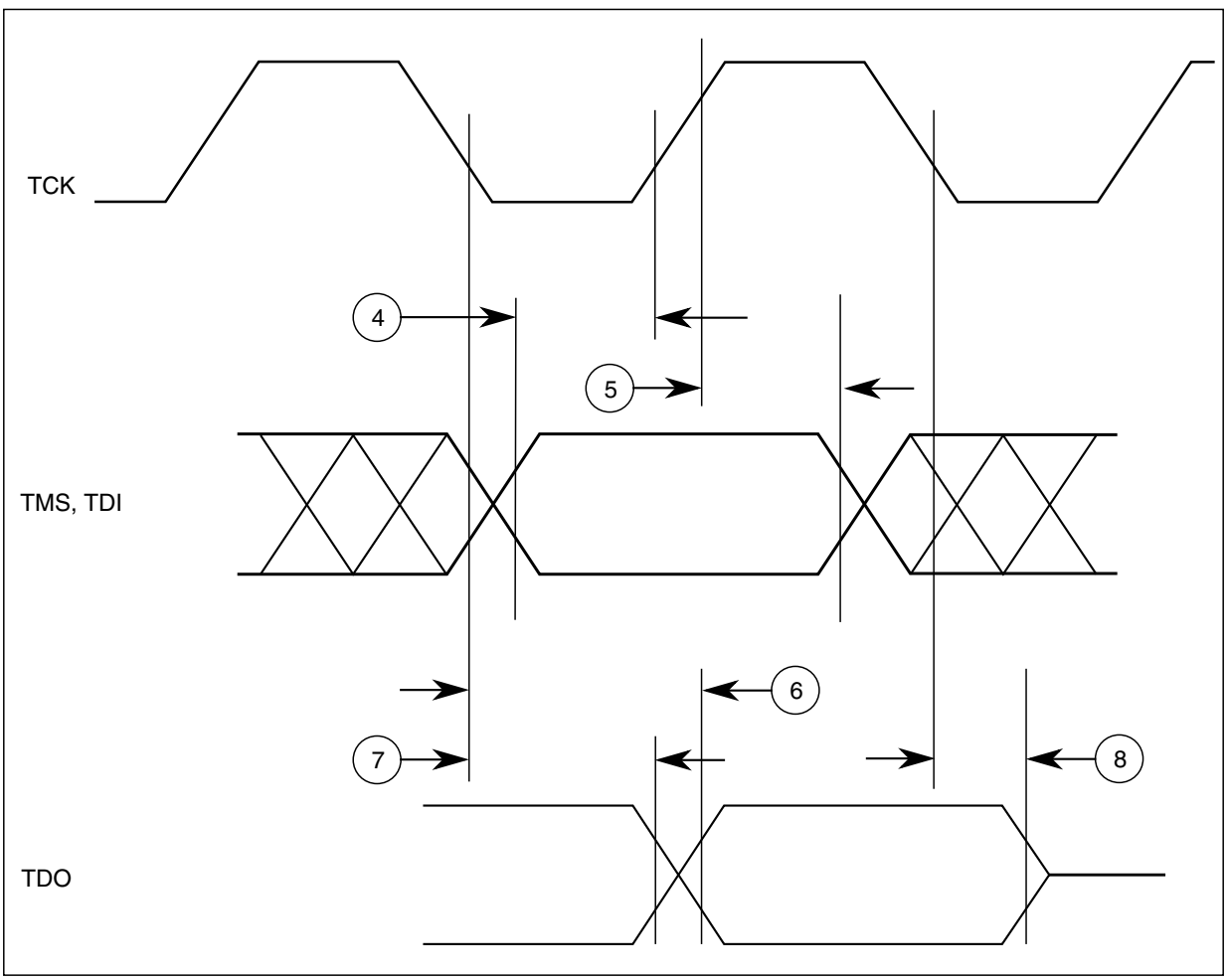


Figure 20. JTAG test access port timing

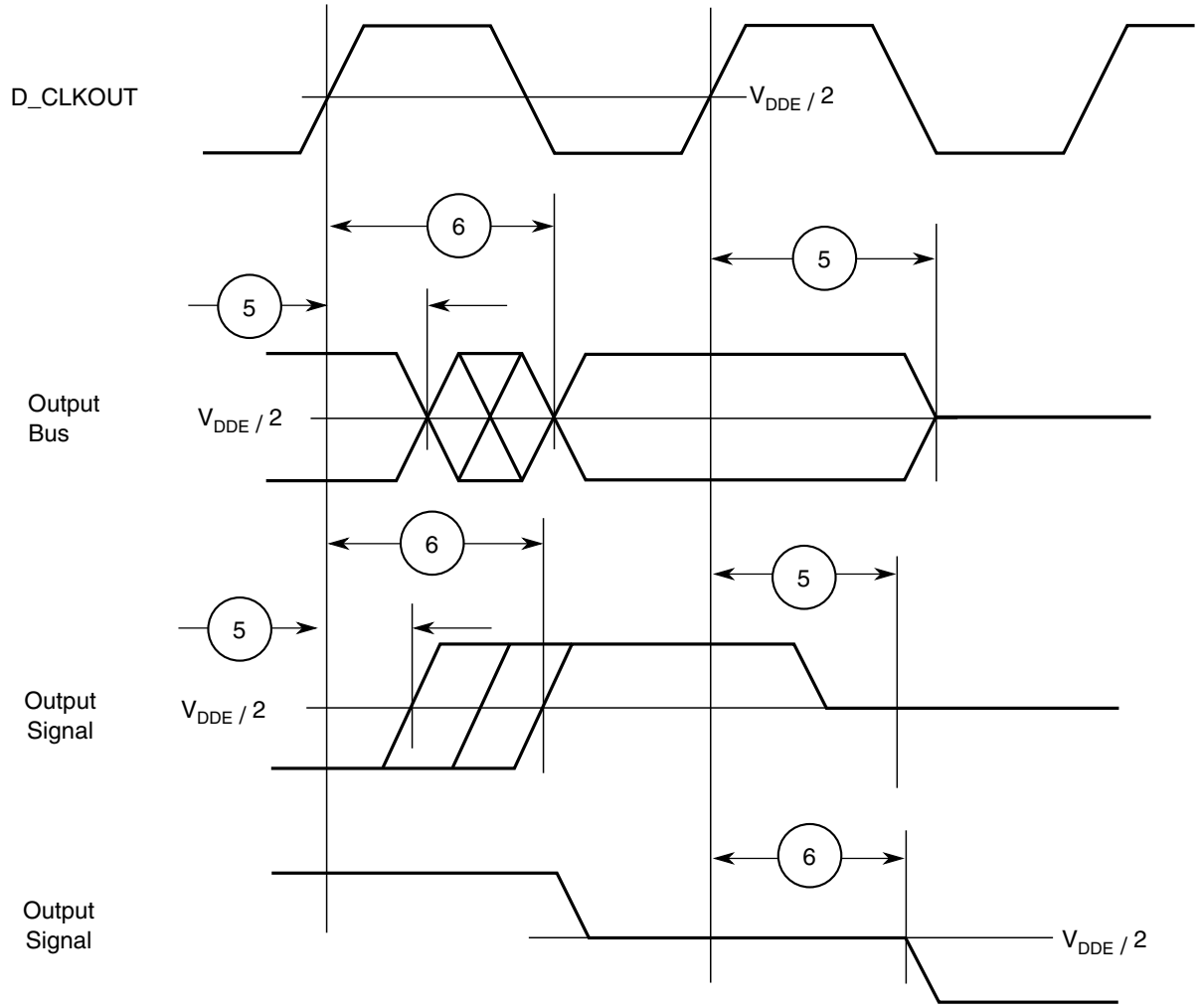


Figure 26. Synchronous output timing

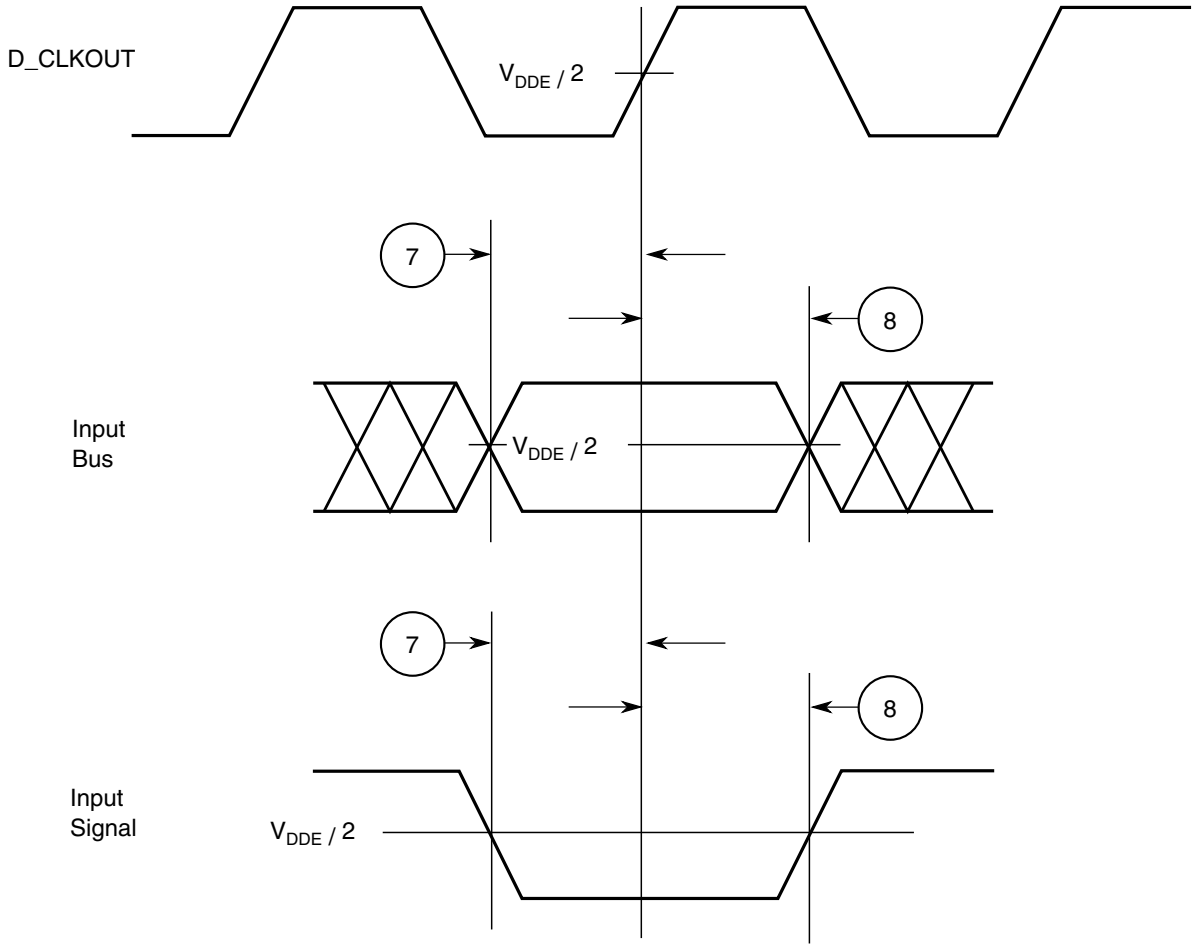


Figure 27. Synchronous input timing

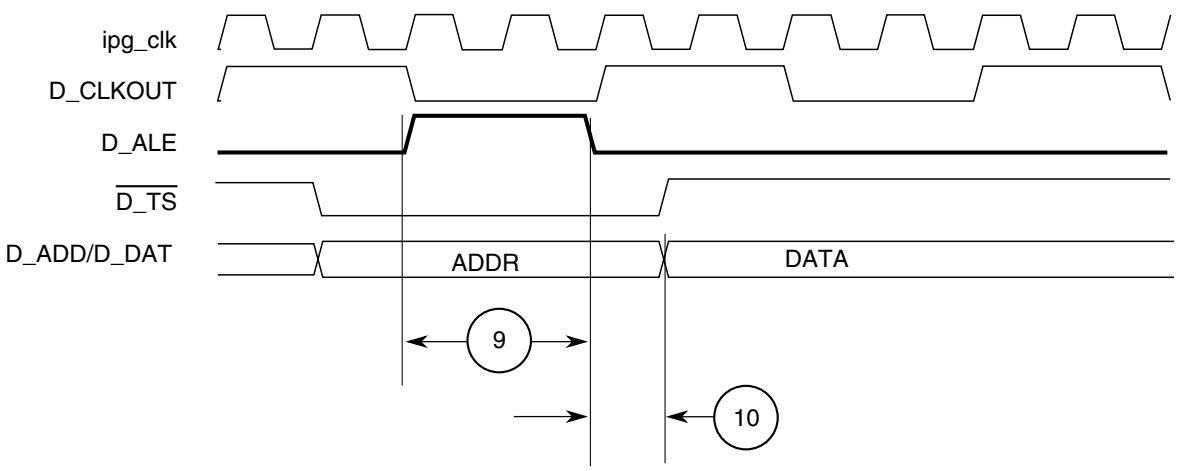


Figure 28. ALE signal timing

3.13.9 DSPI timing with CMOS and LVDS pads

NOTE

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 42. Timing specifications are shown in Table 43, Table 44, Table 45, Table 46, and Table 47.

Table 42. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1, 2]
CMOS (Master mode)	Full duplex – Classic timing (Table 43)	17
	Full duplex – Modified timing (Table 44)	30
	Output only mode (SCK/SOUT/PCS) (Table 43 and Table 44)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 47)	30
LVDS (Master mode)	Full duplex – Modified timing (Table 45)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 46)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.13.9.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.13.9.1.1 DSPI CMOS Master Mode — Classic Timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2] (continued)

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
3	t_{CSH}	PCS hold after SCK[6]	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	–33	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–35	—	ns
4	t_{SDC}	SCK duty cycle[7]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	ns
			PCR[SRC]=01b	50 pF	—	18.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	ns
			PCR[SRC]=01b	50 pF	–21.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

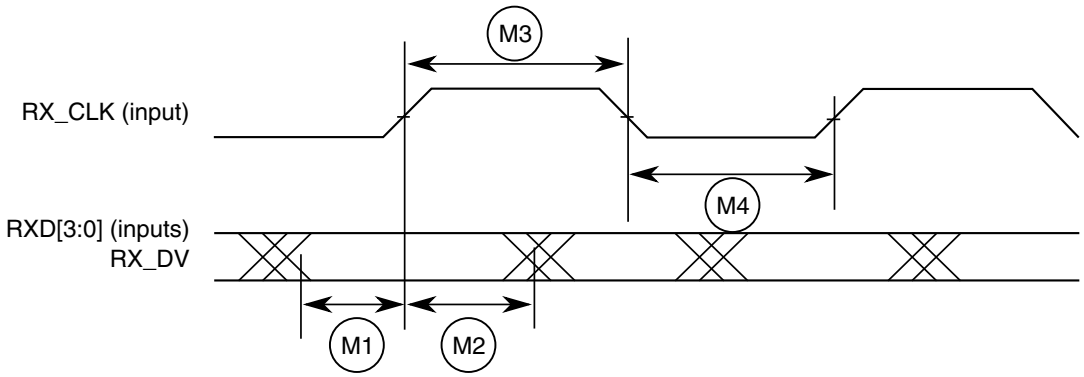


Figure 41. MII receive signal timing diagram

3.13.10.2 MII transmit signal timing (TXD[3:0], TX_EN, and TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of noncompliant MII PHYs.

Refer to the *MPC5777C Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 49. MII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN invalid	4.5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Table 56. Example orderable part numbers

Part number[1]	Package description	Speed (MHz)[2]	Operating temperature[3]	
			Min (T_L)	Max (T_H)
SPC5777CCK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 57. Revision history

Revision	Date	Description of changes
11	04/2017	In Figure 47 of Ordering information, added codes and firmware version information in definition of "Optional features field" • At end of line for *(blank)*, added "version 2.07" • Added line for *A* • At end of line for *R*, added "version 2.08" • At end of line for *C*, added "version 2.07" • Added line for *D* • At end of line for *L*, added "version 2.08"