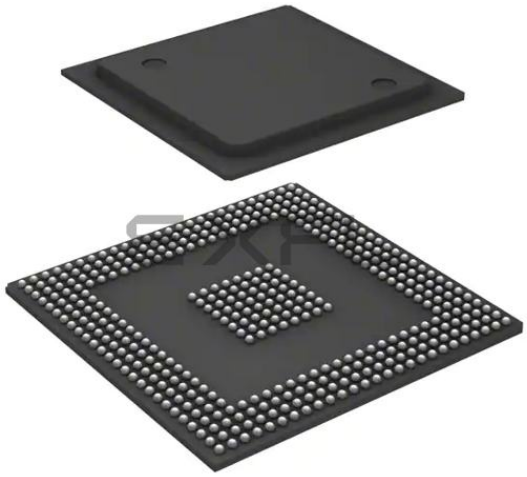

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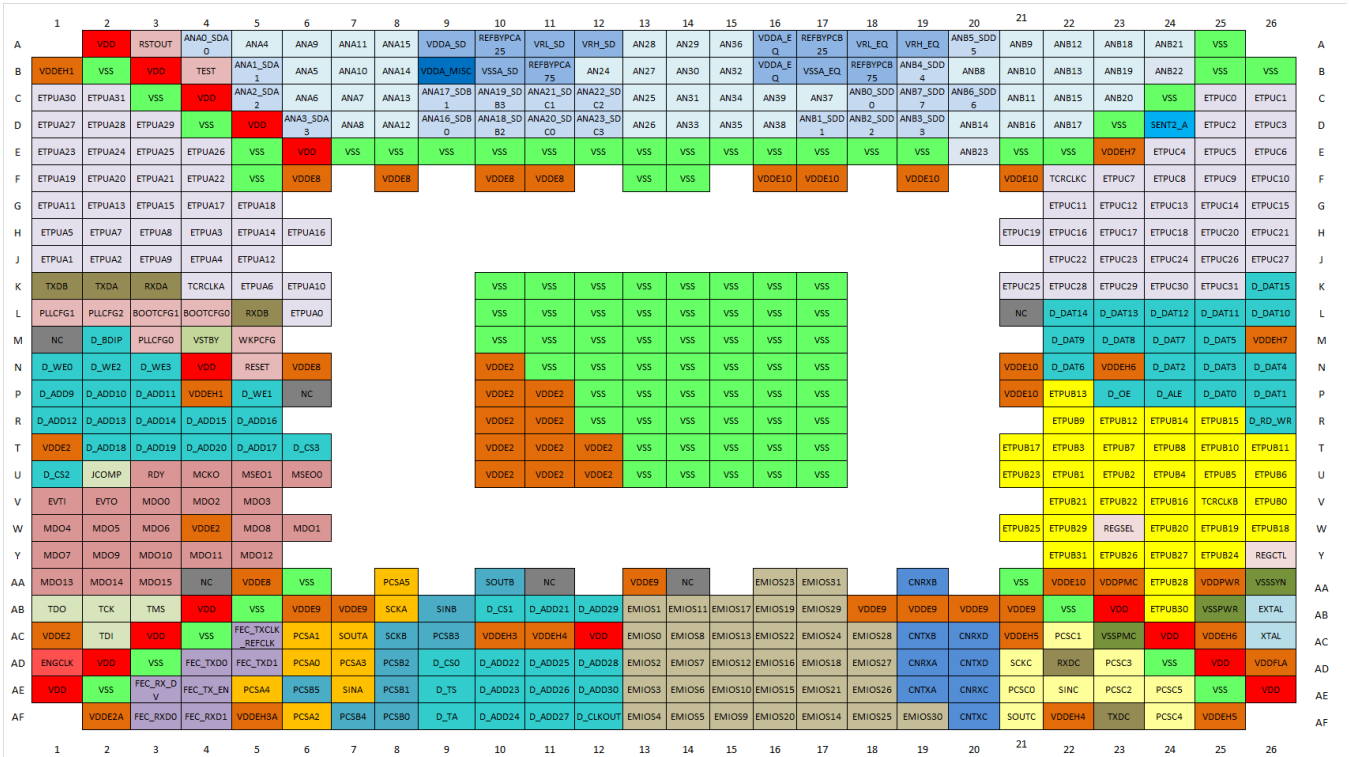
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777crk3mme3

Table of Contents

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0_SDA0	ANA4	ANA9	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN29	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB5_SDD5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN30	AN32	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB4_SDD4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA7	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA22_SDC2	AN25	AN31	AN34	AN39	AN37	ANB0_SDD0	ANB7_SDD7	ANB6_SDD6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA8	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA23_SDC3	AN26	AN33	AN35	AN38	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB14	ANB16	ANB17	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				NC	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	NC	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	NC				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	NC	VDDE8	VSS		PCSA5		SOUTB	NC		VDDE9	NC		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDDPMC	ETPUB28	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5777C 516-ball MAPBGA (full diagram)

3 Electrical characteristics

The following information includes details about power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Absolute maximum ratings

Absolute maximum specifications are stress ratings only. Functional operation at these maxima is not guaranteed.

CAUTION

Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

See Operating conditions for functional operation specifications.

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads
EBI pads	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
THD_{SE150}	Total harmonic distortion in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
SFDR	Spurious free dynamic range	Any GAIN	60	—	—	dB
Z_{DIFF}	Differential input impedance[10, 11]	GAIN = 1	1000	1250	1500	kΩ
		GAIN = 2	600	800	1000	
		GAIN = 4	300	400	500	
		GAIN = 8	200	250	300	
		GAIN = 16	200	250	300	
Z_{CM}	Common Mode input impedance[11, 12]	GAIN = 1	1400	1800	2200	kΩ
		GAIN = 2	1000	1300	1600	
		GAIN = 4	700	950	1150	
		GAIN = 8	500	650	800	
		GAIN = 16	500	650	800	
R_{BIAS}	Bare bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	Common Mode input reference voltage[13]	—	–12	—	+12	%
V_{BIAS}	Bias voltage	—	—	$V_{RH\_SD}/2$	—	V
δV_{BIAS}	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	Common mode rejection ratio	—	20	—	—	dB
R_{Caaf}	Anti-aliasing filter	External series resistance	—	—	20	kΩ
		Filter capacitances	220	—	—	pF
$f_{PASSBAND}$	Pass band[9]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	Pass band ripple[14]	0.333 * f_{ADCD_S}	–1	—	1	%

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$F_{rolloff}$	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
		[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
		[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
		[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
		[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	
δ_{GROUP}	Group delay	Within pass band: Tclk is f_{ADCD_M} / 2	—	—	—	—
		OSR = 24	—	—	235.5	Tclk
		OSR = 28	—	—	275	
		OSR = 32	—	—	314.5	
		OSR = 36	—	—	354	
		OSR = 40	—	—	393.5	
		OSR = 44	—	—	433	
		OSR = 48	—	—	472.5	
		OSR = 56	—	—	551.5	
		OSR = 64	—	—	630.5	
		OSR = 72	—	—	709.5	
		OSR = 75	—	—	696	
		OSR = 80	—	—	788.5	
		OSR = 88	—	—	867.5	
		OSR = 96	—	—	946.5	
		OSR = 112	—	—	1104.5	
		OSR = 128	—	—	1262.5	
		OSR = 144	—	—	1420.5	
		OSR = 160	—	—	1578.5	
		OSR = 176	—	—	1736.5	
		OSR = 192	—	—	1894.5	
		OSR = 224	—	—	2210.5	
		OSR = 256	—	—	2526.5	
		Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	High pass filter 3 dB frequency	Enabled	—	10e–5* fADCD_S	—	—
$t_{STARTUP}$	Startup time from power down state	—	—	—	100	µs
$t_{LATENCY}$	Latency between input data and converted data when input mux does not change[15]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	δ_{GROUP}	

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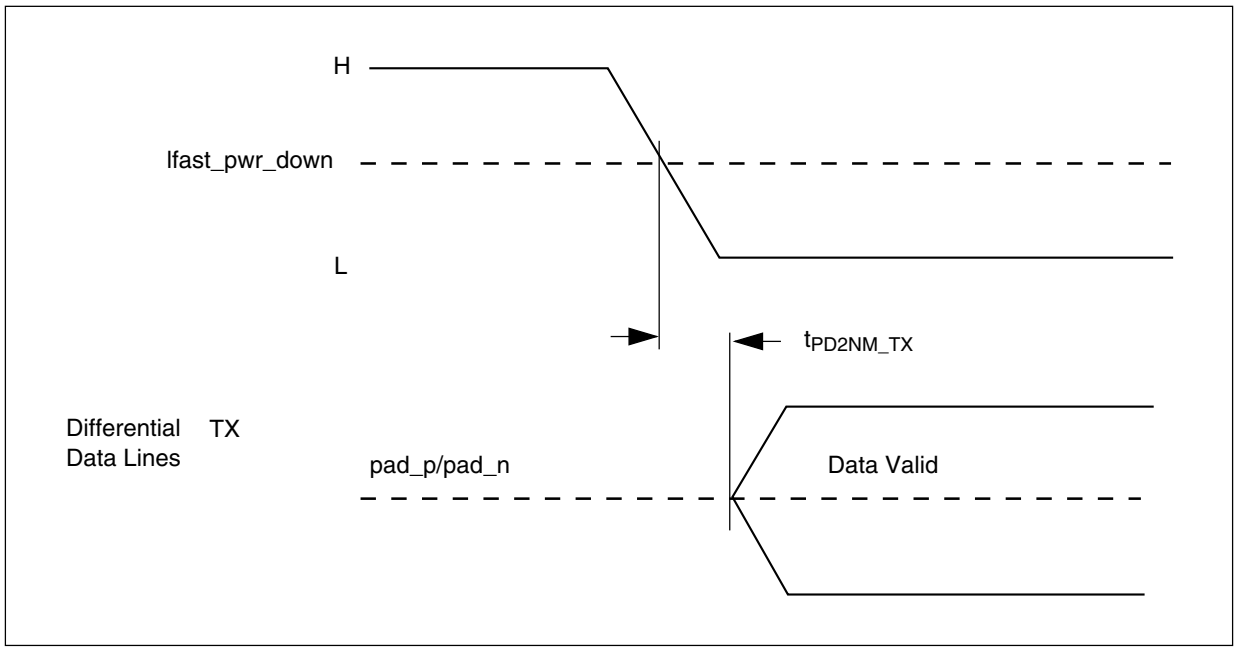

Figure 9. Power-down exit time

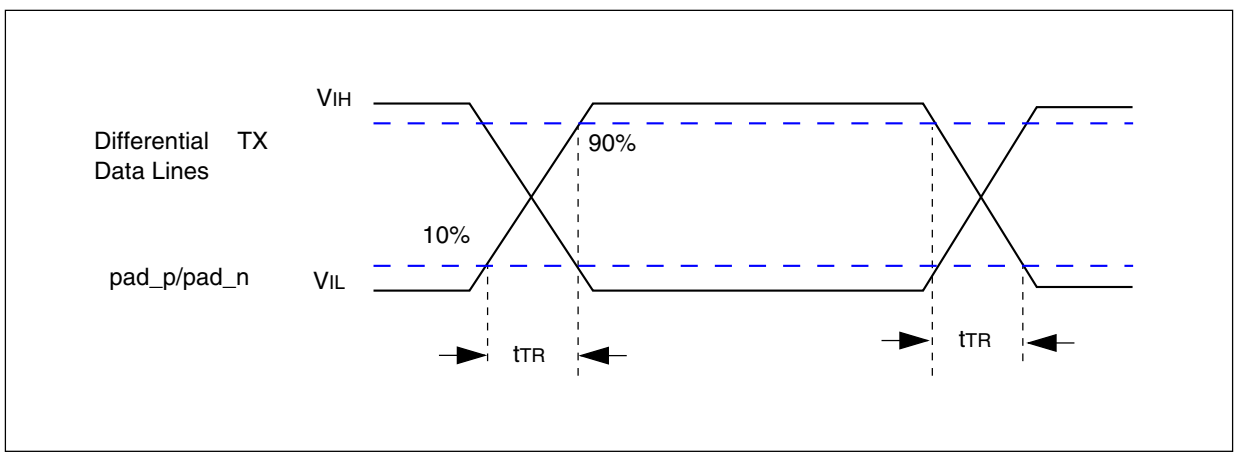

Figure 10. Rise/fall time

3.10.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 20. LVDS pad startup and receiver electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
STARTUP[2,3]						
t_{STRT_BIAS}	Bias current reference startup time[4]	—	—	0.5	4	µs

Table continues on the next page...

Table 23. LFAST PLL electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
ΔPER_{REF}	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps
		Long term, f_{RF_REF} = 10 MHz	–500	—	500	
ΔPER_{EYE}	Output Eye Jitter (peak to peak)[4]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. The 480 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 13 MHz or 26 MHz reference, the VCO frequency is 468 MHz.
3. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
4. Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. See Figure 11.

3.11 Power management: PMC, POR/LVD, power sequencing

3.11.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the V_{DDPMC} supply.

3.11.1.1 LDO mode recommended power transistors

Only specific orderable part numbers of MPC5777C support LDO regulation mode. See Ordering information for MPC5777C parts that support this regulation mode.

The following NPN transistors are recommended for use with the on-chip LDO voltage regulator controller: ON Semiconductor™ NJD2873. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

The following table describes the characteristics of the power transistors.

Table 24. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Maximum DC collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

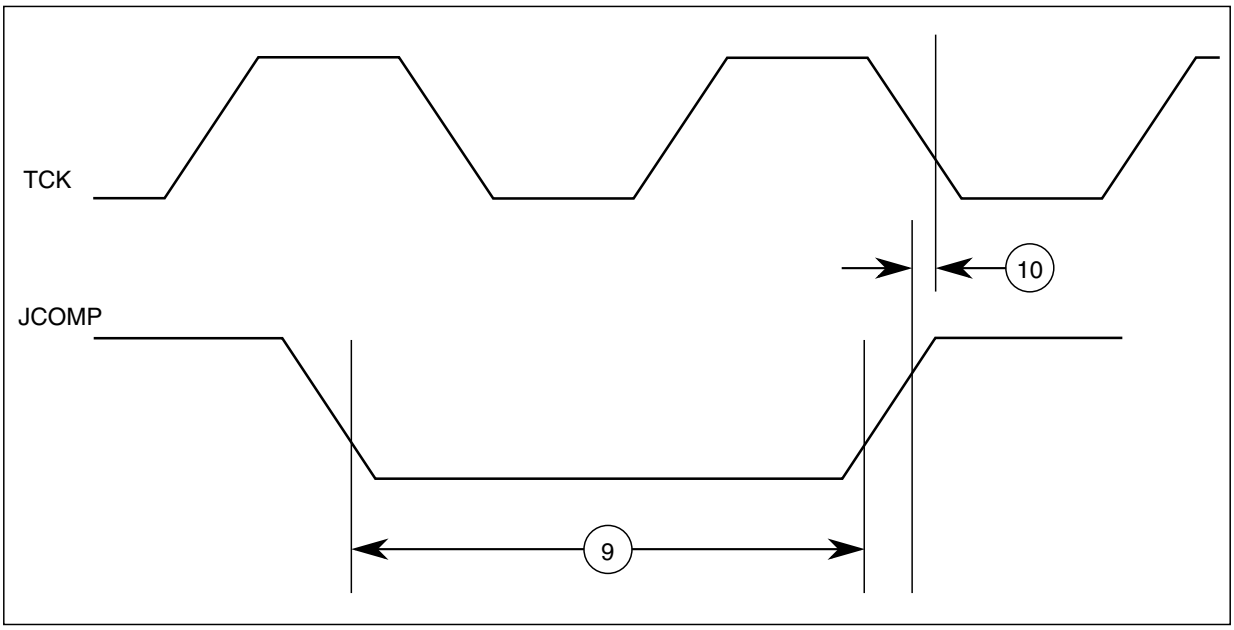

Figure 21. JTAG JCOMP timing

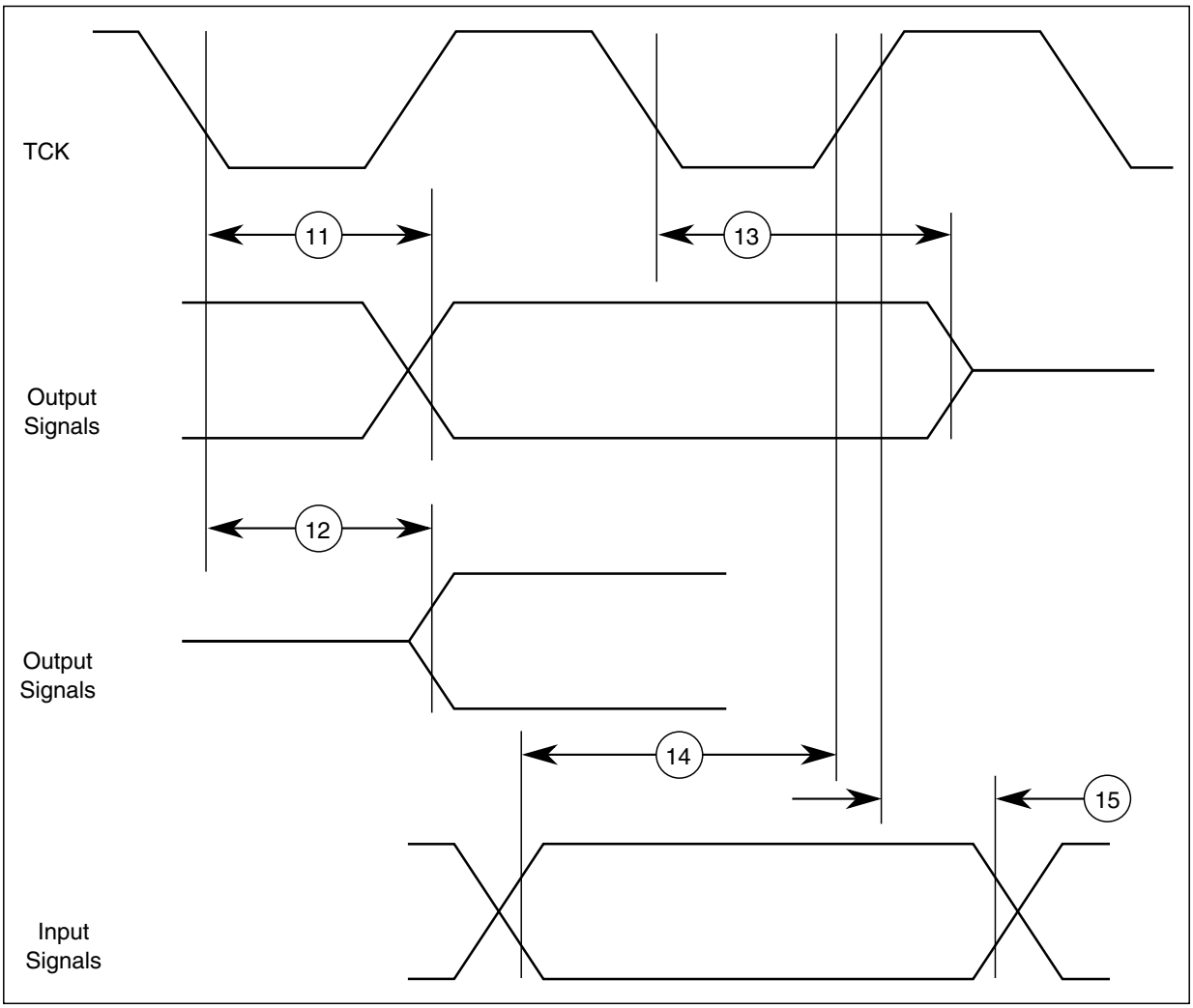

Figure 22. JTAG boundary scan timing

3.13.4 Nexus timing

Table 37. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	2[3]	—	t_{CYC}

Table continues on the next page...

Table 37. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{RDY}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

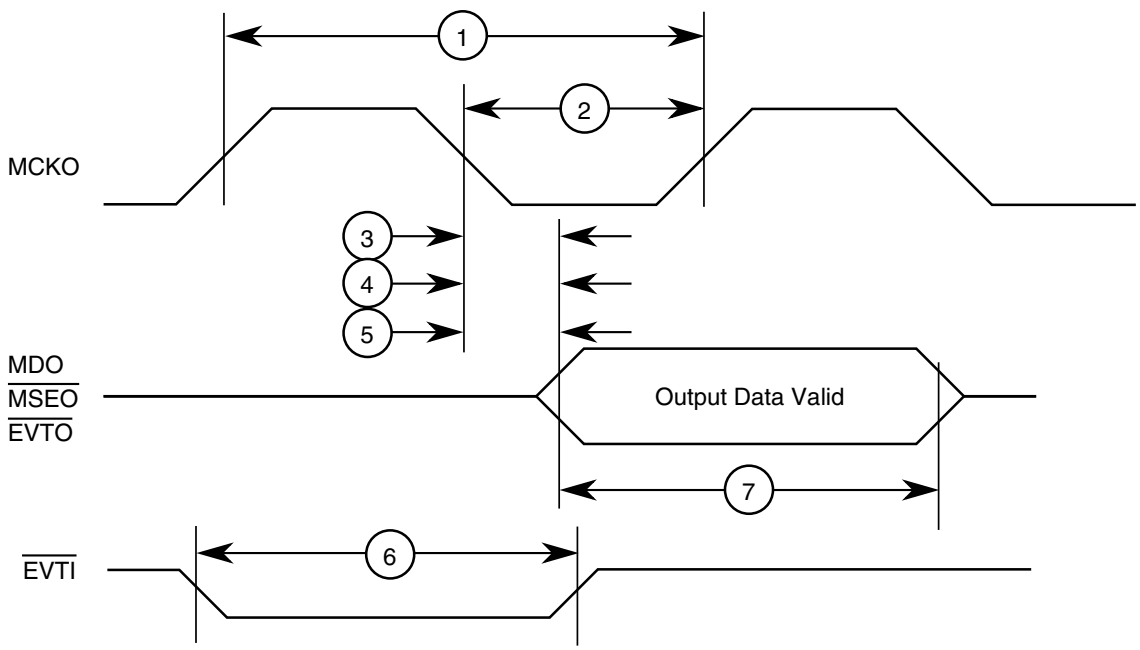

Figure 23. Nexus timings

3.13.6 External interrupt timing (IRQ/NMI pin)

Table 39. External Interrupt timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ/NMI Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ/NMI Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1. IRQ/NMI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H.
2. For further information on t_{cyc}, see Table 3.
3. Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

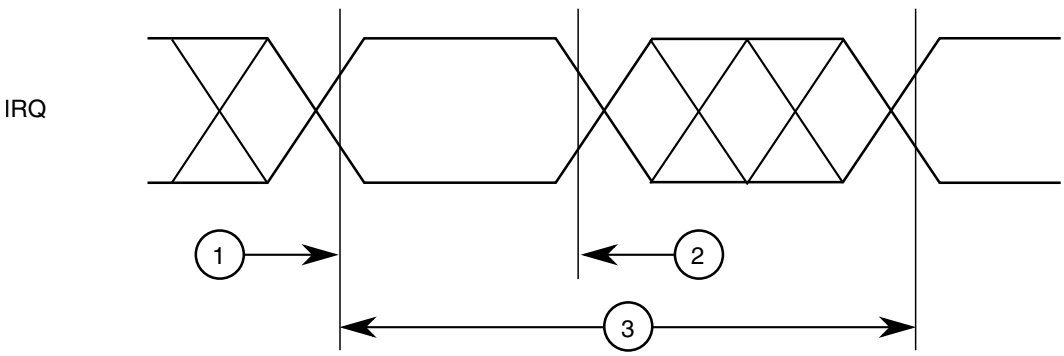

Figure 29. External interrupt timing

3.13.7 eTPU timing

Table 40. eTPU timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{CYC_ETPU}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{CYC_ETPU}[2]

1. eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. For further information on t_{CYC_ETPU}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK}$ – 5	$1/2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	50 pF	31 – ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	50 pF	62 – ($P^{11} \times t_{SYS}$, 6)	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							

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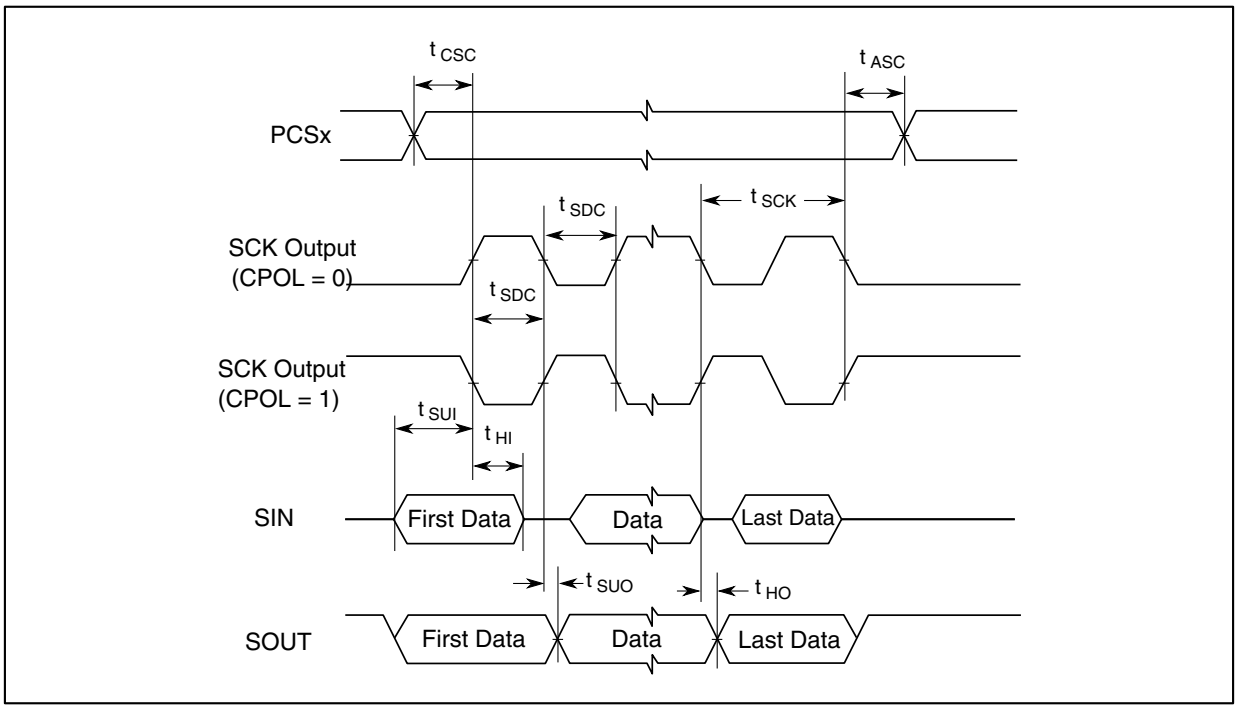

Figure 38. DSPI LVDS master mode – modified timing, CPHA = 0

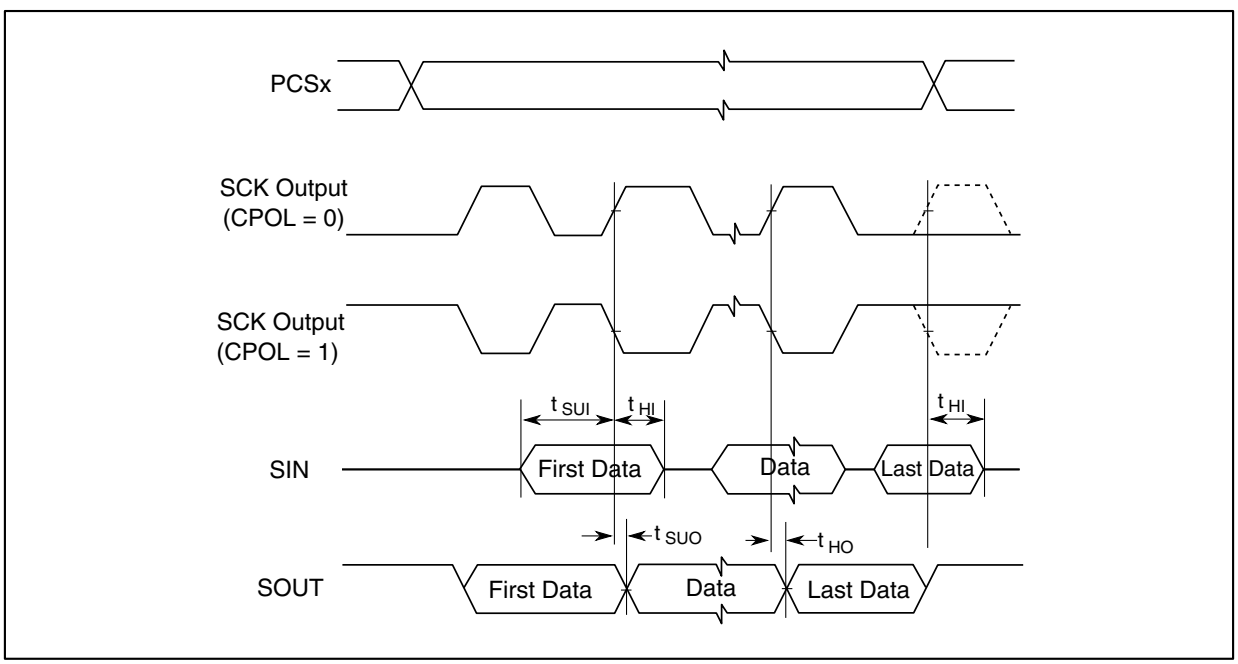

Figure 39. DSPI LVDS master mode – modified timing, CPHA = 1

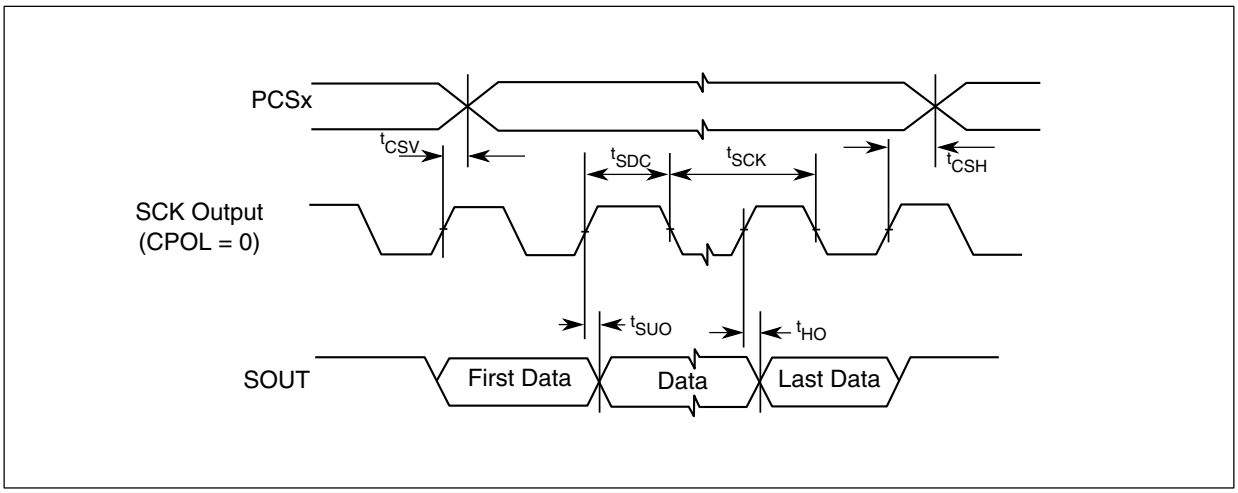

Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

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