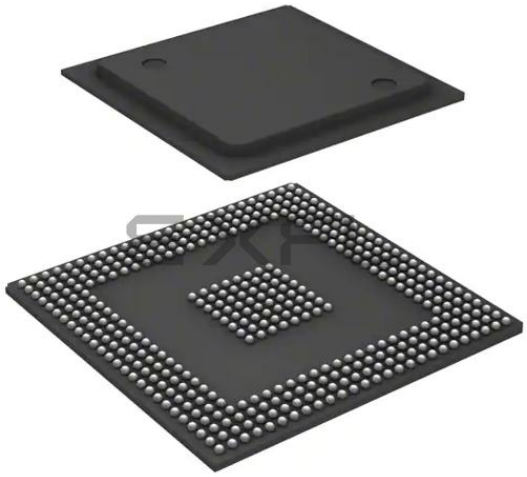

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Details	
Product Status	Active
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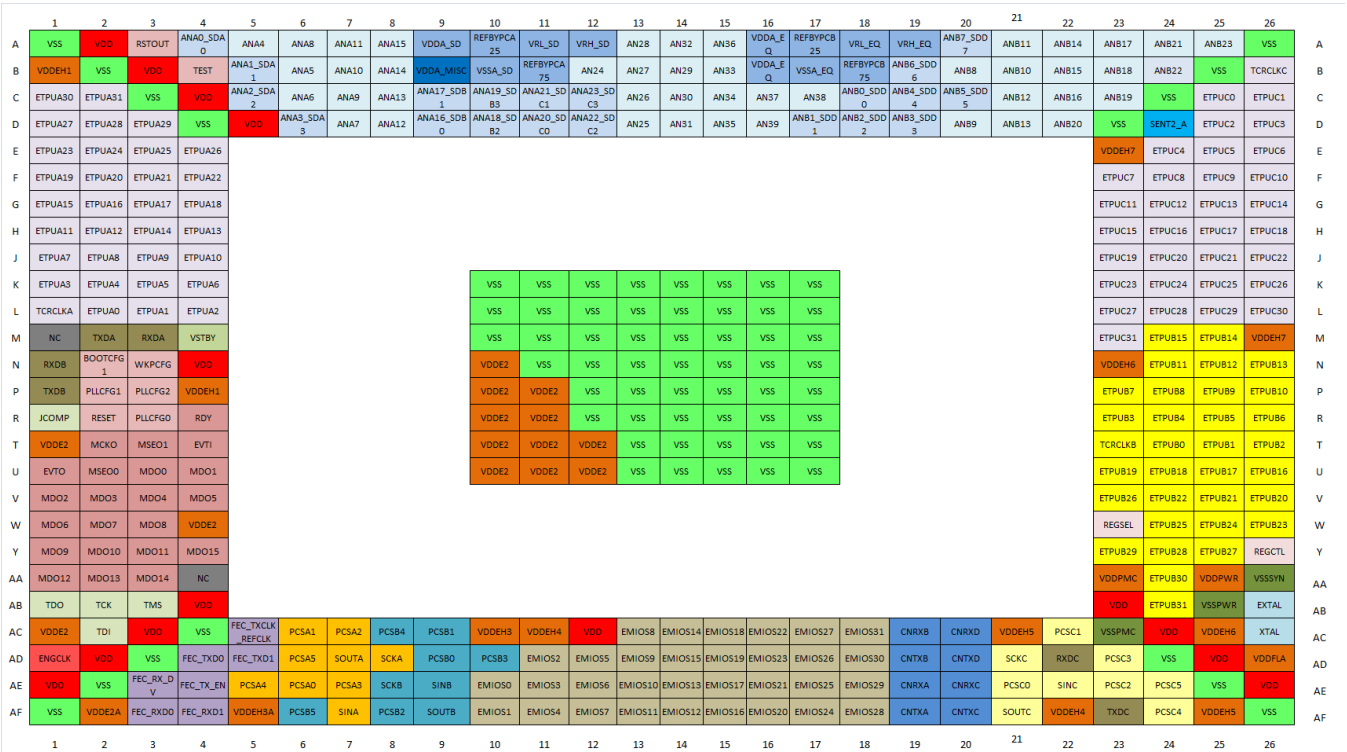
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777csk3mme3

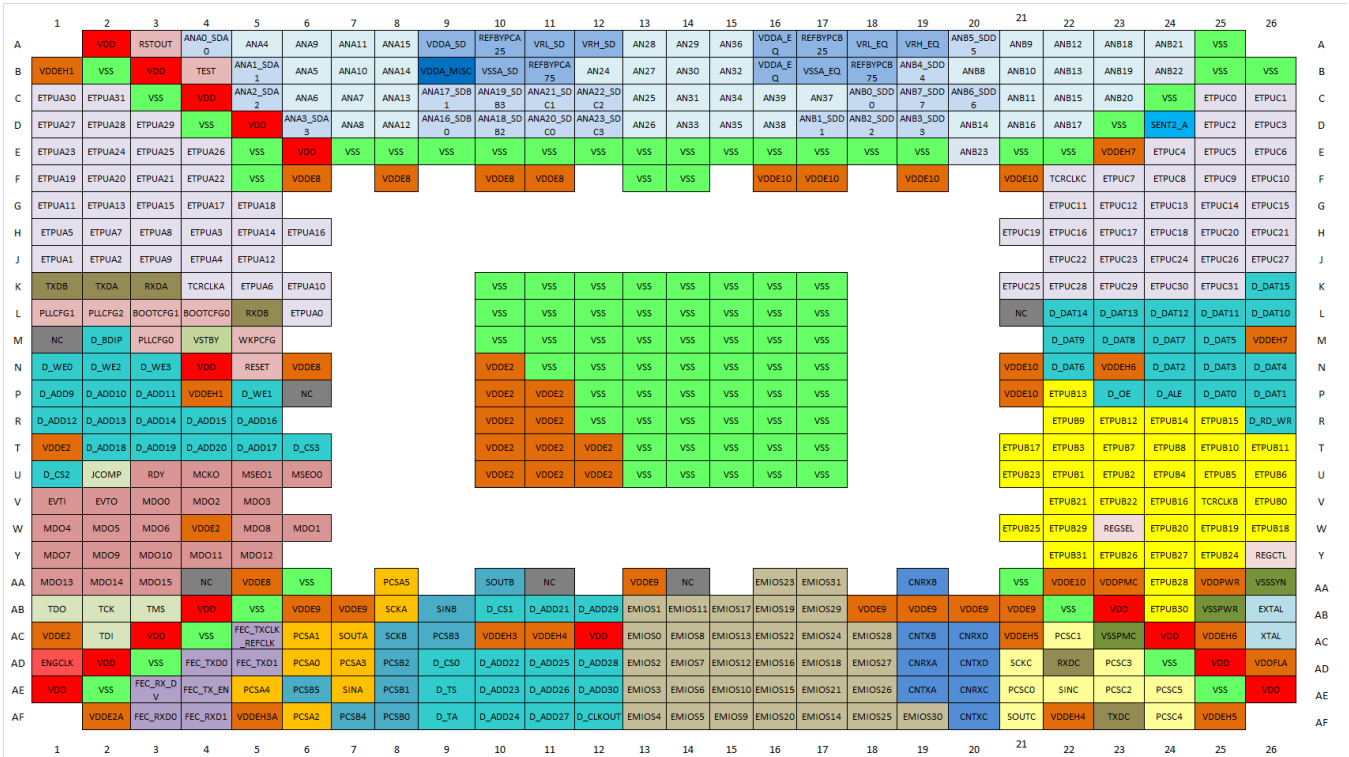


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	AN87_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	AN88	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0_SDA0	ANA4	ANA9	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN29	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB5_SDD5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN30	AN32	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB4_SDD4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA7	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA22_SDC2	AN25	AN31	AN34	AN39	AN37	ANB0_SDD0	ANB7_SDD7	ANB6_SDD6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA8	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA23_SDC3	AN26	AN33	AN35	AN38	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB14	ANB16	ANB17	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				NC	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	NC	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	NC				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	NC	VDDE8	VSS		PCSA5		SOUTB	NC		VDDE9	NC		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDDPMC	ETPUB28	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5777C 516-ball MAPBGA (full diagram)

3 Electrical characteristics

The following information includes details about power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Absolute maximum ratings

Absolute maximum specifications are stress ratings only. Functional operation at these maxima is not guaranteed.

CAUTION

Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

See Operating conditions for functional operation specifications.

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1] (continued)

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
t_{R_F}	GPIO pad output transition time (rise/fall)	PCR[SRC] = 11b	C_L = 25 pF	—	—	1.2	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	2.5	
			C_L = 200 pF	—	—	8	
		PCR[SRC] = 11b	C_L = 25 pF	—	—	1.7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	3.25	
			C_L = 200 pF	—	—	12	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	5	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	18	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	25	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	13	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	24	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	30	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	24	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	50	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	51	
t_{PD}	GPIO pad output propagation delay time	PCR[SRC] = 11b	C_L = 50 pF	—	—	6	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	13	
		PCR[SRC] = 11b	C_L = 50 pF	—	—	8.25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	19.5	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	9	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	22	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	12.5	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	35	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	27	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	40	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	45	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	75	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	100	
$\lvert t_{SKEW\_W} \rvert$	Difference between rise and fall time	—		—	—	25	%

1. All GPIO pad output specifications are valid for 3.0 V < V_{DDEx} < 5.5 V, except where explicitly stated.

2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

The following table shows the EBI CLKOUT, address, and control signal pad electrical characteristics. These pads can also be used for GPIO.

Table 10. GPIO and EBI CLKOUT, address, and control signal pad output buffer electrical characteristics (FC pads)

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications: valid for 3.0 V < V_{DDEx} < 3.6 V							
C_{DRV}	External bus load capacitance	PCR[DSC] = 01b		—	—	10	pF
		PCR[DSC] = 10b		—	—	20	
		PCR[DSC] = 11b		—	—	30	
f_{MAX_EBI}	External bus maximum operating frequency	C_{DRV} = 10/20/30 pF		—	—	66	MHz
GPIO and EBI Mode Output Specifications							
I_{OH_EBI}	GPIO and external bus pad output high current	V_{OH} = 0.8 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	30	—	—	mA
			PCR[DSC] = 10b	22	—	—	
			PCR[DSC] = 01b	13	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OH} = 0.8 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	16	—	—	
			PCR[DSC] = 10b	12	—	—	
			PCR[DSC] = 01b	7	—	—	
			PCR[DSC] = 00b	1	—	—	
I_{OL_EBI}	GPIO and external bus pad output low current	V_{OL} = 0.2 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	54	—	—	mA
			PCR[DSC] = 10b	25	—	—	
			PCR[DSC] = 01b	16	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OL} = 0.2 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	17	—	—	
			PCR[DSC] = 10b	14	—	—	
			PCR[DSC] = 01b	8	—	—	
			PCR[DSC] = 00b	1	—	—	
$t_{R\_F\_EBI}$	GPIO and external bus pad output transition time (rise/fall)	PCR[DSC] = 11b	C_L = 30 pF	—	—	1.5	ns
			C_L = 50 pF	—	—	2.4	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	1.5	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	1.85	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	45	
t_{PD_EBI}	GPIO and external bus pad output propagation delay time	PCR[DSC] = 11b	C_L = 30 pF	—	—	4.2	ns
			C_L = 50 pF	—	—	5.5	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	4.2	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	4.4	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	59	

Table 15. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
01110	14.9
01111	15.8

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the die and package capacitances given by C_{S_XTAL}/C_{S_EXTAL} in Table 14.

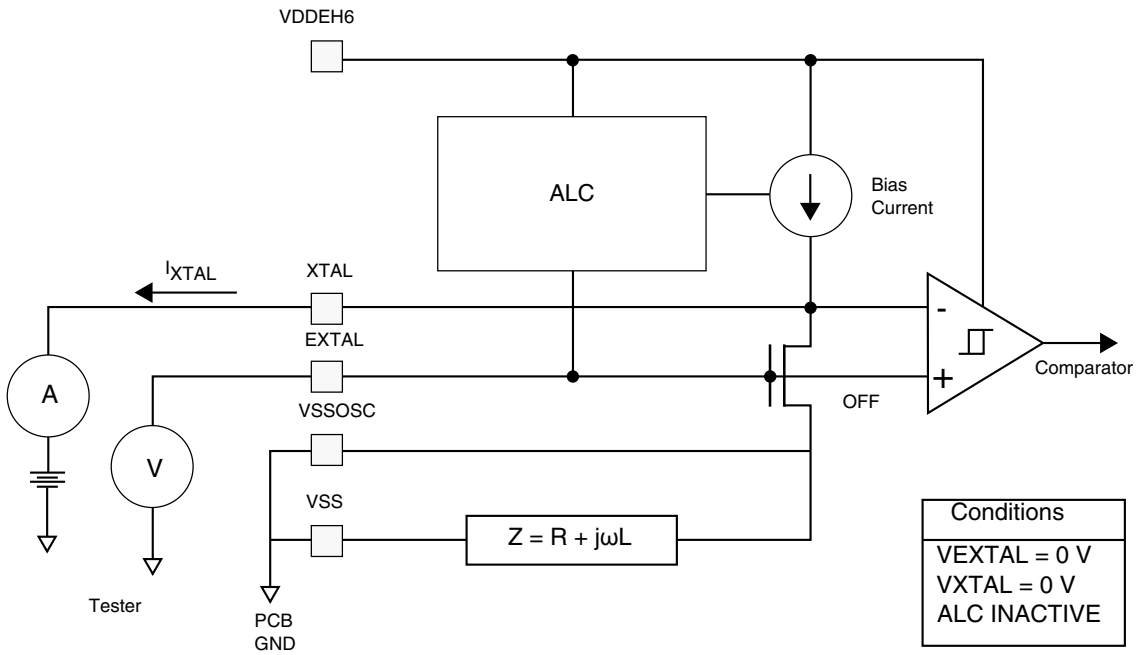


Figure 7. Test circuit

Table 16. Internal RC (IRC) oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRC target frequency	—	—	16	—	MHz
δf_{var_T}	IRC frequency variation	T < 150 °C	–8	—	8	%

3.8 Analog-to-Digital Converter (ADC) electrical specifications

5. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.
6. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
7. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.
8. Condition applies to two adjacent pins at injection limits.
9. Performance expected with production silicon.
10. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.
11. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
12. TUE does not apply to differential conversions.
13. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
14. Guaranteed 10-bit monotonicity.
15. At $V_{RH\_EQ} - V_{RL\_EQ} = 5.12$ V, one LSB = 1.25 mV.

3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

NOTE

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

Table 18. SDADC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	V_{DDA_SD}	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended $V_{INM} = V_{RL\_SD}$	V_{RH_SD}/GAIN			V
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 1	±0.5*V_{RH_SD}			
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 2,4,8,16	±V_{RH_SD}/GAIN			
		Differential $0 < V_{IN} < V_{DDEx}$	±V_{RH_SD}/GAIN			
f_{ADCD_M}	SD clock frequency[4]	—	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	—	—	—	333	Ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	SD register resolution[5]	2's complement notation	16			bit

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
GAIN	ADC gain	Defined through SDADC_MCR[PGAN]. Only integer powers of 2 are valid gain values.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$	Absolute value of the ADC gain error[6, 7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	Conversion offset[6, 7]	Before calibration (applies to all gain settings: 1, 2, 4, 8, 16)	—	10*(1+1/gain)	20	mV
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	72	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	69	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	66	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	62	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be “clipped.”
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5*V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range $3.6\ V < V_{DDA\_SD} < 4.0\ V$: SNR parameter degrades by 3 dB. SDADC is functional in the range $3.0\ V < V_{RH\_SD} < 4.0\ V$: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

Table 29. Voltage monitor electrical characteristics[1, 2] (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR_HV	HV V_{DDPMC} supply power on reset threshold	Rising voltage (powerup)	N/A	No	Enab.	2444	2600	2756	mV
		Falling voltage (power down)				2424	2580	2736	
LVD_HV	HV internal V_{DDPMC} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2946	3010	3066	
		Falling voltage (trimmed)				2934	2998	3044	
HVD_HV	HV internal V_{DDPMC} supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	5696	5860	5968	mV
		Falling voltage				5666	5830	5938	
LVD_FLASH	FLASH supply low voltage monitoring[6]	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2956	3010	3053	
		Falling voltage (trimmed)				2944	2998	3041	
HVD_FLASH	FLASH supply high voltage monitoring[6]	Rising voltage	4bit	Yes	Disab.	3456	3530	3584	mV
		Falling voltage				3426	3500	3554	
LVD_IO	Main I/O V_{DDEH1} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	3250	3350	3488	mV
		Falling voltage (untrimmed)				3220	3320	3458	
		Rising voltage (trimmed)				3347	3420	3468	
		Falling voltage (trimmed)				3317	3390	3438	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	µs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	µs

1. LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed; LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.
2. HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed; HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.
3. POR098_c threshold is an untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
6. V_{DDFLA} range is guaranteed when internal flash memory regulator is used.

3.11.4 Power sequencing requirements

Requirements for power sequencing include the following.

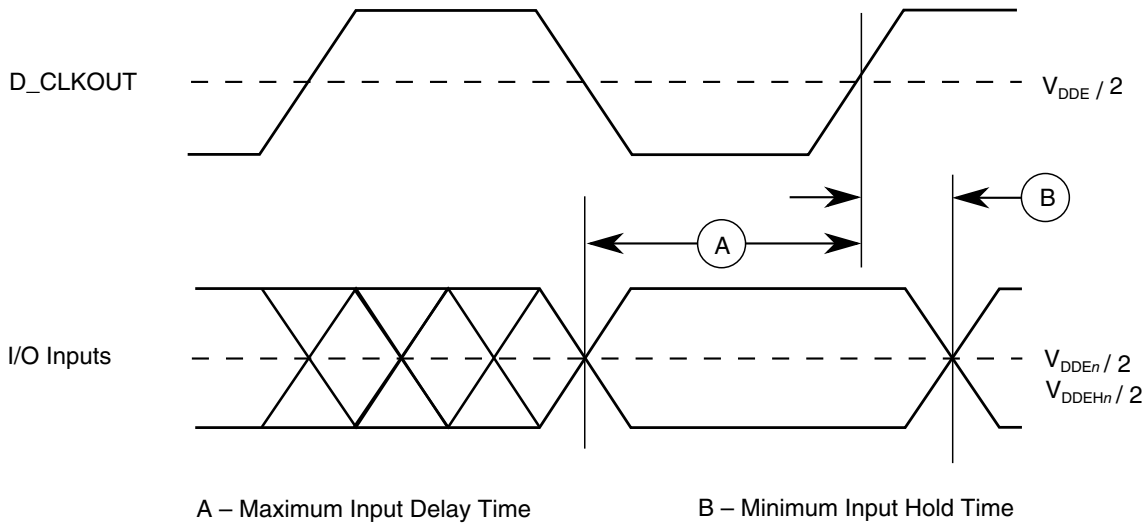


Figure 17. Generic input setup/hold timing

3.13.2 Reset and configuration pin timing

Table 35. Reset and configuration pin timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, TA = TL to TH.
2. For further information on t_{cyc}, see Table 3.

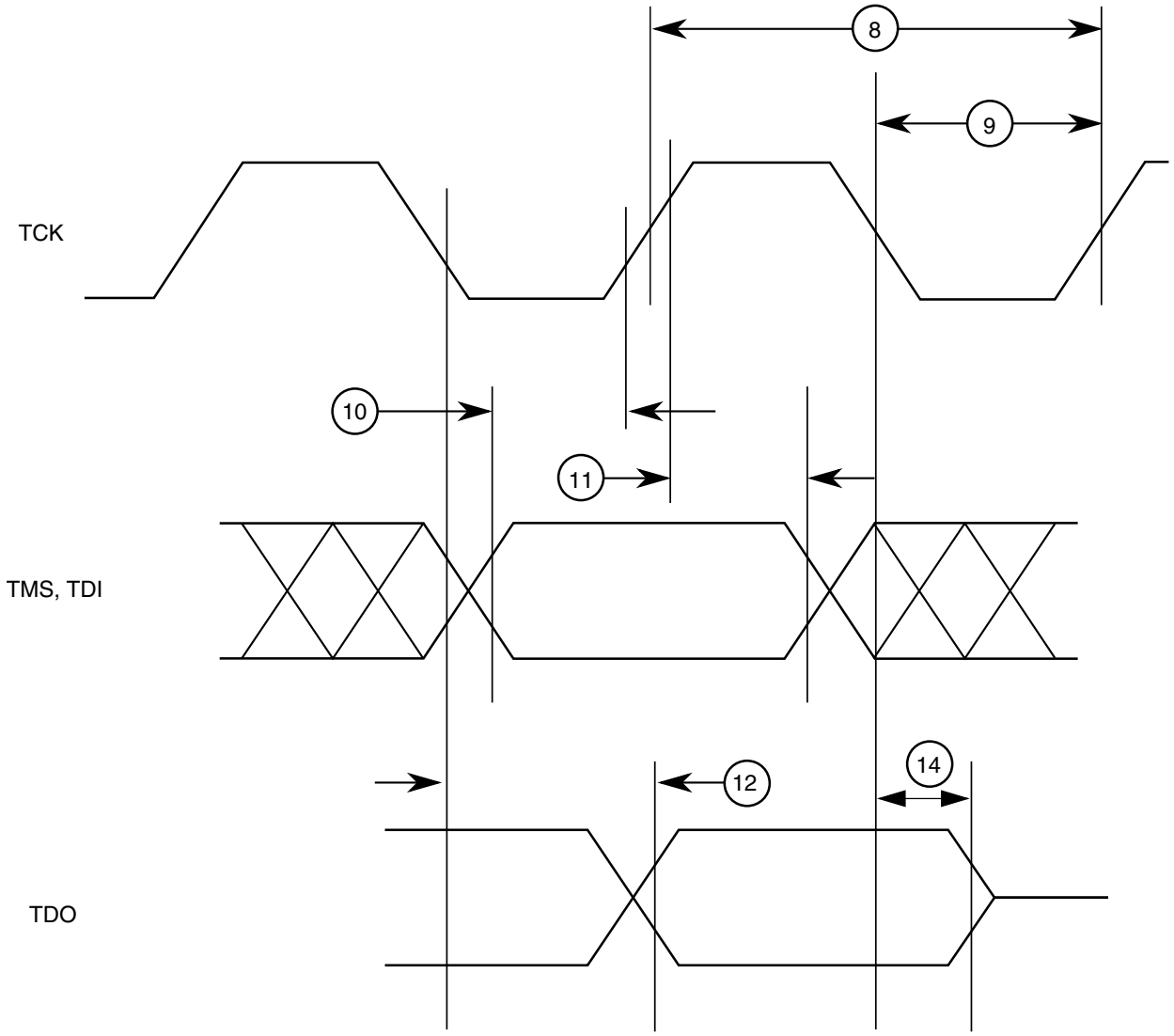


Figure 24. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External Bus Interface (EBI) timing

Table 38. Bus operation timing[1]

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	—
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	—
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	—

Table continues on the next page...

Table 38. Bus operation timing[1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3]	t_{COV}	—	8.5/9.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
	D_DAT[0:15]			11.5		—
	D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]			8.5/9.0		Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	t_{CIS}	7.5	—	ns	—
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	t_{CIH}	1.0	—	ns	—
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.

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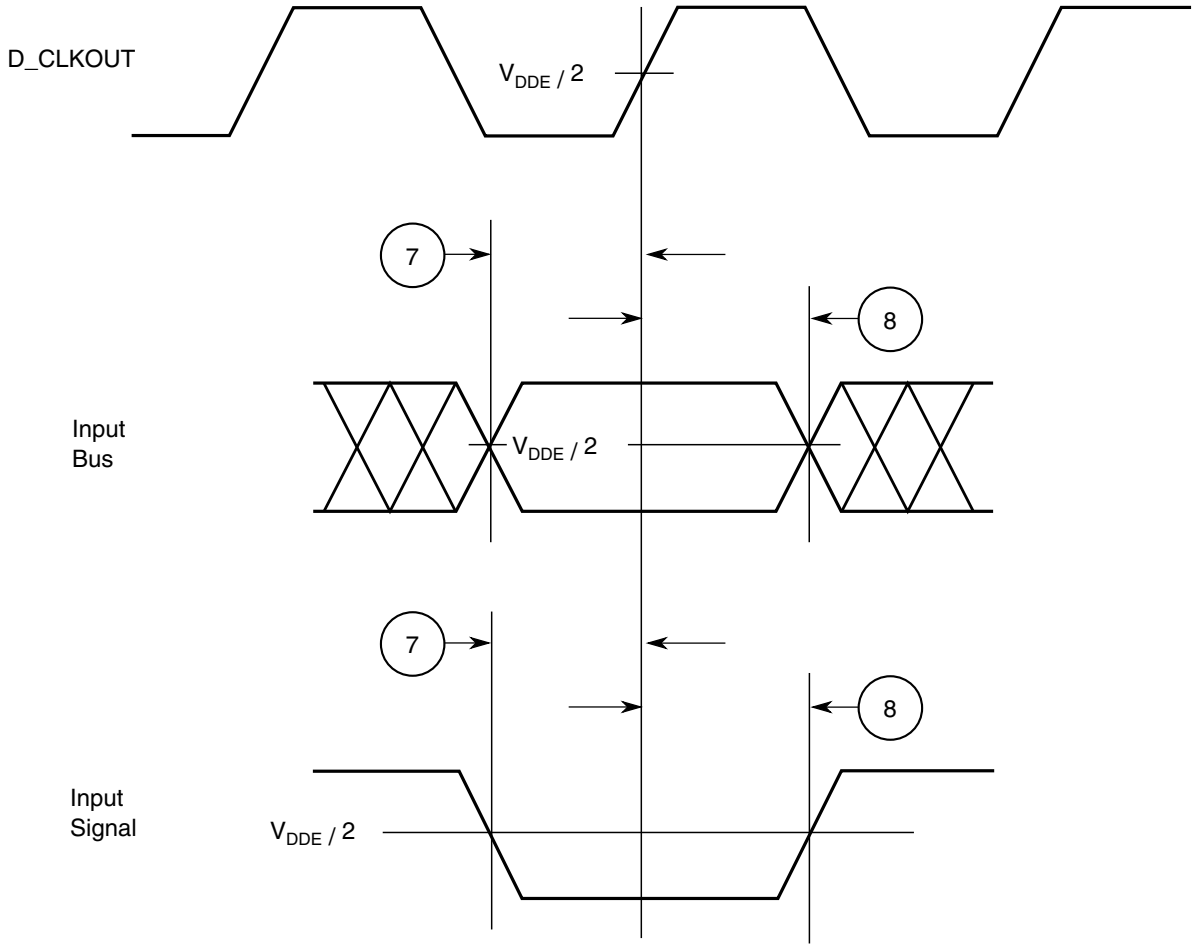


Figure 27. Synchronous input timing

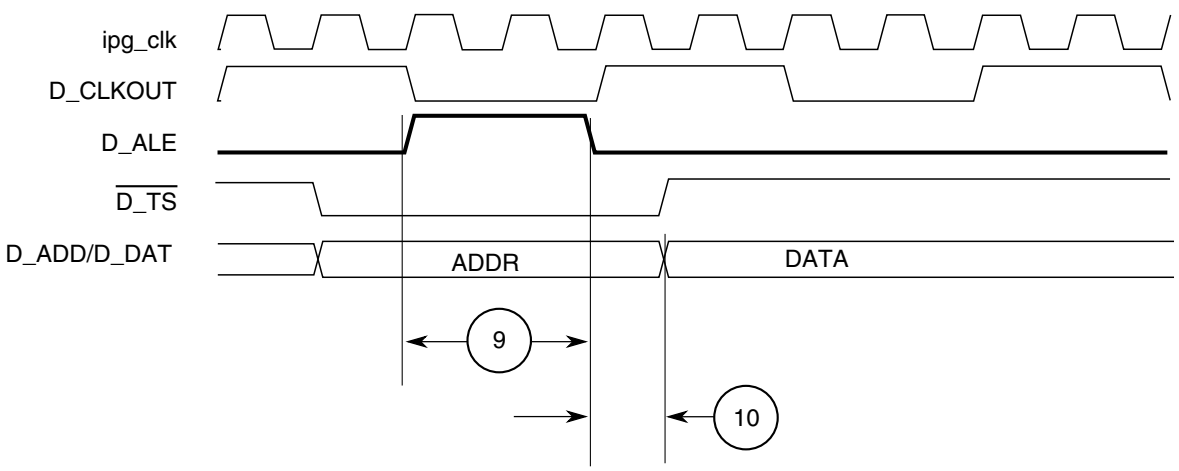


Figure 28. ALE signal timing

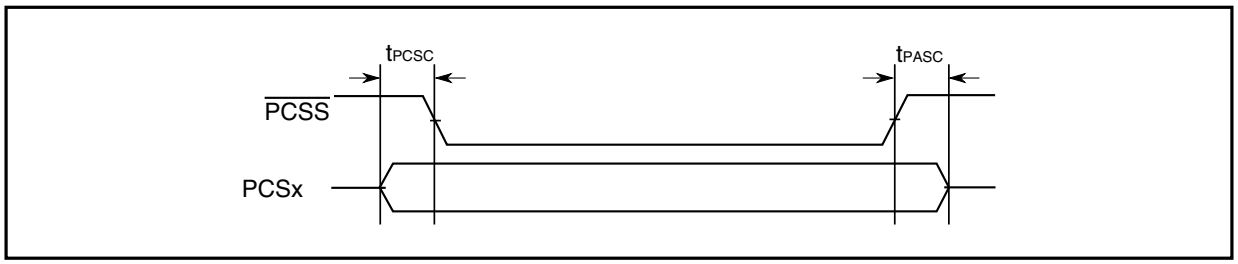


Figure 37. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.3 DSPI LVDS Master Mode – Modified Timing

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 25 pF differential	33.3	—	ns
2	t_{CSC}	PCS to SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	25 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=10b	50 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=01b	50 pF	($N^4 \times t_{SYS}$, [5]) – 32	—	ns
3	t_{ASC}	After SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
			PCS: PCR[SRC]=10b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
			PCS: PCR[SRC]=01b	PCS: 0 pF SCK: 25 pF	($M^6 \times t_{SYS}$, [5]) – 8	—	ns
4	t_{SDC}	SCK duty cycle[7]	LVDS	15 pF to 25 pF differential	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ +2	ns
7	t_{SUI}	**SIN setup time**					
		SIN setup time to SCK CPHA = 0[8]	LVDS	15 pF to 25 pF differential	23 – ($P^9 \times t_{SYS}$, [5])	—	ns
		SIN setup time to SCK CPHA = 1[8]	LVDS	15 pF to 25 pF differential	23	—	ns
8	t_{HI}	**SIN hold time**					
		SIN hold time from SCK CPHA = 0[8]	LVDS	0 pF differential	–1 + ($P^9 \times t_{SYS}$, [5])	—	ns
		SIN hold time from SCK CPHA = 1[8]	LVDS	0 pF differential	–1	—	ns

Table continues on the next page...

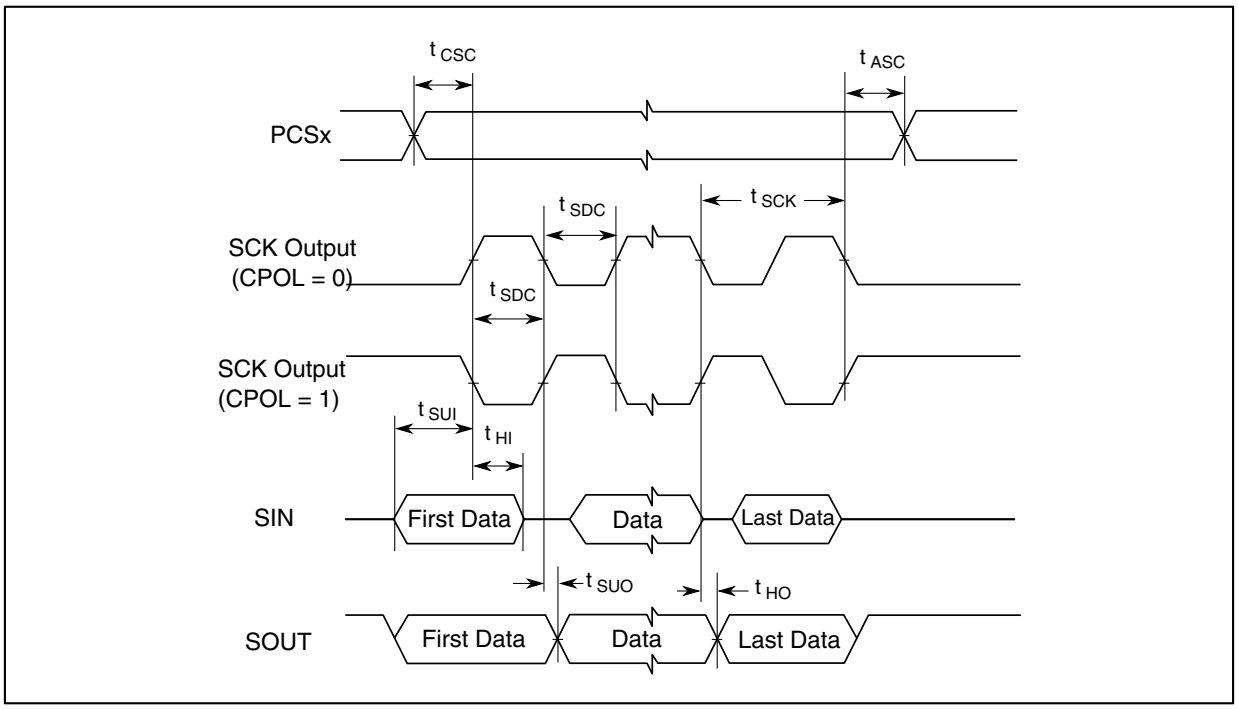


Figure 38. DSPI LVDS master mode – modified timing, CPHA = 0

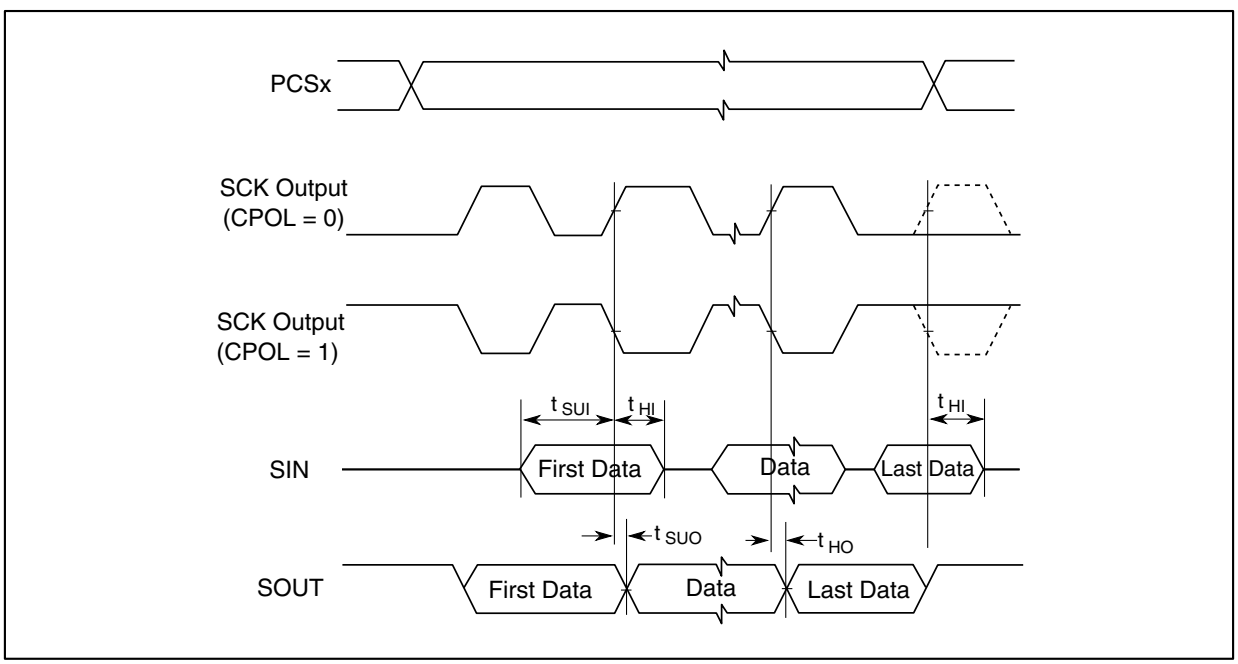


Figure 39. DSPI LVDS master mode – modified timing, CPHA = 1

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 55. Thermal characteristics, 516-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.5	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	20.0	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.5	°C/W
Junction to Board [4]	$R_{\Theta JB}$	8.8	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.1 General notes for thermal characteristics

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component

1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} x P_D)$$

where:

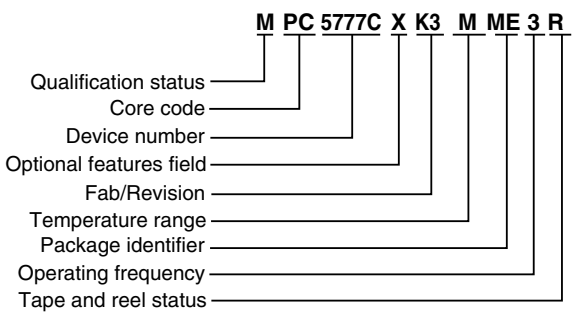
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 47 and Table 56 describe orderable part numbers for the MPC5777C.



Temperature range
M = –40 °C to 125 °C

Operating frequency
3 = 2 x 264 MHz

Package identifier
ME = 416 MAPBGA Pb-Free
MO = 516 MAPBGA Pb-Free

Tape and reel status
R = Tape and reel
(blank) = Trays

Qualification status
P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Optional features field
(blank) = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
A = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
R = ISO-compliant CAN FD not available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
C = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
D = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
L = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
S = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes RSA-enhanced security firmware
T = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes RSA-enhanced security firmware

Note: Not all options are available on all devices.

Figure 47. MPC5777C Orderable part number description

How to Reach Us:

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Web Support:
nxp.com/support

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