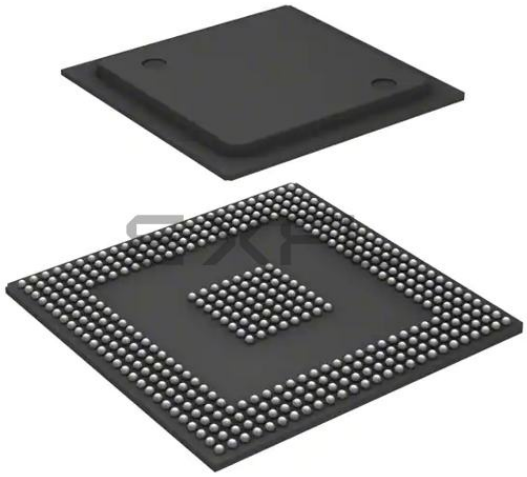

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Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777csk3mme3r

Table of Contents

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability

1.2 Block diagram

The following figure shows a top-level block diagram of the MPC5777C. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch.

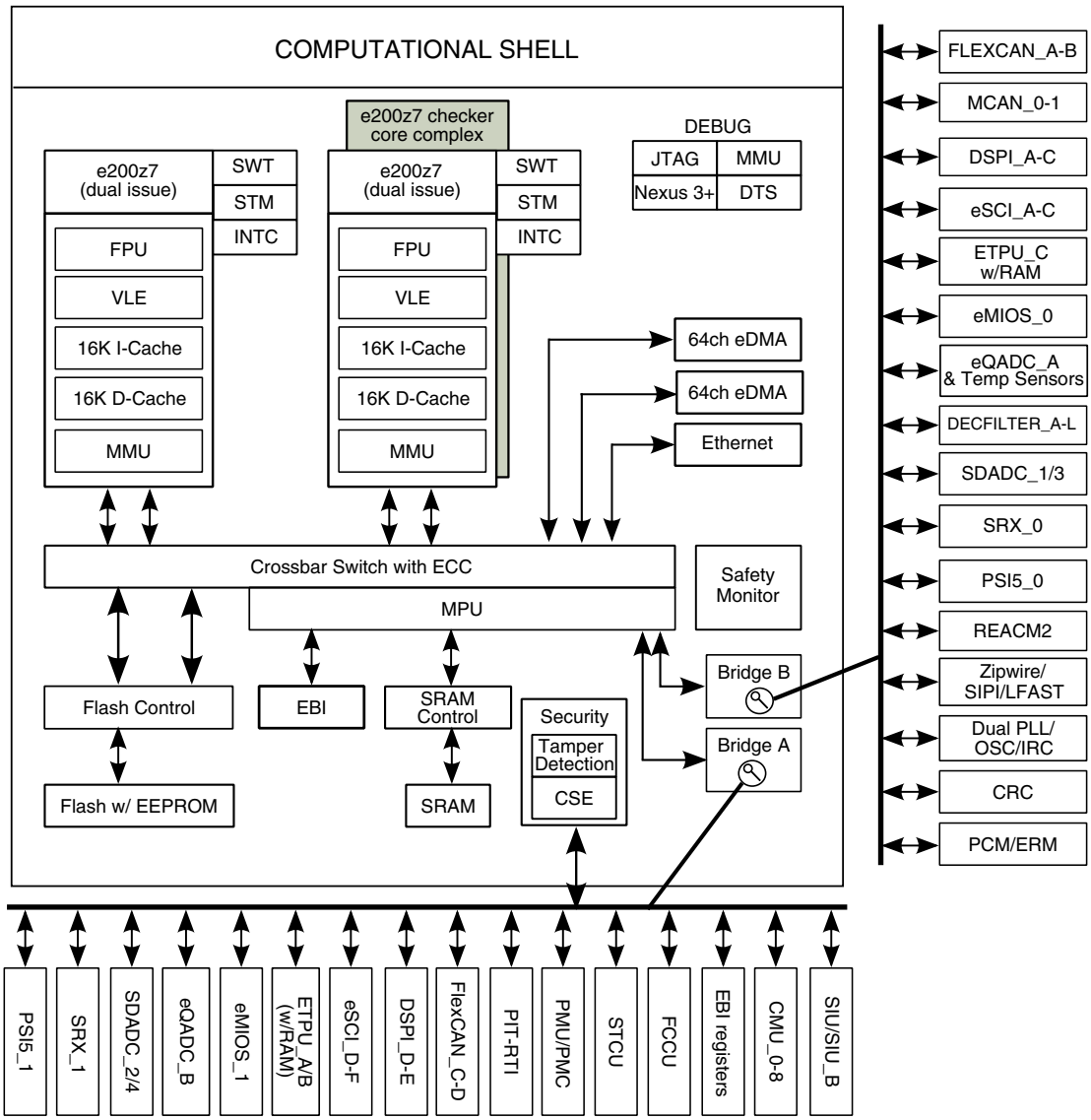


Figure 1. MPC5777C block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
Cycle	Lifetime power cycles	—	—	1000k	—
V_{DD}	1.2 V core supply voltage[2, 3, 4]	—	–0.3	1.5	V
V_{DDEHx}	I/O supply voltage (medium I/O pads)[5]	—	–0.3	6.0	V
V_{DDEx}	I/O supply voltage (fast I/O pads)[5]	—	–0.3	6.0	V
V_{DDPMC}	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
V_{DDFLA}	Decoupling pin for flash regulator[6]	—	–0.3	4.5	V
V_{STBY}	RAM standby supply voltage[5]	—	–0.3	6.0	V
V_{SSA_SD}	SDADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
V_{SSA_EQ}	eQADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	Reference to V_{SSA_EQ}	–0.3	6.0	V
V_{DDA_SD}	SDADC supply voltage	Reference to V_{SSA_SD}	–0.3	6.0	V
V_{RL_SD}	SDADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RL_EQ}	eQADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RH_EQ}	eQADC alternate reference	Reference to V_{RL_EQ}	–0.3	6.0	V
V_{RH_SD}	SDADC alternate reference	Reference to V_{RL_SD}	–0.3	6.0	V
$V_{REFBYPC}$	eQADC reference decoupling capacitor pins	REFBYPCA25, REFBYPCA75, REFBYPCB25, REFBYPC75	–0.3	6.0	V
V_{DDA_MISC}	TRNG and IRC supply voltage	—	–0.3	6.0	V
V_{DDPWR}	SMPS driver supply pin	—	–0.3	6.0	V
V_{SSPWR}	SMPS driver supply pin	Reference to V_{SS}	–0.3	0.3	V
$V_{SS} – V_{SSA\_EQ}$	V_{SSA_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SSA\_SD}$	V_{SSA_SD} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–0.3	0.3	V
V_{IN}	I/O input voltage range[7]	—	–0.3	6.0	V
		Relative to V_{DDEx}/V_{DDEHx}	—	0.3	V
		Relative to V_{SS}	–0.3	—	V
I_{INJD}	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[8, 9]	Maximum current per I/O power segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	Maximum solder temperature[10] Pb-free package	—	—	260	°C

Table continues on the next page...

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

13. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
14. Full device lifetime without performance degradation
15. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
16. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
17. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
18. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

3.5 DC electrical specifications

NOTE

I_{DDA_MISC} is the sum of current consumption of IRC, I_{TRNG}, and I_{STBY} in the 5 V domain. IRC current is provided in the IRC specifications.

NOTE

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

Table 4. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD}	Operating current on the V_{DD} core logic supply[1]	LVD/HVD enabled, V_{DD} = 1.2 V to 1.32 V	—	0.65	1.35	A
		LVD/HVD disabled, V_{DD} = 1.2 V to 1.38 V	—	0.65	1.4	
I_{DD_PE}	Operating current on the V_{DD} supply for flash memory program/erase	—	—	—	85	mA
I_{DDPMC}	Operating current on the V_{DDPMC} supply[2]	Flash memory read	—	—	40	mA
		Flash memory program/erase	—	—	70	
		PMC only	—	—	35	
	Operating current on the V_{DDPMC} supply (internal core regulator bypassed)	Flash memory read	—	—	10	mA
		Flash memory program/erase	—	—	40	
		PMC only	—	—	5	
I_{REGCTL}	Core regulator DC current output on V_{REGCTL} pin	—	—	—	25	mA
I_{STBY}	Standby RAM supply current (T_J = 150°C)	1.08 V	—	—	1140	µA
		1.25 V to 5.5 V	—	—	1170	
I_{DD_PWR}	Operating current on the V_{DDPWR} supply	—	—	—	50	mA
I_{BG_REF}	Bandgap reference current consumption[3]		—	—	600	µA
I_{TRNG}	True Random Number Generator current	—	—	—	2.1	mA

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads
EBI pads	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

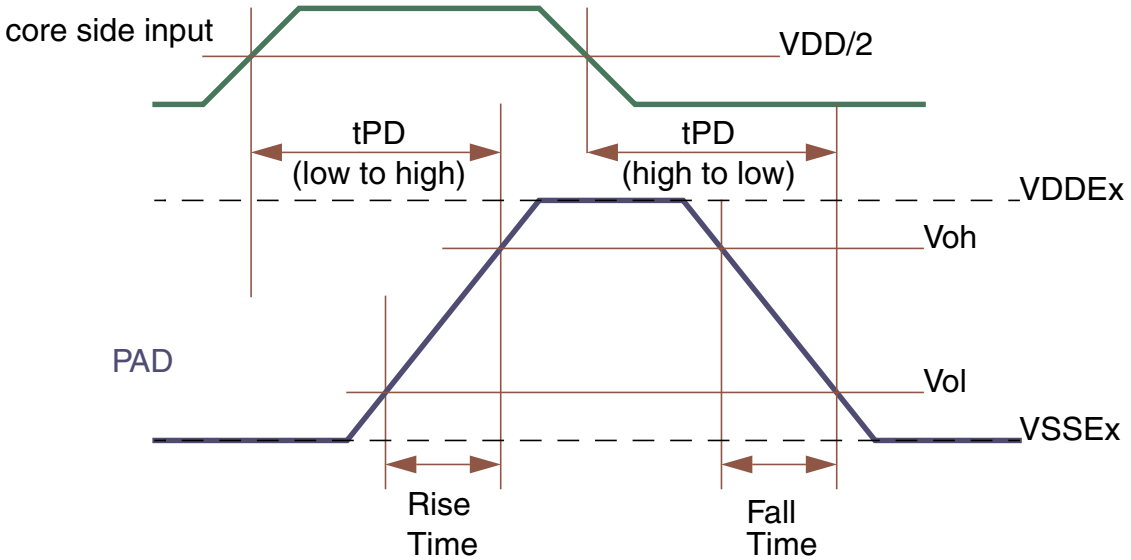


Figure 5. I/O output DC electrical characteristics definition

The following tables specify output DC electrical characteristics.

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1]

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
I_{OH}	GPIO pad output high current	V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	25	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	15	—	—	
		V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	13	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	8	—	—	
I_{OL}	GPIO pad output low current	V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	48	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	22	—	—	
		V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	17	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	10.5	—	—	

Table continues on the next page...

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

Table 13. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL1PHISPJ}\rvert$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[2]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 14 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 14. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	—	V_{REF} – 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.1	2.8	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.2	2.9	
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	

Table continues on the next page...

Table 14. External oscillator (XOSC) electrical specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

1. This value is determined by the crystal manufacturer and board design.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
4. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating in a "low" transconductance range. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating in a "medium" or "high" transconductance range, the integrated load capacitor value is selected via software to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
5. Select a "low," "medium," or "high" setting using the UTEST Miscellaneous DCF client's XOSC_LF_EN and XOSC_EN_HIGH fields. "Low" is the setting commonly used for crystals at 8 MHz, "medium" is commonly used for crystals greater than 8 MHz to 20 MHz, and "high" is commonly used for crystals greater than 20 MHz to 40 MHz. However, the user must characterize carefully to determine the best g_m setting for the intended application because crystal load capacitance, board layout, and other factors affect the g_m value that is needed. The user may need an additional Rshunt to optimize g_m depending on the system environment. Use of overtone crystals is not recommended.
6. Amplitude on the EXTAL pin after startup is determined by the ALC block (that is, the Automatic Level Control Circuit). The function of the ALC is to provide high drive current during oscillator startup, while reducing current after oscillation to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
7. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 7.

Table 15. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
00000	1.8
00001	2.8
00010	3.7
00011	4.6
00100	5.6
00101	6.5
00110	7.4
00111	8.4
01000	9.3
01001	10.2
01010	11.2
01011	12.1
01100	13.0
01101	13.9

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$F_{rolloff}$	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
		[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
		[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
		[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
		[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	
δ_{GROUP}	Group delay	Within pass band: Tclk is f_{ADCD_M} / 2	—	—	—	—
		OSR = 24	—	—	235.5	Tclk
		OSR = 28	—	—	275	
		OSR = 32	—	—	314.5	
		OSR = 36	—	—	354	
		OSR = 40	—	—	393.5	
		OSR = 44	—	—	433	
		OSR = 48	—	—	472.5	
		OSR = 56	—	—	551.5	
		OSR = 64	—	—	630.5	
		OSR = 72	—	—	709.5	
		OSR = 75	—	—	696	
		OSR = 80	—	—	788.5	
		OSR = 88	—	—	867.5	
		OSR = 96	—	—	946.5	
		OSR = 112	—	—	1104.5	
		OSR = 128	—	—	1262.5	
		OSR = 144	—	—	1420.5	
		OSR = 160	—	—	1578.5	
		OSR = 176	—	—	1736.5	
		OSR = 192	—	—	1894.5	
		OSR = 224	—	—	2210.5	
		OSR = 256	—	—	2526.5	
		Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	High pass filter 3 dB frequency	Enabled	—	10e–5* fADCD_S	—	—
$t_{STARTUP}$	Startup time from power down state	—	—	—	100	µs
$t_{LATENCY}$	Latency between input data and converted data when input mux does not change[15]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	δ_{GROUP}	

Table continues on the next page...

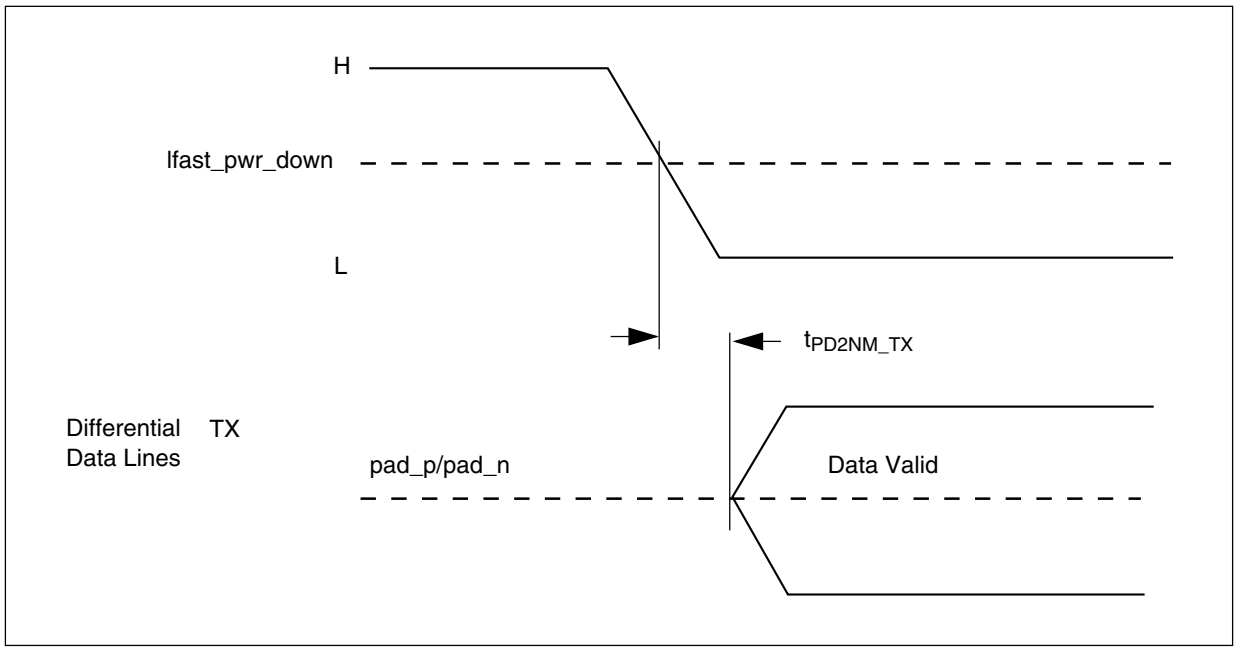


Figure 9. Power-down exit time

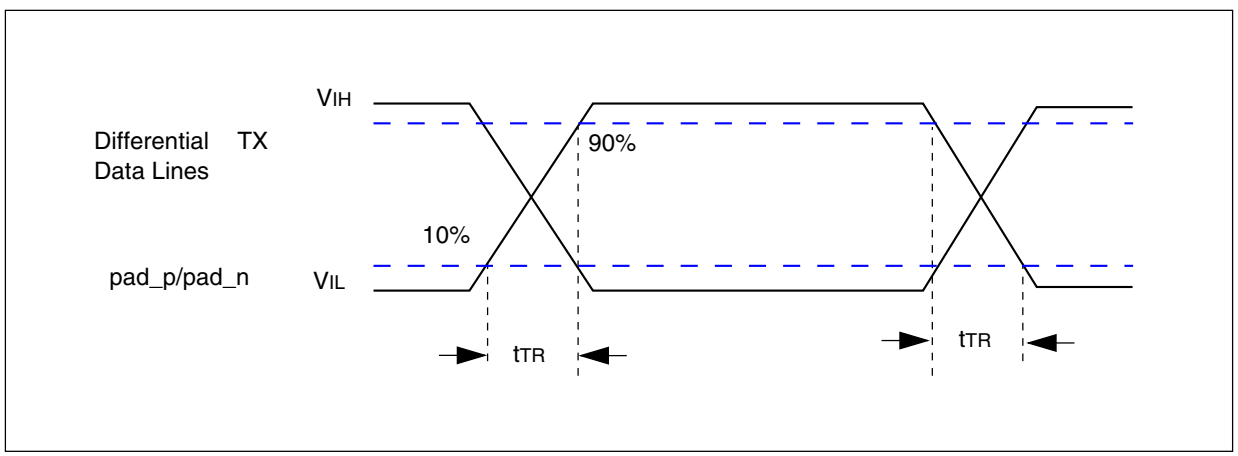


Figure 10. Rise/fall time

3.10.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 20. LVDS pad startup and receiver electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
STARTUP[2,3]						
t_{STRT_BIAS}	Bias current reference startup time[4]	—	—	0.5	4	µs

Table continues on the next page...

The SMPS regulator characteristics appear in the following table.

Table 27. SMPS electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SMPS_{CLOCK}$	SMPS oscillator frequency	Trimmed	825	1000	1220	kHz
$SMPS_{SLOPE}$	SMPS soft-start ramp slope	—	0.01	0.025	0.05	V/µs
$SMPS_{EFF}$	SMPS typical efficiency	—	—	70	—	%

3.11.2 Power management integration

To ensure correct functionality of the device, use the following recommended integration scheme for LDO mode.

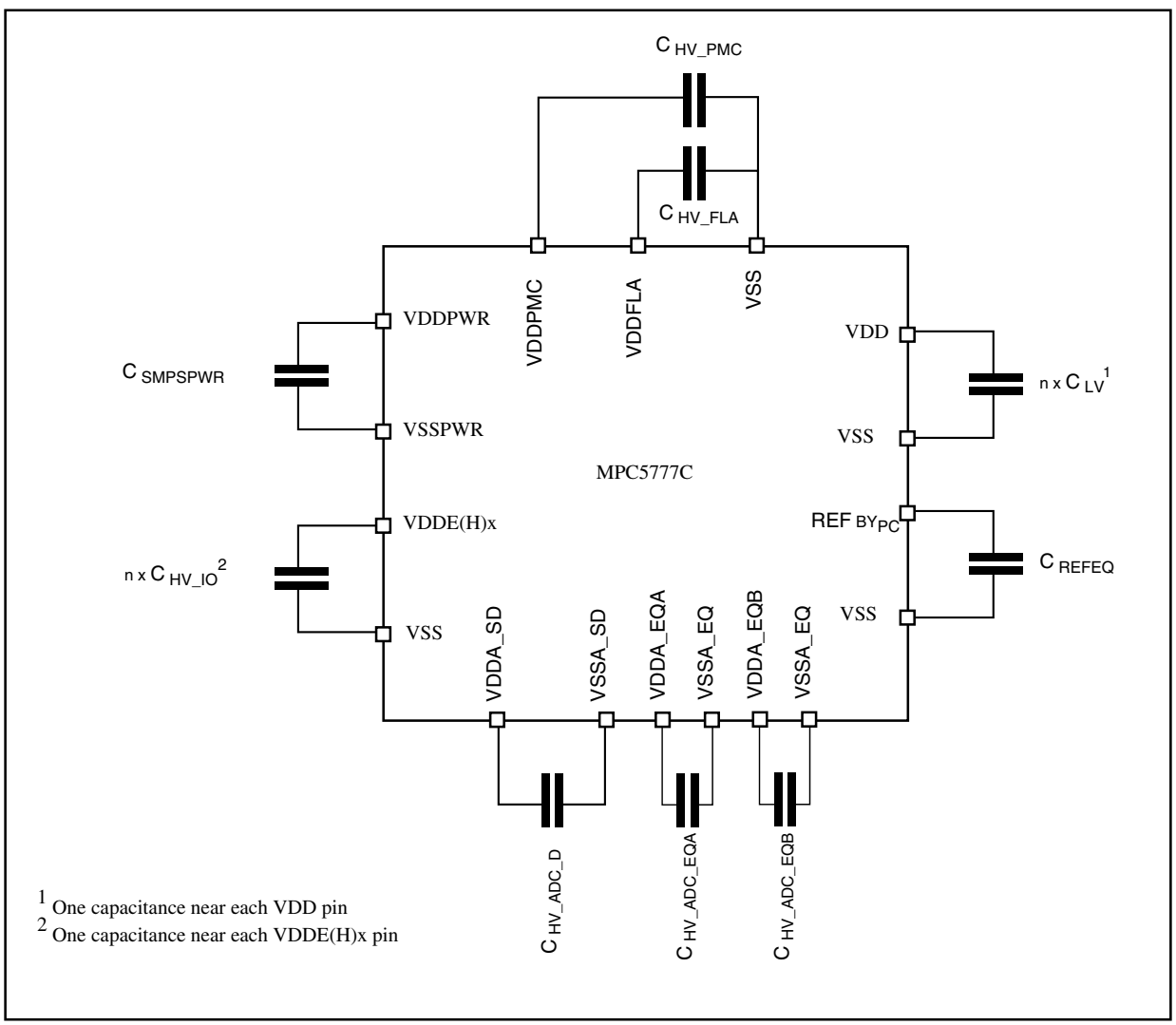


Figure 14. Recommended supply pin circuits

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
   - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

   During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

   During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

3.12.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units [2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.12.3 Flash memory module life specifications

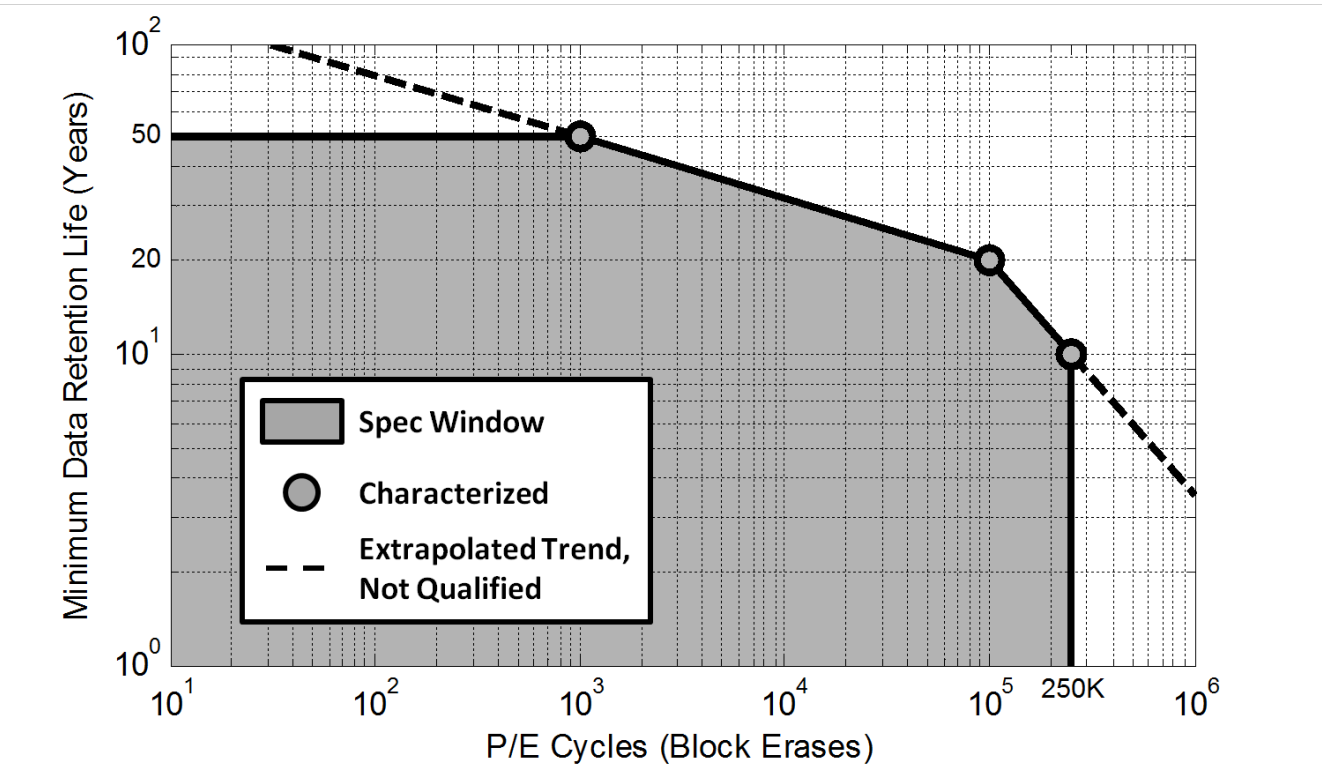
Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

3.12.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.12.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns

Table continues on the next page...

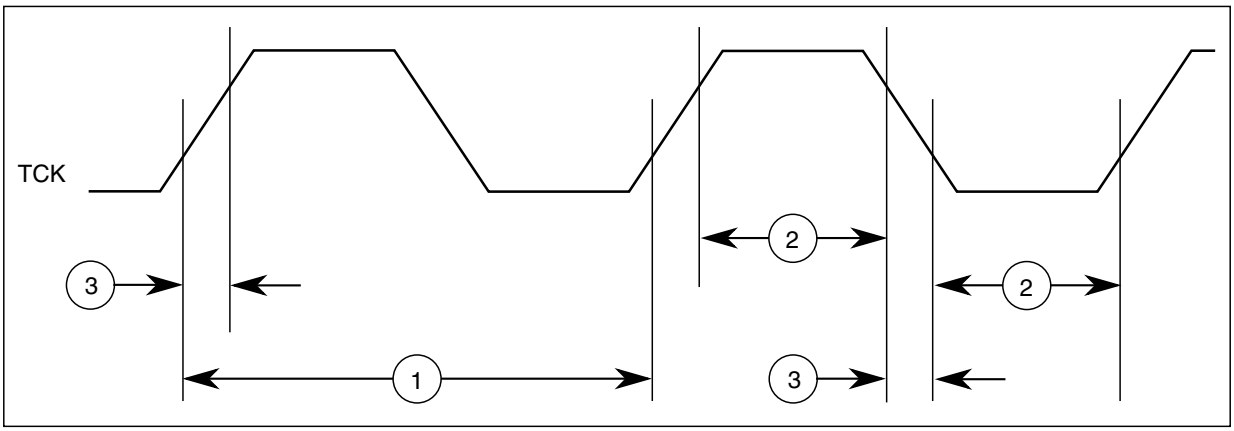


Figure 19. JTAG test clock input timing

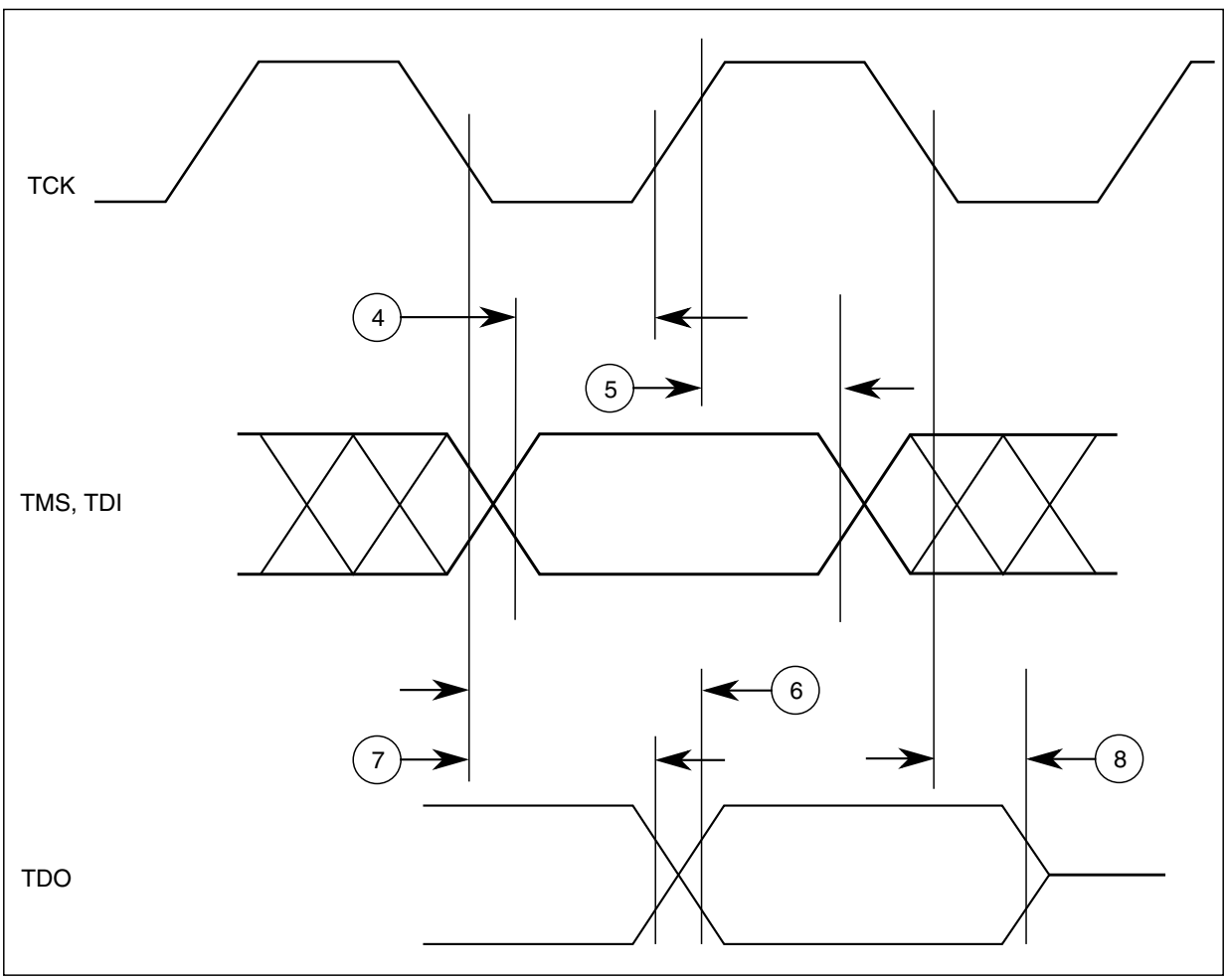


Figure 20. JTAG test access port timing

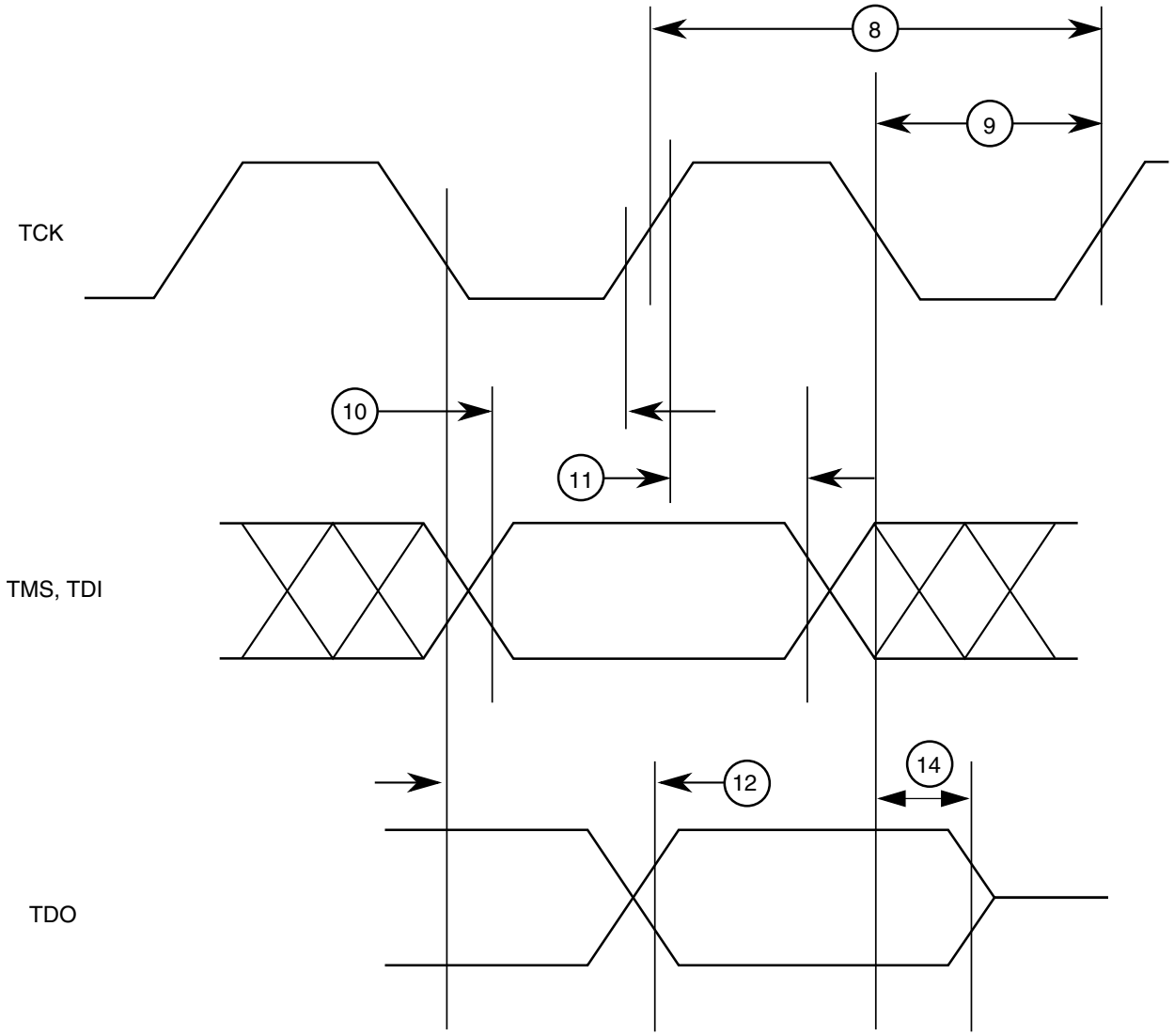


Figure 24. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External Bus Interface (EBI) timing

Table 38. Bus operation timing[1]

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	—
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	—
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	—

Table continues on the next page...

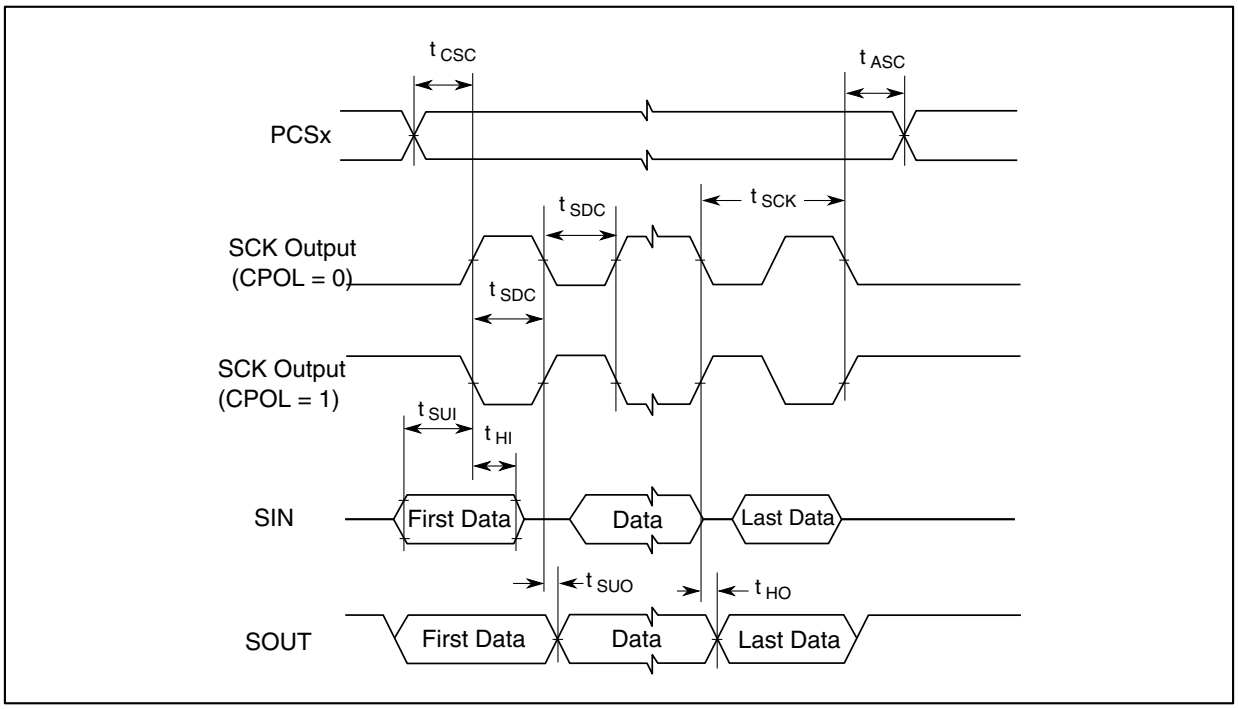


Figure 35. DSPI CMOS master mode – modified timing, CPHA = 0

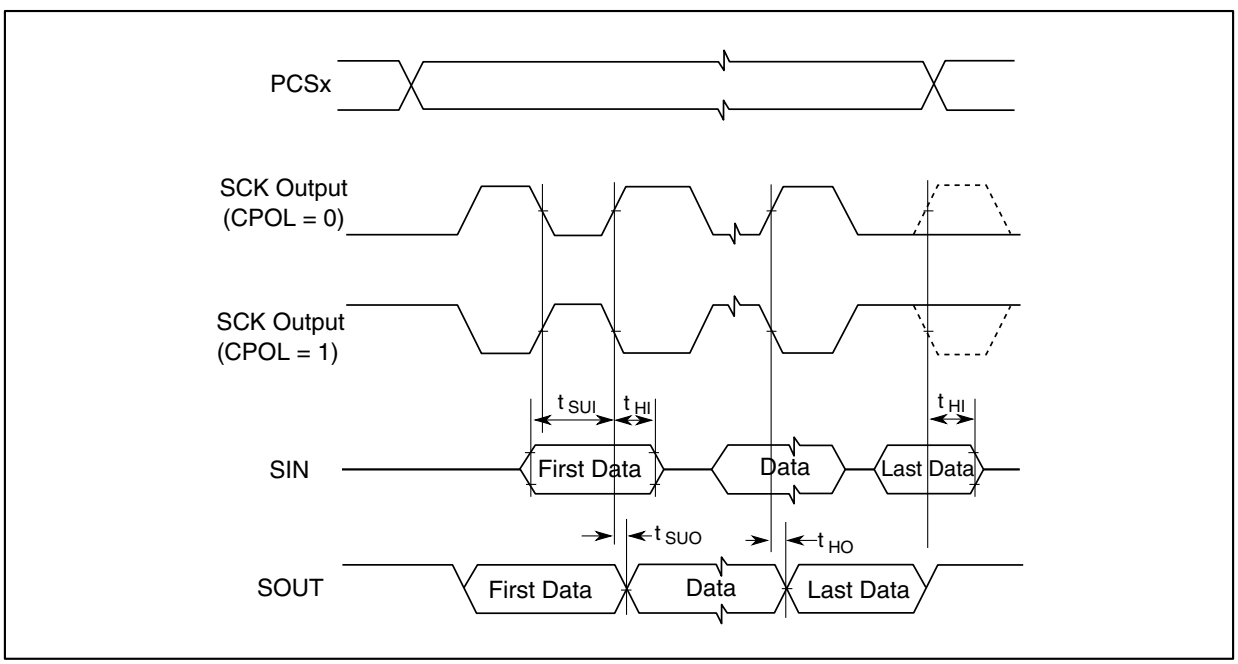


Figure 36. DSPI CMOS master mode – modified timing, CPHA = 1