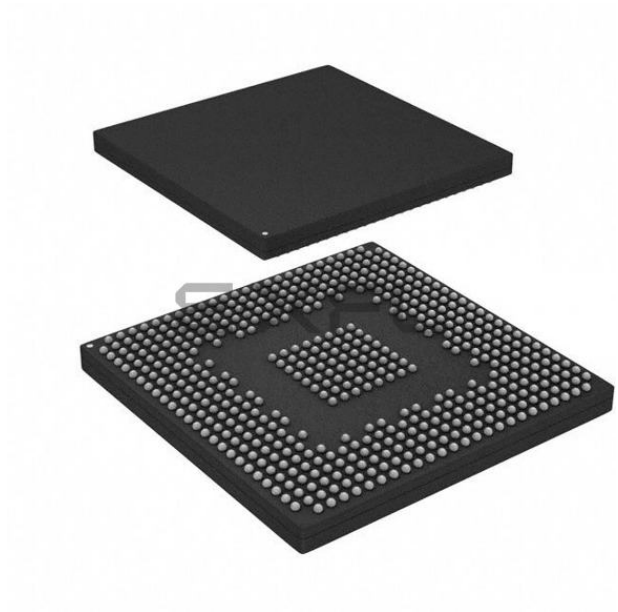

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777csk3mmo3

1.2 Block diagram

The following figure shows a top-level block diagram of the MPC5777C. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch.

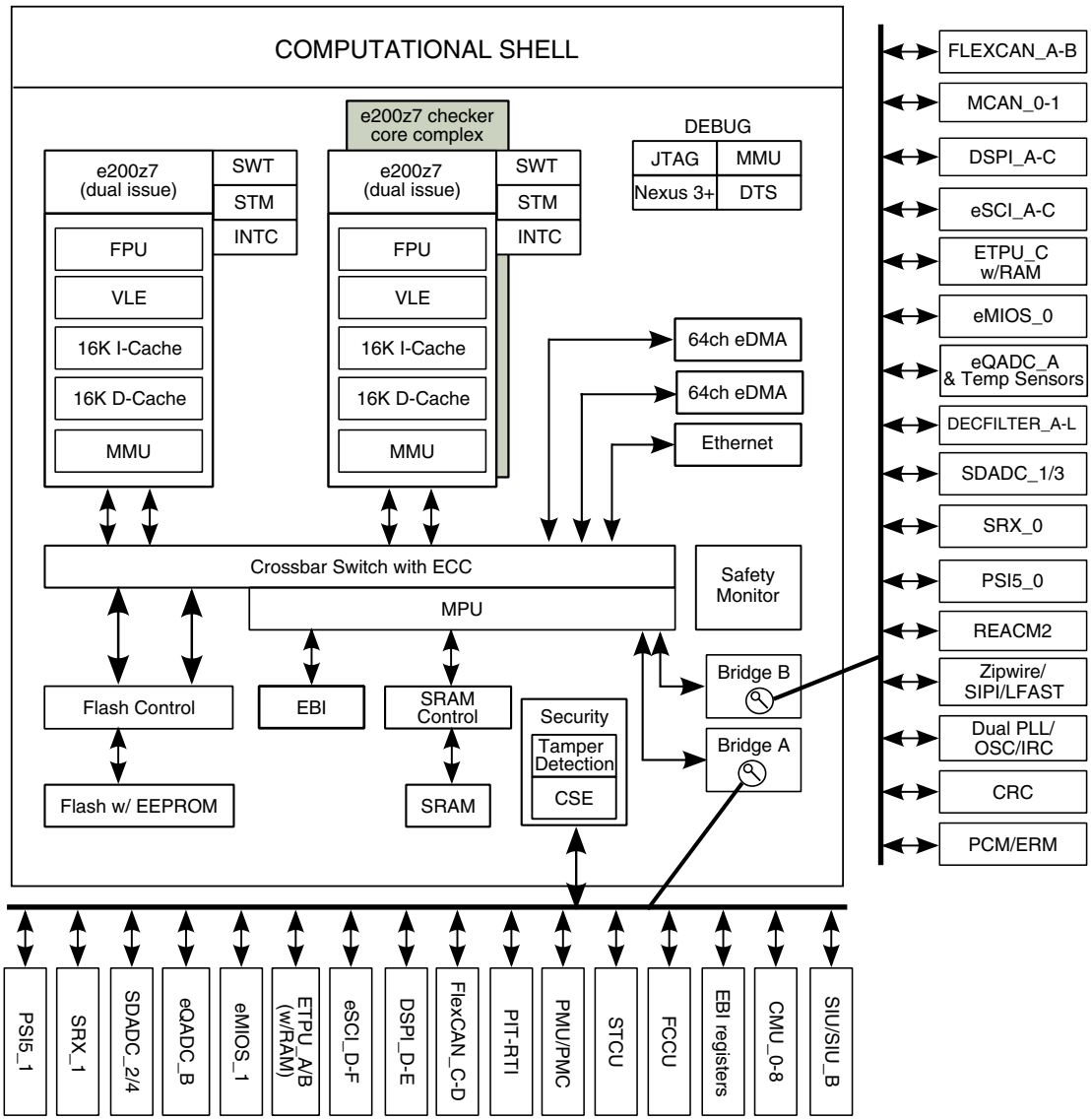


Figure 1. MPC5777C block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

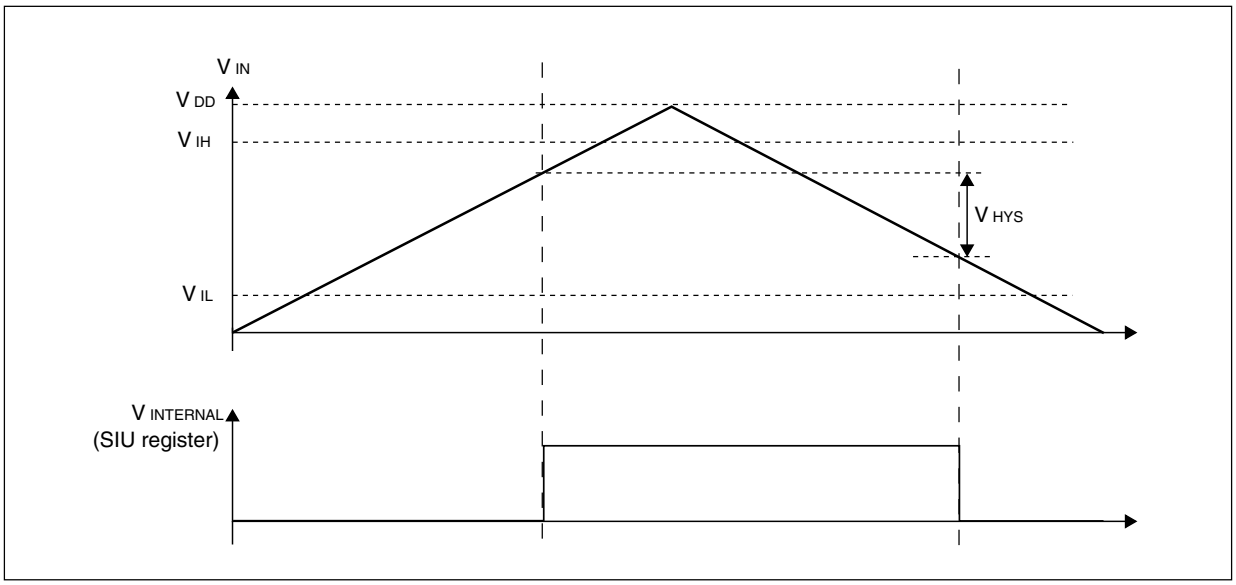


Figure 4. I/O input DC electrical characteristics definition

Table 6. I/O input DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IHCMOS_H}	Input high level CMOS (with hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.65 * V_{DDEx}	—	V_{DDEx} + 0.3	V
V_{IHCMOS}	Input high level CMOS (without hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.55 * V_{DDEx}	—	V_{DDEx} + 0.3	V
V_{ILCMOS_H}	Input low level CMOS (with hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	–0.3	—	0.35 * V_{DDEx}	V
V_{ILCMOS}	Input low level CMOS (without hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	–0.3	—	0.4 * V_{DDEx}	V
$V_{HYSCMOS}$	Input hysteresis CMOS	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.1 * V_{DDEx}	—	—	V
Input Characteristics[1]						
I_{LKG}	Digital input leakage	V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}	—	—	2.5	µA
I_{LKG_FAST}	Digital input leakage for EBI address/control signal pads	V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}	—	—	2.5	µA
I_{LKGA}	Analog pin input leakage (5 V range)	V_{SSA_SD} < V_{IN} < V_{DDA_SD}, V_{SSA_EQ} < V_{IN} < $V_{DDA\_EQA/B}$	—	—	220	nA
C_{IN}	Digital input capacitance	GPIO and EBI input pins	—	—	7	pF

1. For LFAST, microsecond bus, and LVDS input characteristics, see dedicated communication module sections.

Table 7 provides current specifications for weak pullup and pulldown.

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1] (continued)

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
t_{R_F}	GPIO pad output transition time (rise/fall)	PCR[SRC] = 11b	C_L = 25 pF	—	—	1.2	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	2.5	
			C_L = 200 pF	—	—	8	
		PCR[SRC] = 11b	C_L = 25 pF	—	—	1.7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	3.25	
			C_L = 200 pF	—	—	12	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	5	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	18	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	25	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	13	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	24	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	30	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	24	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	50	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	51	
t_{PD}	GPIO pad output propagation delay time	PCR[SRC] = 11b	C_L = 50 pF	—	—	6	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	13	
		PCR[SRC] = 11b	C_L = 50 pF	—	—	8.25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	19.5	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	9	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	22	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	12.5	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	35	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	27	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	40	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	45	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	75	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	100	
$\lvert t_{SKEW\_W} \rvert$	Difference between rise and fall time	—		—	—	25	%

1. All GPIO pad output specifications are valid for 3.0 V < V_{DDEx} < 5.5 V, except where explicitly stated.

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

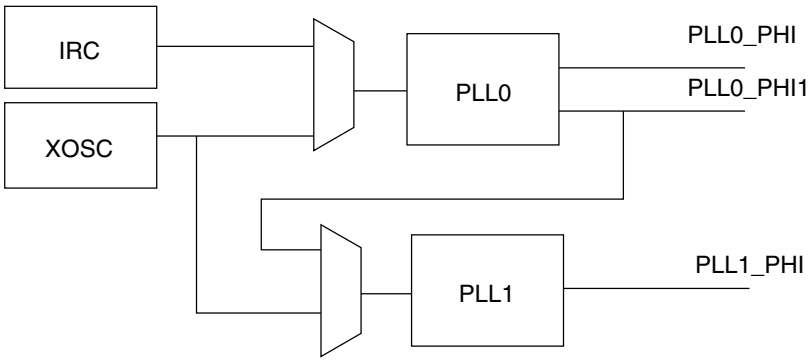


Figure 6. PLL integration

3.7.1 PLL electrical specifications

Table 12. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1, 2]	—	8	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	PLL0 output frequency	—	4.762	—	200	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 200 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[3]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	7.5	mA

1. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz to 20 MHz.
2. PLL0IN clock retrieved directly from either internal IRC or external XOSC clock. Input characteristics are granted when using internal IRC or external oscillator is used in functional mode.
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

5. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.
6. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
7. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.
8. Condition applies to two adjacent pins at injection limits.
9. Performance expected with production silicon.
10. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.
11. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
12. TUE does not apply to differential conversions.
13. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
14. Guaranteed 10-bit monotonicity.
15. At $V_{RH\_EQ} - V_{RL\_EQ} = 5.12$ V, one LSB = 1.25 mV.

3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

NOTE

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

Table 18. SDADC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	V_{DDA_SD}	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended $V_{INM} = V_{RL\_SD}$	V_{RH_SD}/GAIN			V
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 1	±0.5*V_{RH_SD}			
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 2,4,8,16	±V_{RH_SD}/GAIN			
		Differential $0 < V_{IN} < V_{DDEx}$	±V_{RH_SD}/GAIN			
f_{ADCD_M}	SD clock frequency[4]	—	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	—	—	—	333	Ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	SD register resolution[5]	2's complement notation	16			bit

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	80	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	77	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	74	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	71	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	71	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	70	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	68	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	65	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	62	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	72	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	69	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	66	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	62	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
THD_{SE150}	Total harmonic distortion in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
SFDR	Spurious free dynamic range	Any GAIN	60	—	—	dB
Z_{DIFF}	Differential input impedance[10, 11]	GAIN = 1	1000	1250	1500	kΩ
		GAIN = 2	600	800	1000	
		GAIN = 4	300	400	500	
		GAIN = 8	200	250	300	
		GAIN = 16	200	250	300	
Z_{CM}	Common Mode input impedance[11, 12]	GAIN = 1	1400	1800	2200	kΩ
		GAIN = 2	1000	1300	1600	
		GAIN = 4	700	950	1150	
		GAIN = 8	500	650	800	
		GAIN = 16	500	650	800	
R_{BIAS}	Bare bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	Common Mode input reference voltage[13]	—	–12	—	+12	%
V_{BIAS}	Bias voltage	—	—	$V_{RH\_SD}/2$	—	V
δV_{BIAS}	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	Common mode rejection ratio	—	20	—	—	dB
R_{Caaf}	Anti-aliasing filter	External series resistance	—	—	20	kΩ
		Filter capacitances	220	—	—	pF
$f_{PASSBAND}$	Pass band[9]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	Pass band ripple[14]	0.333 * f_{ADCD_S}	–1	—	1	%

Table continues on the next page...

Table 21. LFAST transmitter electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	110	200	285	mV
t_{TR}	Rise/fall time (10% – 90% of swing)[2,3]	—	0.26	—	1.5	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	12.0	pF
		V_{DDE} = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst-case internal capacitance values shown in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load CL.

Table 22. MSC/DSPI LVDS transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing)[2,3]	—	0.8	—	4.0	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	50	pF
		V_{DDE} = 3.0 V	—	—	39	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst-case internal capacitance values given in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load C_L.

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

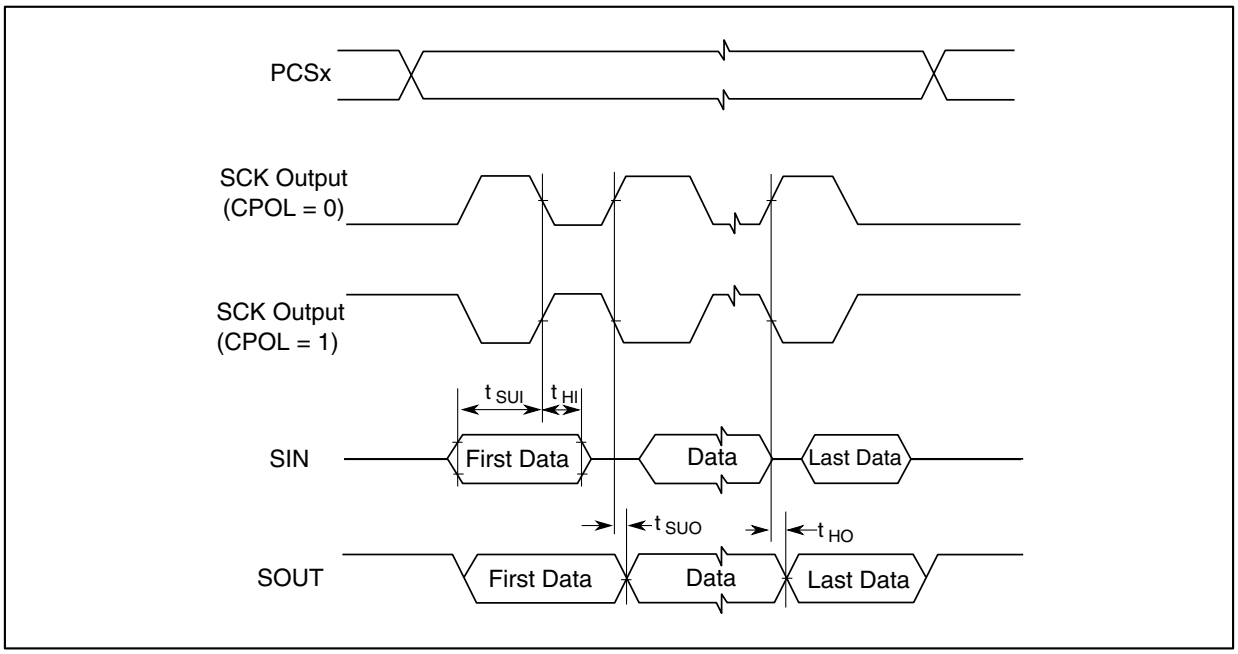


Figure 33. DSPI CMOS master mode – classic timing, CPHA = 1

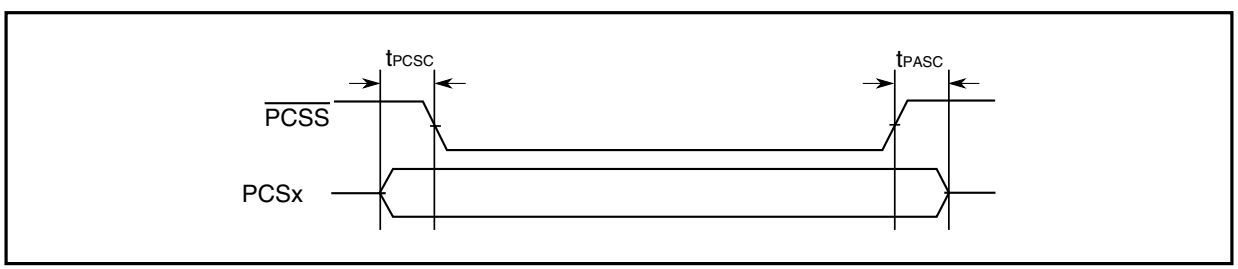


Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.2 DSPI CMOS Master Mode – Modified Timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} – 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

Table continues on the next page...

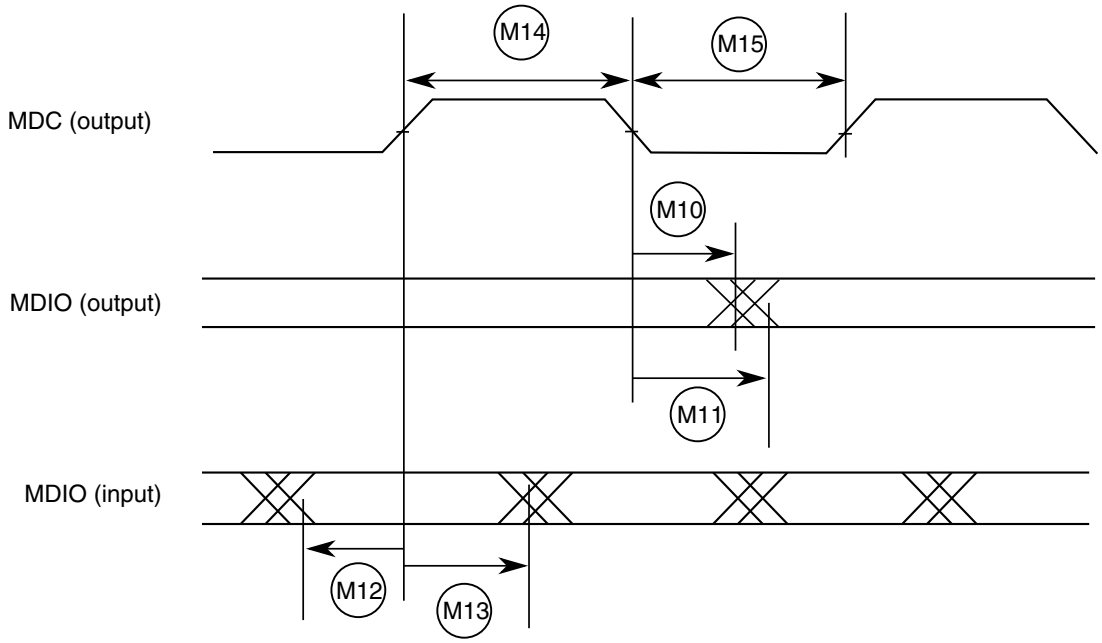


Figure 44. MII serial management channel timing diagram

3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 52. RMII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.

1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} x P_D)$$

where:

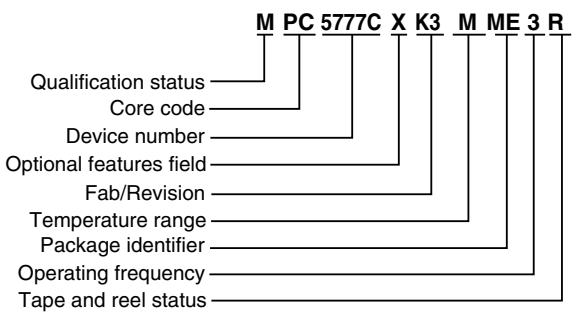
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 47 and Table 56 describe orderable part numbers for the MPC5777C.



Temperature range
M = –40 °C to 125 °C

Operating frequency
3 = 2 x 264 MHz

Package identifier
ME = 416 MAPBGA Pb-Free
MO = 516 MAPBGA Pb-Free

Tape and reel status
R = Tape and reel
(blank) = Trays

Qualification status
P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Optional features field
(blank) = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
A = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
R = ISO-compliant CAN FD not available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
C = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
D = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
L = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
S = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes RSA-enhanced security firmware
T = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes RSA-enhanced security firmware

Note: Not all options are available on all devices.

Figure 47. MPC5777C Orderable part number description

Table 56. Example orderable part numbers

Part number[1]	Package description	Speed (MHz)[2]	Operating temperature[3]	
			Min (T_L)	Max (T_H)
SPC5777CCK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 57. Revision history

Revision	Date	Description of changes
11	04/2017	In Figure 47 of Ordering information, added codes and firmware version information in definition of "Optional features field" • At end of line for *(blank)*, added "version 2.07" • Added line for *A* • At end of line for *R*, added "version 2.08" • At end of line for *C*, added "version 2.07" • Added line for *D* • At end of line for *L*, added "version 2.08"