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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga108-e-pt

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Special Microcontroller Features:

- Operating Voltage Range of 2.0V to 3.6V
- Self-Reprogrammable under Software Control
- 5.5V Tolerant Input (digital pins only)
- Configurable Open-Drain Outputs on Digital I/O
- High-Current Sink/Source (18 mA/18 mA) on all I/O
- Selectable Power Management modes:
 Sloop, Idle and Daza modes with fast works up
- Sleep, Idle and Doze modes with fast wake-upFail-Safe Clock Monitor Operation:
 - Detects clock failure and switches to on-chip FRC oscillator
- On-Chip LDO Regulator

- Power-on Reset (POR), Power-up Timer (PWRT), Low-Voltage Detect (LVD) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with On-Chip Low-Power RC Oscillator for Reliable Operation
- In-Circuit Serial Programming[™] (ICSP[™]) and In-Circuit Debug (ICD) via 2 Pins
- JTAG Boundary Scan Support
- Brown-out Reset (BOR)
- Flash Program Memory:
 - 10,000 erase/write cycle endurance (minimum)
 - 20-year data retention minimum
 - Selectable write protection boundary
 - Write protection option for Flash Configuration Words

Pin Diagram (64-Pin TQFP and QFN⁽¹⁾)



Pin Diagram (100-Pin TQFP)



		Pin Number				
Function	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP	VO	Input Buffer	Description
CN43		52	66	I	ST	Interrupt-on-Change Inputs.
CN44	_	53	67	I	ST	
CN45	_	4	6	I	ST	
CN46	_	_	7	I	ST	
CN47	_	5	8	I	ST	
CN48	-	_	9	Ι	ST	
CN49	46	58	72	Ι	ST	
CN50	49	61	76	I	ST	
CN51	50	62	77	Ι	ST	
CN52	51	63	78	Ι	ST	
CN53	42	54	68	Ι	ST	
CN54	43	55	69	I	ST	
CN55	44	56	70	I	ST	
CN56	45	57	71	I	ST	
CN57	_	64	79	I	ST	
CN58	60	76	93	I	ST	
CN59	61	77	94	I	ST	
CN60	62	78	98	I	ST	
CN61	63	79	99	I	ST	
CN62	64	80	100	I	ST	
CN63	1	1	3	Ι	ST	
CN64	2	2	4	Ι	ST	
CN65	3	3	5	Ι	ST	
CN66	_	13	18	I	ST	
CN67	_	14	19	I	ST	
CN68	58	72	87	I	ST	
CN69	59	73	88	I	ST	
CN70	34	42	52	I	ST	
CN71	33	41	51	I	ST	
CN72	35	45	55	I	ST	
CN73	—	44	54	I	ST	
CN74	_	43	53	I	ST	
CN75	—	—	40	I	ST	
CN76	—	_	39	I	ST	
CN77	—	75	90	I	ST	
CN78	—	74	89		ST	
CN79	—	—	96		ST	
CN80	—	—	97		ST	
CN81	—	—	95		ST	
CN82		—	1		ST	
CN83	37	47	57		ST	
CN84	36	46	56	I	ST	

TABLE 1-4: PIC24FJ256GA110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Legend:

TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer $I^2C^{TM} = I^2C/SMBus$ input buffer

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3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 1. 16-bit x 16-bit signed
- 2. 16-bit x 16-bit unsigned
- 3. 16-bit signed x 5-bit (literal) unsigned
- 4. 16-bit unsigned x 16-bit unsigned
- 5. 16-bit unsigned x 5-bit (literal) unsigned
- 6. 16-bit unsigned x 16-bit signed
- 7. 8-bit unsigned x 8-bit unsigned

3.3.2 DIVIDER

The divide block supports signed and unsigned integer divide operations with the following data sizes:

- 1. 32-bit signed/16-bit signed divide
- 2. 32-bit unsigned/16-bit unsigned divide
- 3. 16-bit signed/16-bit signed divide
- 4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn), and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.3.3 MULTI-BIT SHIFT SUPPORT

The PIC24F ALU supports both single bit and single-cycle, multi-bit arithmetic and logic shifts. Multi-bit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multi-bit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided below in Table 3-2.

TABLE 3-2: INSTRUCTIONS THAT USE THE SINGLE AND MULTI-BIT SHIFT OPERATION

Instruction Description							
ASR	Arithmetic shift right source register by one or more bits.						
SL	Shift left source register by one or more bits.						
LSR	Logical shift right source register by one or more bits.						

TABLE 4-22: PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	0600	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP	0000
PMMODE	0602	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000
PMADDR	0604	CS2	CS1	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	0000
PMDOUT1							Pa	arallel Port D	ata Out Reg	gister 1 (Buf	fers 0 and 1)						0000
PMDOUT2	0606						Pa	arallel Port D	ata Out Reg	gister 2 (Buf	fers 2 and 3)						0000
PMDIN1	0608						P	arallel Port I	Data In Regi	ister 1 (Buffe	ers 0 and 1)							0000
PMDIN2	060A						P	arallel Port I	Data In Regi	ister 2 (Buffe	ers 2 and 3)							0000
PMAEN	060C	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMSTAT	060E	IBF	IBOV		_	IB3F	IB2F	IB1F	IB0F	OBE	OBUF		_	OB3E	OB2E	OB1E	OB0E	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620						Alarm	Value Registe	er Window Bas	ed on ALR	MPTR<1:0>							xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	0624						RTC	C Value Regis	ter Window Ba	sed on RT	CPTR<1:0>							xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	xxxx
Lanandi						a la la sua da s	ine al											

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: COMPARATORS REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0630	CMIDL	—			—	C3EVT	C2EVT	C1EVT						C3OUT	C2OUT	C10UT	0000
CVRCON	0632	—	—	—	—	_	_	—	_	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	0634	CEN	COE	CPOL	—	_	_	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	_	CCH1	CCH0	0000
CM2CON	0636	CEN	COE	CPOL	—	_	_	CEVT	COUT	EVPOL1	EVPOL0	_	CREF	_	_	CCH1	CCH0	0000
CM3CON	0638	CEN	COE	CPOL		_	_	CEVT	COUT	EVPOL1	EVPOL0		CREF	-	_	CCH1	CCH0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: CRC REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON	0640	—	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0	CRCFUL	CRCMPT		CRCGO	PLEN3	PLEN2	PLEN1	PLEN0	0040
CRCXOR	0642	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	_	0000
CRCDAT	0644		CRC Data Input Register 000										0000					
CRCWDAT	0646								CRC Resi	ult Register								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/SO-0 ⁽	¹⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15		- -					bit 8
U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	ERASE	—		NVMOP3 ⁽²⁾	NVMOP2 ⁽²⁾	NVMOP1 ⁽²⁾	NVMOP0 ⁽²⁾
bit 7							bit 0
Legend:		SO = Set Onl	y bit				
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 15	WR: Write Co	ontrol bit ⁽¹⁾					
	1 = Initiates a	a Flash memoi	ry program or	erase operatior	n. The operation	on is self-timed	and the bit is
	Cleared b	or erase opera	ce the operation	on is complete.			
hit 14	WREN. Write	Enable bit ⁽¹⁾					
Sit 11	1 = Enable F	lash program/e	erase operation	IS			
	0 = Inhibit Fla	ash program/er	ase operations	6			
bit 13	WRERR: Writ	te Sequence E	rror Flag bit ⁽¹⁾				
	1 = An impro	oper program	or erase seq	uence attempt	or terminatio	on has occurre	ed (bit is set
	automatio	cally on any se	t attempt of the	e WR bit)			
bit 12_7		ted: Read as '	n'	leted normally			
bit 6	ERASE: Eras	e/Program En:	∪ ahle hit(1)				
bit 0	1 = Perform f	the erase oper	ation specified)> on the next '	WR command	
	0 = Perform	the program op	eration specifie	ed by NVMOP<	3:0> on the ne	ext WR comman	nd
bit 5-4	Unimplemen	ted: Read as '	0'				
bit 3-0	NVMOP<3:0>	-: NVM Operat	ion Select bits(1,2)			
	1111 = Mem o	ory bulk erase o	operation (ERA	SE = 1) or no o	operation (ERA	SE = 0) ⁽³⁾	
	0011 = Memo	ory word progra	am operation (E	ERASE = 0 or $ASE = 1$ or $BRASE = 1$	no operation (E	ERASE = 1)	
	0010 = Memory 0001 = Memory 00001 = Memory 000000000000000000000000000000000000	ory page erase	n operation (ER	ASE = 1) of no RASE = 0) or n	operation (ER	ASE = 0	
	-						
Note 1:	These bits can or	ily be reset on	POR.				
2:	All other combina	tions of NVMO	P<3:0> are un	implemented.			

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

3: Available in ICSP[™] mode only. Refer to the device programming specification.

5.6.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time. To do this, it is necessary to erase the 8-row erase block containing the desired row. The general process is as follows:

- 1. Read eight rows of program memory (512 instructions) and store in data RAM.
- 2. Update the program data in RAM with the desired new data.
- 3. Erase the block (see Example 5-1 for an implementation in assembler):
 - a) Set the NVMOP bits (NVMCON<3:0>) to ⁽⁰⁰¹⁰⁾ to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
 - b) Write the starting address of the block to be erased into the TBLPAG and W registers.
 - c) Write 55h to NVMKEY.
 - d) Write AAh to NVMKEY.
 - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
- 4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-3 for the implementation in assembler).

- 5. Write the program block to Flash memory:
 - a) Set the NVMOP bits to '0001' to configure for row programming. Clear the ERASE bit and set the WREN bit.
 - b) Write 55h to NVMKEY.
 - c) Write AAh to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
- 6. Repeat Steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as shown in Example 5-5.

Note: The equivalent C code for these steps, prepared using Microchip's MPLAB C30 compiler and a specific library of built-in hardware functions, is shown in Examples 5-2, 5-4 and 5-6.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY BLOCK (ASSEMBLY LANGUAGE CODE)

; Set up NVMCO	N for block erase operation		
MOV	#0x4042, W0	;	
MOV	W0, NVMCON	;	Initialize NVMCON
; Init pointer	to row to be ERASED		
MOV	<pre>#tblpage(PROG_ADDR), W0</pre>	;	
MOV	W0, TBLPAG	;	Initialize PM Page Boundary SFR
MOV	<pre>#tbloffset(PROG_ADDR), W0</pre>	;	Initialize in-page EA[15:0] pointer
TBLWTL	W0, [W0]	;	Set base address of erase block
DISI	#5	;	Block all interrupts with priority <7
		;	for next 5 instructions
MOV	#0x55, W0		
MOV	W0, NVMKEY	;	Write the 55 key
MOV	#0xAA, W1	;	
MOV	W1, NVMKEY	;	Write the AA key
BSET	NVMCON, #WR	;	Start the erase sequence
NOP		;	Insert two NOPs after the erase
NOP		;	command is asserted

7.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the "PIC24F Family Reference Manual", Section 8. "Interrupts" (DS39707).

The PIC24F interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24F CPU. It has the following features:

- Up to 8 processor exceptions and software traps
- 7 user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors, consisting of 8 non-maskable trap vectors, plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address.

PIC24FJ256GA110 family devices implement non-maskable traps and unique interrupts. These are summarized in Table 7-1 and Table 7-2.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports emulation and debugging efforts by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24F devices clear their registers in response to a Reset which forces the PC to zero. The micro-controller then begins program execution at location 000000h. The user programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-21:	IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4
----------------	--

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	CNIP2	CNIP1	CNIP0	_	CMIP2	CMIP1	CMIP0
bit 15					I		bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	MI2C1IP2	MI2C1IP1	MI2C1IP0	<u> </u>	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
6:4 <i>4 C</i>		tad. Deed as '	、 ,				
		ted: Read as () atification later	www.undt Duinewider, bit	-		
DIT 14-12	111 - Intorru	nput Change N	ouncation inter	interrupt)	5		
	•		lighest phonty	interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1 pt source is dis:	abled				
bit 11	Unimplemen	ted: Read as ')'				
bit 10-8	CMIP<2:0>: (Comparator Inte	errupt Priority b	oits			
	111 = Interru	, pt is priority 7 (ł	nighest priority	interrupt)			
	•						
	•						
	• 001 = Interru	ot is priority 1					
	000 = Interru	pt source is disa	abled				
bit 7	Unimplemen	ted: Read as 'd)'				
bit 6-4	MI2C1IP<2:0	>: Master I2C1	Event Interrup	t Priority bits			
	111 = Interru	pt is priority 7 (ł	nighest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				
bit 3	Unimplemen	ted: Read as '0)'				
bit 2-0	SI2C1IP<2:0	Slave I2C1 E	vent Interrupt	Priority bits			
	111 = Interru	pt is priority 7 (ł	nighest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				

REGISTER	8-4: REF	OCON: REFE		ILLATOR CO	NTROL REG	SISTER	
R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN		ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—				—	—	—
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 14	1 = Reference 0 = Reference Unimpleme	ce oscillator ena ce oscillator disa nted: Read as 'i	bled on REFO	pin			
		oforonoo Oppilla	tor Output Sto	n in Sloon hit			
DIL 13	1 = Reference 0 = Reference	ce oscillator con ce oscillator is di	tinues to run ir sabled in Slee	p in Sleep bit Sleep p			
bit 12	ROSEL: Rei	ference Oscillato	or Source Sele	ct bit			
	1 = Primary the FOS 0 = System	Oscillator used SC<2:0> bits; cry clock used as th	as the base c stal maintains he base clock;	lock. Note that the operation in base clock refle	the crystal osc n Sleep mode. ects any clock s	sillator must be switching of the	enabled using e device
bit 11-8	RODIV<3:0:	>: Reference Os	cillator Divisor	Select bits			
	1111 = Base 1110 = Base 1101 = Base 1001 = Base 1011 = Base 1001 = Base 0111 = Base 0111 = Base 0110 = Base 0101 = Base 0011 = Base 0011 = Base 0011 = Base 0011 = Base 0011 = Base	e clock value div e clock value div	ided by 32,768 ided by 16,384 ided by 8,192 ided by 4,096 ided by 2,048 ided by 1,024 ided by 512 ided by 512 ided by 256 ided by 128 ided by 4 ided by 4 ided by 4 ided by 2	3 4			
bit 7-0	Unimpleme	nted: Read as ')'				

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10.3 Input Change Notification

The input change notification function of the I/O ports allows the PIC24FJ256GA110 family of devices to generate interrupt requests to the processor in response to a change of state on selected input pins. This feature is capable of detecting input change of states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 81 external inputs that may be selected (enabled) for generating an interrupt request on a change of state.

Registers, CNEN1 through CNEN6, contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin has both a weak pull-up and a weak pull-down connected to it. The pull-up acts as a current source that is connected to the pin, while the pull-down acts as a current sink that is connected to the pin. These eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are separately enabled using the CNPU1 through CNPU6 registers (for pull-ups) and the CNPD1 through CNPD6 registers (for pull-downs). Each CN pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

When the internal pull-up is selected, the pin pulls up to $V_{DD} - 0.7V$ (typical). Make certain that there is no external pull-up source when the internal pull-ups are enabled, as the voltage difference can cause a current path.

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

10.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. In an application that needs to use more than one peripheral multiplexed on a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select feature provides an alternative to these choices by enabling the user's peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of any one of many digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

10.4.1 AVAILABLE PINS

The Peripheral Pin Select feature is used with a range of up to 46 pins, depending on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation "RPn" or "RPIn" in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

PIC24FJ256GA110 family devices support a larger number of remappable input only pins than remappable input/output pins. In this device family, there are up to 32 remappable input/output pins, depending on the pin count of the particular device selected; these are numbered, RP0 through RP31. Remappable input only pins are numbered above this range, from RPI32 to RPI45 (or the upper limit for that particular device).

See Table 1-4 for a summary of pinout options in each package offering.

REGISTER 10-3: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT4R5	INT4R4	INT4R3	INT4R2	INT4R1	INT4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 INT4R<5:0>: Assign External Interrupt 4 (INT4) to Corresponding RPn or RPIn Pin bits

REGISTER 10-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				

'0' = Bit is cleared

bit 15-14Unimplemented: Read as '0'bit 13-8T3CKR<5:0>: Assign Timer3 External Clock (T3CK) to Corresponding RPn or RPIn Pin bits

'1' = Bit is set

bit 7-6 Unimplemented: Read as '0'

bit 5-0 T2CKR<5:0>: Assign Timer2 External Clock (T2CK) to Corresponding RPn or RPIn Pin bits

-n = Value at POR

x = Bit is unknown

REGISTER 10-22: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—		RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0	
bit 15							bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0	
bit 7 bit 0								
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-14	Unimplement	ted: Read as 'd	כי					
bit 13-8	RP1R<5:0>: RP1 Output Pin Mapping bits							
	Peripheral output number n is assigned to pin, RP1 (see Table 10-3 for peripheral function numbers).							

- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP0R<5:0>:** RP0 Output Pin Mapping bits Peripheral output number n is assigned to pin, RP0 (see Table 10-3 for peripheral function numbers).

REGISTER 10-23: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP3R<5:0>:** RP3 Output Pin Mapping bits

Peripheral output number n is assigned to pin, RP3 (see Table 10-3 for peripheral function numbers).

- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP2R<5:0>:** RP2 Output Pin Mapping bits Peripheral output number n is assigned to pin, RP2 (see Table 10-3 for peripheral function numbers).

14.0 OUTPUT COMPARE WITH DEDICATED TIMER

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, Section 35. "Output Compare with Dedicated Timer" (DS39723)

Devices in the PIC24FJ256GA110 family all feature 9 independent enhanced output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the enhanced output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 30 user-selectable trigger/sync sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

14.1 General Operating Modes

14.1.1 SYNCHRONOUS AND TRIGGER MODES

By default, the enhanced output compare module operates in a free-running mode. The internal, 16-bit counter, OCxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow, with its period synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs. In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-running mode is selected by default, or any time that the SYNCSEL bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSEL bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSEL bits determine the sync/trigger source.

14.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-Bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, modules 1 and 2 are paired, as are modules 3 and 4, and so on.) The odd-numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even module (OCy) provides the Most Significant 16 bits. Wraparounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bits (OCxCON2<8>) for both modules.

NOTES:

18.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the "PIC24F Family Reference Manual", Section 13. "Parallel Master Port (PMP)" (DS39713).

The Parallel Master Port (PMP) module is a parallel, 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable. Key features of the PMP module include:

- Up to 16 Programmable Address Lines
- · Up to 2 Chip Select Lines
- Programmable Strobe Options:
 - Individual Read and Write Strobes or;
- Read/Write Strobe with Enable Strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
 - Address Support
 - 4-Byte Deep Auto-Incrementing Buffer
- Programmable Wait States
- · Selectable Input Voltage Levels



FIGURE 18-1: PMP MODULE OVERVIEW

DC CHARACTE	RISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Parameter No.	Typical ⁽¹⁾	Max	Units		Conditions		
Operating Curr	ent (IDD): PMI	D Bits are S	et ⁽²⁾				
DC20	0.83	1.2	mA	-40°C			
DC20a	0.83	1.2	mA	+25°C	2 ov (3)		
DC20b	0.83	1.2	mA	+85°C	2.00		
DC20c	0.9	1.3	mA	+125°C			
DC20d	1.1	1.7	mA	-40°C		T MIPS	
DC20e	1.1	1.7	mA	+25°C	2 21/(4)		
DC20f	1.1	1.7	mA	+85°C	5.500		
DC20g	1.2	1.7	mA	+125°C			
DC23	3.3	4.5	mA	-40°C			
DC23a	3.3	4.5	mA	+25°C	2 01/(3)		
DC23b	3.3	4.6	mA	+85°C	2.0 V		
DC23c	3.4	4.6	mA	+125°C			
DC23d	4.3	6.5	mA	-40°C		4 10117-3	
DC23e	4.3	6.5	mA	+25°C	3 3/(4)		
DC23f	4.3	6.5	mA	+85°C	5.50		
DC23g	4.3	6.5	mA	+125°C			
DC24	18.2	24.0	mA	-40°C			
DC24a	18.2	24.0	mA	+25°C	2 51/(3)		
DC24b	18.2	24.0	mA	+85°C	2.500		
DC24c	18.2	24.0	mA	+125°C			
DC24d	18.2	24.0	mA	-40°C		TO IMIE 3	
DC24e	18.2	24.0	mA	+25°C	3 31/(4)		
DC24f	18.2	24.0	mA	+85°C	5.500		
DC24g	18.2	24.0	mA	+125°C			
DC31	15.0	54.0	μA	-40°C			
DC31a	15.0	54.0	μA	+25°C	2 01/(3)		
DC31b	20.0	69.0	μA	+85°C	2.00		
DC31c	60.0	159.0	μA	+125°C			
DC31d	57.0	96.0	μΑ	-40°C			
DC31e	57.0	96.0	μΑ	+25°C	3 31/(4)		
DC31f	95.0	145.0	μΑ	+85°C	0.00.7		
DC31g	120.0	281.0	μΑ	+125°C			

TABLE 28-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VDD. MCLR = VDD; WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator disabled (ENVREG tied to Vss).

4: On-chip voltage regulator enabled (ENVREG tied to VDD).

TADLE 20-7:	DC CHARACTERISTIC	3. 1/0 FIN INFUT SPECIFICATIONS (CONTINUED)				
		Standard Operating Cor	nditions: 2.0V to 3.6V (unless otherwise stated)			
DC CHARACTI	ERISTICS	Operating temperature	-40°C < TA < +85°C for Industrial			

CUADACTEDICTICS, 1/0 DIN INDUT ODECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Operating temp	-40°C \leq TA \leq +85°C for Industrial -40°C \leq TA \leq +125°C for Extended			
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions
	lı∟	Input Leakage Current ^(2,3)					
DI50		I/O Ports	—	—	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &VSS \leq VPIN \leq VDD, \\ &Pin \ at \ high-impedance \end{split}$
DI51		Analog Input Pins	—	_	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &VSS \leq V\text{PIN} \leq V\text{DD}, \\ &Pin \ at \ high-impedance \end{split}$
DI55		MCLR	—	—	<u>+</u> 1	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
DI56		OSC1	_	-	<u>+</u> 1	μA	VSS \leq VPIN \leq VDD, XT and HS modes

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-4 for I/O pins buffer types.

5: VIH requirements are met when internal pull-ups are enabled.

TABLE 28-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Sym	Characteristic	Min Typ ⁽¹⁾ Max Units Conditions					
	Vol	Output Low Voltage						
DO10		I/O Ports	—	_	0.4	V	IOL = 8.5 mA, VDD = 3.6V	
			—	_	0.4	V	IOL = 6.0 mA, VDD = 2.0V	
DO16		OSC2/CLKO	—	_	0.4	V	IOL = 8.5 mA, VDD = 3.6V	
					0.4	V	IOL = 6.0 mA, VDD = 2.0V	
	Vон	Output High Voltage						
DO20		I/O Ports	3.0	_	—	V	Юн = -3.0 mA, VDD = 3.6V	
			2.4	_	—	V	Юн = -6.0 mA, VDD = 3.6V	
			1.65	_	—	V	Юн = -1.0 mA, VDD = 2.0V	
			1.4	—	—	V	ЮН = -3.0 mA, VDD = 2.0V	
DO26		OSC2/CLKO	2.4	—	—	V	Юн = -6.0 mA, VDD = 3.6V	
			1.4		—	V	ЮН = -3.0 mA, VDD = 2.0V	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

- 3: Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-4 for I/O pins buffer types.
- **5:** VIH requirements are met when internal pull-ups are enabled.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

Mold Draft Angle Top

Mold Draft Angle Bottom

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

α

β

11°

11°

12°

12°

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

13°

13°

NOTES: