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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga106-e-mr

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Pin Number			Innit	
Function	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP	I/O	Buffer	Description
CTED1	28	34	42	I	ANA	CTMU External Edge Input 1.
CTED2	27	33	41	Ι	ANA	CTMU External Edge Input 2.
CTPLS	29	35	43	0		CTMU Pulse Output.
CVREF	23	29	34	0	_	Comparator Voltage Reference Output.
ENVREG	57	71	86	I	ST	Voltage Regulator Enable.
INT0	35	45	55	I	ST	External Interrupt Input.
MCLR	7	9	13	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	39	49	63	I	ANA	Main Oscillator Input Connection.
OSCO	40	50	64	0	ANA	Main Oscillator Output Connection.
PGEC1	15	19	24	I/O	ST	In-Circuit Debugger/Emulator/ICSP™ Programming Clock.
PGED1	16	20	25	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PGEC2	17	21	26	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock.
PGED2	18	22	27	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PGEC3	11	15	20	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Clock.
PGED3	12	16	21	I/O	ST	In-Circuit Debugger/Emulator/ICSP Programming Data.
PMA0	30	36	44	I/O	ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	35	43	I/O	ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	10	14	0		Parallel Master Port Address (Demultiplexed Master
PMA3	6	8	12	0		modes).
PMA4	5	7	11	0	_	
PMA5	4	6	10	0	—	
PMA6	16	24	29	0	—	
PMA7	22	23	28	0		
PMA8	32	40	50	0	—	
PMA9	31	39	49	0	—	
PMA10	28	34	42	0	—	
PMA11	27	33	41	0	—	
PMA12	24	30	35	0	—	
PMA13	23	29	34	0	—	
PMCS1	45	57	71	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe/Address Bit 15.
PMCS2	44	56	70	0	ST	Parallel Master Port Chip Select 2 Strobe/Address Bit 14.
PMBE	51	63	78	0	—	Parallel Master Port Byte Enable Strobe.
PMD0	60	76	93	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or
PMD1	61	77	94	I/O	ST/TTL	Address/Data (Multiplexed Master modes).
PMD2	62	78	98	I/O	ST/TTL	
PMD3	63	79	99	I/O	ST/TTL	
PMD4	64	80	100	I/O	ST/TTL	-
PMD5	1	1	3	I/O	ST/TTL	-
PMD6	2	2	4	I/O	ST/TTL	-
PMD7	3	3	5	I/O	ST/TTL	
PMRD	53	67	82	0	—	Parallel Master Port Read Strobe.
PMWR	52	66	81	0	—	Parallel Master Port Write Strobe.
Legend:	TTL = TTL inj ANA = Analog	out buffer g level input/o	utput		ST = S I <sup>2</sup> C™ :	Schmitt Trigger input buffer = I <sup>2</sup> C/SMBus input buffer

### TABLE 1-4: PIC24FJ256GA110 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

		Pin Number				
Function	64-Pin TQFP, QFN	80-Pin TQFP	100-Pin TQFP	I/O	Input Buffer	Description
RA0	_	-	17	I/O	ST	PORTA Digital I/O.
RA1	—	_	38	I/O	ST	
RA2	_	_	58	I/O	ST	
RA3	_	_	59	I/O	ST	
RA4	—	_	60	I/O	ST	
RA5	_	_	61	I/O	ST	
RA6	_	_	91	I/O	ST	
RA7	_		92	I/O	ST	
RA9	_	23	28	I/O	ST	
RA10	—	24	29	I/O	ST	
RA14	—	52	66	I/O	ST	
RA15	_	53	67	I/O	ST	
RB0	16	20	25	I/O	ST	PORTB Digital I/O.
RB1	15	19	24	I/O	ST	
RB2	14	18	23	I/O	ST	
RB3	13	17	22	I/O	ST	
RB4	12	16	21	I/O	ST	
RB5	11	15	20	I/O	ST	
RB6	17	21	26	I/O	ST	
RB7	18	22	27	I/O	ST	
RB8	21	27	32	I/O	ST	
RB9	22	28	33	I/O	ST	
RB10	23	29	34	I/O	ST	
RB11	24	30	35	I/O	ST	
RB12	27	33	41	I/O	ST	
RB13	28	34	42	I/O	ST	-
RB14	29	35	43	I/O	ST	
RB15	30	36	44	I/O	ST	
RC1	—	4	6	I/O	ST	PORTC Digital I/O.
RC2	—	_	7	I/O	ST	
RC3	—	5	8	I/O	ST	
RC4	_		9	I/O	ST	
RC12	39	49	63	I/O	ST	
RC13	47	59	73	I/O	ST	
RC14	48	60	74	I/O	ST	
RC15	40	50	64	I/O	ST	

ΤΔRI F 1-4·	PIC24EJ256GA110 FAMILY PINOUT DESCRIPTIONS (	
IADLE 1-4.	FIC24FJ250GATTO FAMILI FINOUT DESCRIFTIONS	CONTINUED)

**Legend:** TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer

I<sup>2</sup>C<sup>™</sup> = I<sup>2</sup>C/SMBus input buffer

#### 2.4 **Voltage Regulator Pins** (ENVREG/DISVREG and VCAP/VDDCORE)

Note:	This section applies only to PIC24F J
	devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- · For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to Section 25.2 "On-Chip Voltage Regulator" for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (<  $5\Omega$ ) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to Section 28.0 "Electrical Characteristics" for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to Section 28.0 "Electrical Characteristics" for information on VDD and VDDCORE.



TABLE 2-1:	SUITABLE CAPACITOR	EQUIVALENTS				
Make	Part #	Part # Nominal Base Toleran				
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125°C	
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85°C	
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125°C	
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85°C	
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125°C	
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85°C	

#### REGISTER 3-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0

00	00	00	00	1000	1411 0	00	00
—	_		_	IPL3 <sup>(1)</sup>	PSV		_
bit 7							bit 0

Legend:	C = Clearable bit						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-4 **Unimplemented:** Read as '0'

- bit 3IPL3: CPU Interrupt Priority Level Status bit<sup>(1)</sup>1 = CPU interrupt priority level is greater than 70 = CPU interrupt priority level is 7 or lessbit 2PSV: Program Space Visibility in Data Space Enable bit1 = Program space visible in data space0 = Program space not visible in data spacebit 1-0Unimplemented: Read as '0'
- **Note 1:** User interrupts are disabled when IPL3 = 1.

## TABLE 4-12: PORTA REGISTER MAP<sup>(1)</sup>

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7 <sup>(2)</sup>	Bit 6 <sup>(2)</sup>	Bit 5 <sup>(2)</sup>	Bit 4 <sup>(2)</sup>	Bit 3 <sup>(2)</sup>	Bit2 <sup>(2)</sup>	Bit 1 <sup>(2)</sup>	Bit 0 <sup>(2)</sup>	All Resets
TRISA	02C0	TRISA15	TRISA14	_	_	_	TRISA10	TRISA9	_	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	36FF
PORTA	02C2	RA15	RA14	—	_	_	RA10	RA9	_	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	02C4	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
ODCA	02C6	ODA15	ODA14	_	_	_	ODA10	ODA9	_	ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Reset values shown are for 100-pin devices.

Note 1: PORTA and all associated bits are unimplemented on 64-pin devices and read as '0'. Bits are available on 80-pin and 100-pin devices only, unless otherwise noted.

2: Bits are implemented on 100-pin devices only; otherwise, read as '0'.

#### TABLE 4-13: PORTB REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	02CE	ODB15	ODB14	ODB13	ODB12	ODB11	ODB10	ODB9	ODB8	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	0000

Legend: Reset values are shown in hexadecimal.

#### TABLE 4-14: PORTC REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4 <sup>(1)</sup>	Bit 3 <sup>(2)</sup>	Bit 2 <sup>(1)</sup>	Bit 1 <sup>(2)</sup>	Bit 0	All Resets
TRISC	02D0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	_	—	_	—	—	TRISC4	TRISC3	TRISC2	TRISC1	_	F01E
PORTC	02D2	RC15 <sup>(3,4)</sup>	RC14	RC13	RC12 <sup>(3)</sup>	—	—	—	—	_	—	—	RC4	RC3	RC2	RC1	_	xxxx
LATC	02D4	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	_	xxxx
ODCC	02D6	ODC15	ODC14	ODC13	ODC12	—	—	_	—	—	—	—	ODC4	ODC3	ODC2	ODC1	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Reset values shown are for 100-pin devices.

**Note** 1: Bits are unimplemented in 64-pin and 80-pin devices; read as '0'.

2: Bits are unimplemented in 64-pin devices; read as '0'.

3: RC12 and RC15 are only available when the Primary Oscillator is disabled or when EC mode is selected (POSCMD<1:0> Configuration bits = 11 or 00); otherwise, read as '0'

4: RC15 is only available when POSCMD<1:0> Configuration bits = 11 or 00 and the OSCIOFN Configuration bit = 1.

#### TABLE 4-15: PORTD REGISTER MAP

File Name	Addr	Bit 15 <sup>(1)</sup>	Bit 14 <sup>(1)</sup>	Bit 13 <sup>(1)</sup>	Bit 12 <sup>(1)</sup>	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D8	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	02DA	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	02DC	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	02DE	ODD15	ODD14	ODD13	ODD12	ODD11	ODD10	ODD9	ODD8	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Reset values shown are for 100-pin devices.

Note 1: Bits are unimplemented on 64-pin devices; read as '0'.

#### 4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

 TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>). In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when the byte select is '1'; the lower byte is selected when it is '0'. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'. In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address (TBLPAG) register. TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

**Note:** Only table read operations will execute in the configuration memory space, and only then, in implemented areas, such as the Device ID. Table write operations are not allowed.



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			11.0									
		0-0	U-U	0-0	0-0	K/W-0	K/W-U					
hit 15	IUPUWR		_		—		L LINIOLL hit o					
bit 15							Dit 0					
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1					
EXTR	SWR	SWDTEN <sup>(2)</sup>	WDTO	SLEEP	IDLE	BOR	POR					
bit 7							bit 0					
Legend:	Legena: R = Readable bit W = Writable bit II = Unimplemented bit read as '0'											
$R = Readable bit \qquad V = Witable bit \qquad U = Offiniplemented bit, read as U = n = Value at POP \qquad (1' = Pit is set (0' = Pit is cleared x = Pit is unknown)$												
TT Value												
bit 15	TRAPR: Trap	Reset Flag bit										
	$1 = A \operatorname{Trap} Co$	onflict Reset has	occurred	1								
bit 14		egal Opcode or U	not occurred Ininitialized V	v Access Reset	Flag bit							
Sit 11	1 = An illegal	l opcode detectio	on, an illegal a	address mode o	r uninitialized W	/ register used	as an Address					
	Pointer c	aused a Reset										
hit 13_10	0 = An liega	topcode or unini		eset has not occ	curred							
hit 9	CM: Configur	ration Word Mism	natch Reset F	-lag hit								
bit o	1 = A Configu	uration Word Mis	match Reset	has occurred								
	0 = A Configu	uration Word Mis	match Reset	has not occurre	ed							
bit 8	PMSLP: Prog	gram Memory Po	wer During S	Sleep bit	n Sloop							
	1 = Program r	nemory bias volta	ge is powered	d down during Sl	eep and voltage	regulator enters	Standby mode					
bit 7	EXTR: Extern	nal Reset (MCLR	) Pin bit	C		•	-					
	1 = A Master	Clear (pin) Rese	t has occurre	ed								
bit 6	0 = A Master	Clear (pin) Rese	et nas not occ	currea								
DILO	1 = A  RESET	instruction has b	een execute	d								
	0 = A reset	instruction has n	ot been exec	cuted								
bit 5	SWDTEN: So	oftware Enable/D	isable of WD	)T bit <sup>(2)</sup>								
	1 = WDT is e 0 = WDT is d	nabled isabled										
bit 4	WDTO: Watc	hdog Timer Time	e-out Flag bit									
	1 = WDT time	e-out has occurre	ed .									
<b>h</b> # 0		e-out has not occ	urred									
DIL 3	1 = Device ha	e From Sleep Fia	ag bit mode									
	0 = Device ha	as not been in SI	eep mode									
bit 2	IDLE: Wake-	up From Idle Flag	g bit									
	1 = Device ha	as been in Idle m as not been in Idl	ode e mode									
bit 1	BOR: Brown-	-out Reset Flag b	pit									
	1 = A Brown-	out Reset has or	curred. Note	that BOR is als	so set after a Po	wer-on Reset.						
	0 = A Brown-	out Reset has no	ot occurred									
DIT U	<b>POR:</b> Power- $1 = \Delta$ Power-	on Reset Flag bi	t curred									
	0 = A Power-	on Reset has no	t occurred									
Note 1:	All of the Reset	status bits may b	e set or clear	ed in software.	Setting one of th	nese bits in soft	ware does not					
٦.	cause a device f	Reset. Configuration bit	is '1' (unnro	arammed) the l	NDT is alwave	enabled record	lless of the					
۷.	SWDTEN bit set	tting.	is ⊤ (mhi0(		i is aiways (	Shabica, icyala						

## REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup>

	Vector		ΑΙντ	Inte	Interrupt Bit Locations			
Interrupt Source	Number	IVT Address	Address	Flag	Enable	Priority		
ADC1 Conversion Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>		
Comparator Event	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>		
CRC Generator	67	00009Ah	00019Ah	IFS4<3>	IEC4<3>	IPC16<14:12>		
CTMU Event	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>		
External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>		
External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>		
External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>		
External Interrupt 3	53	00007Eh	00017Eh	IFS3<5>	IEC3<5>	IPC13<6:4>		
External Interrupt 4	54	000080h	000180h	IFS3<6>	IEC3<6>	IPC13<10:8>		
I2C1 Master Event	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>		
I2C1 Slave Event	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>		
I2C2 Master Event	50	000078h	000178h	IFS3<2>	IEC3<2>	IPC12<10:8>		
I2C2 Slave Event	49	000076h	000176h	IFS3<1>	IEC3<1>	IPC12<6:4>		
I2C3 Master Event	85	0000BEh	0001BEh	IFS5<5>	IEC5<5>	IPC21<6:4>		
I2C3 Slave Event	84	0000BCh	0001BCh	IFS5<4>	IEC5<4>	IPC21<2:0>		
Input Capture 1	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>		
Input Capture 2	5	00001Eh	00011Eh	IFS0<5>	IEC0<5>	IPC1<6:4>		
Input Capture 3	37	00005Eh	00015Eh	IFS2<5>	IEC2<5>	IPC9<6:4>		
Input Capture 4	38	000060h	000160h	IFS2<6>	IEC2<6>	IPC9<10:8>		
Input Capture 5	39	000062h	000162h	IFS2<7>	IEC2<7>	IPC9<14:12>		
Input Capture 6	40	000064h	000164h	IFS2<8>	IEC2<8>	IPC10<2:0>		
Input Capture 7	22	000040h	000140h	IFS1<6>	IEC1<6>	IPC5<10:8>		
Input Capture 8	23	000042h	000142h	IFS1<7>	IEC1<7>	IPC5<14:12>		
Input Capture 9	93	0000CEh	0001CEh	IFS5<13>	IEC5<13>	IPC23<6:4>		
Input Change Notification	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>		
LVD Low-Voltage Detect	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC18<2:0>		
Output Compare 1	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>		
Output Compare 2	6	000020h	000120h	IFS0<6>	IEC0<6>	IPC1<10:8>		
Output Compare 3	25	000046h	000146h	IFS1<9>	IEC1<9>	IPC6<6:4>		
Output Compare 4	26	000048h	000148h	IFS1<10>	IEC1<10>	IPC6<10:8>		
Output Compare 5	41	000066h	000166h	IFS2<9>	IEC2<9>	IPC10<6:4>		
Output Compare 6	42	000068h	000168h	IFS2<10>	IEC2<10>	IPC10<10:8>		
Output Compare 7	43	00006Ah	00016Ah	IFS2<11>	IEC2<11>	IPC10<14:12>		
Output Compare 8	44	00006Ch	00016Ch	IFS2<12>	IEC2<12>	IPC11<2:0>		
Output Compare 9	92	0000CCh	0001CCh	IFS5<12>	IEC5<12>	IPC23<2:0>		
Parallel Master Port	45	00006Eh	00016Eh	IFS2<13>	IEC2<13>	IPC11<6:4>		
Real-Time Clock/Calendar	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>		
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>		
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>		
SPI2 Error	32	000054h	000154h	IFS2<0>	IEC2<0>	IPC8<2:0>		
SPI2 Event	33	000056h	000156h	IFS2<1>	IEC2<1>	IPC8<6:4>		
SPI3 Error	90	0000C8h	0001C8h	IFS5<10>	IEC5<10>	IPC22<10:8>		
SPI3 Event	91	0000CAh	0001CAh	IFS5<11>	IEC5<11>	IPC22<14:12>		

TABLE 7-2:	<b>IMPLEMENTED INTERRUPT VECTORS</b>

### REGISTER 7-1: SR: ALU STATUS REGISTER (IN CPU)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
—	—	—	—	—	—	—	DC <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 <sup>(2,3)</sup>	IPL1 <sup>(2,3)</sup>	IPL0 <sup>(2,3)</sup>	RA <sup>(1)</sup>	N <sup>(1)</sup>	OV <sup>(1)</sup>	Z <sup>(1)</sup>	C <sup>(1)</sup>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits <sup>(2,3)</sup>
	111 = CPU interrupt priority level is 7 (15). User interrupts disabled.
	110 = CPU interrupt priority level is 6 (14)
	101 = CPU interrupt priority level is 5 (13)
	100 = CPU interrupt priority level is 4 (12)
	011 = CPU interrupt priority level is 3 (11)
	010 = CPU interrupt priority level is 2 (10)
	001 = CPU interrupt priority level is 1 (9)
	000 = CPU interrupt priority level is 0 (8)

- **Note 1:** See Register 3-1 for the description of the remaining bit(s) that are not dedicated to interrupt control functions.
  - **2:** The IPL bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the interrupt priority level if IPL3 = 1.
  - 3: The IPL Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 7-2:	CORCON: CPU CON	TROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	-	—	—	—	—		
bit 15							bit 8		
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0		
—	—	—	—	IPL3 <sup>(2)</sup>	PSV <sup>(1)</sup>	—	—		
bit 7	•						bit 0		
Legend:		C = Clearable	bit						
R = Readable b	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	ared	x = Bit is unknown			

bit 3 IPL3: CPU Interrupt Priority Level Status bit<sup>(2)</sup> 1 = CPU interrupt priority level is greater than 7 0 = CPU interrupt priority level is 7 or less

- **Note 1:** See Register 3-2 for the description of the remaining bit(s) that are not dedicated to interrupt control functions.
  - 2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

## 8.5 Reference Clock Output

In addition to the CLKO output (Fosc/2) available in certain oscillator modes, the device clock in the PIC24FJ256GA110 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 8-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the Primary Oscillator modes (EC, HS or XT); otherwise, if the POSCEN bit is also not set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

### REGISTER 10-11: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
—	—	IC9R5	IC9R4	IC9R3	IC9R2	IC9R1	IC9R0		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	_	—	—	—	—		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1		'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown			

bit 15-14Unimplemented: Read as '0'bit 13-8IC9R<5:0>: Assign Input Capture 9 (IC9) to Corresponding RPn or RPIn Pin bitsbit 7-0Unimplemented: Read as '0'

### REGISTER 10-12: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
—	—	U3RXR5	U3RXR4	U3RXR3	U3RXR2	U3RXR1	U3RXR0		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	—	—	—	—	_		
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown					

bit 15-14 Unimplemented: Read as '0'

bit 13-8 U3RXR<5:0>: Assign UART3 Receive (U3RX) to Corresponding RPn or RPIn Pin bits

bit 7-0 Unimplemented: Read as '0'

#### TyCON: TIMER3 AND TIMER5 CONTROL REGISTER<sup>(3)</sup> **REGISTER 12-2:** R/W-0 U-0 R/W-0 U-0 U-0 U-0 U-0 U-0 TON<sup>(1)</sup> TSIDL<sup>(1)</sup> \_\_\_ \_\_\_\_ bit 15 bit 8 U-0 R/W-0 R/W-0 R/W-0 U-0 U-0 R/W-0 U-0 TGATE<sup>(1)</sup> TCKPS1<sup>(1)</sup> TCKPS0<sup>(1)</sup> TCS<sup>(1,2)</sup> bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' '0' = Bit is cleared -n = Value at POR '1' = Bit is set x = Bit is unknown bit 15 TON: Timery On bit<sup>(1)</sup> 1 = Starts 16-bit Timery 0 = Stops 16-bit Timery Unimplemented: Read as '0' bit 14 TSIDL: Stop in Idle Mode bit<sup>(1)</sup> bit 13 1 = Discontinue module operation when device enters Idle mode 0 = Continue module operation in Idle mode bit 12-7 Unimplemented: Read as '0' TGATE: Timery Gated Time Accumulation Enable bit<sup>(1)</sup> bit 6 When TCS = 1: This bit is ignored. When TCS = 0: 1 = Gated time accumulation enabled 0 = Gated time accumulation disabled bit 5-4 TCKPS<1:0>: Timery Input Clock Prescale Select bits<sup>(1)</sup> 11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1 bit 3-2 Unimplemented: Read as '0' TCS: Timery Clock Source Select bit<sup>(1,2)</sup> bit 1 1 = External clock from pin TyCK (on the rising edge) 0 = Internal clock (Fosc/2) bit 0 Unimplemented: Read as '0' **Note 1:** When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

- 2: If TCS = 1, RPINRx (TyCK) must be configured to an available RPn pin. See Section 10.4 "Peripheral **Pin Select**" for more information.
- **3:** Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

## 13.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own 16-bit timer. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, modules 1 and 2 are paired, as are modules 3 and 4, and so on.) The odd-numbered module (ICx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even module (ICy) provides the Most Significant 16 bits. Wraparounds of the ICx registers cause an increment of their corresponding ICy registers.

Cascaded operation is configured in hardware by setting the IC32 bits (ICxCON2<8>) for both modules.

## 13.2 Capture Operations

The enhanced input capture module can be configured to capture timer values and generate interrupts on rising edges on ICx, or all transitions on ICx. Captures can be configured to occur on all rising edges or just some (every 4th or 16th). Interrupts can be independently configured to generate on each event or a subset of events.

To set up the module for capture operations:

- 1. Configure the ICx input for one of the available Peripheral Pin Select pins.
- 2. If Synchronous mode is to be used, disable the sync source before proceeding.
- Make sure that any previous data has been removed from the FIFO by reading ICxBUF until the ICBNE bit (ICxCON1<3>) is cleared.
- 4. Set the SYNCSEL bits (ICxCON2<4:0>) to the desired sync/trigger source.
- 5. Set the ICTSEL bits (ICxCON1<12:10>) for the desired clock source.
- 6. Set the ICI bits (ICxCON1<6:5>) to the desired interrupt frequency
- 7. Select Synchronous or Trigger mode operation:
  - a) Check that the SYNCSEL bits are not set to '00000'.
  - b) For Synchronous mode, clear the ICTRIG bit (ICxCON2<7>).
  - c) For Trigger mode, set ICTRIG and clear the TRIGSTAT bit (ICxCON2<6>).
- 8. Set the ICM bits (ICxCON1<2:0>) to the desired operational mode.
- 9. Enable the selected trigger/sync source.

For 32-bit cascaded operations, the setup procedure is slightly different:

- 1. Set the IC32 bits for both modules (ICyCON2<8> and (ICxCON2<8>), enabling the even-numbered module first. This ensures the modules will start functioning in unison.
- 2. Set the ICTSEL and SYNCSEL bits for both modules to select the same sync/trigger and time base source. Set the even module first, then the odd module. Both modules must use the same ICTSEL and SYNCSEL settings.
- Clear the ICTRIG bit of the even module (ICyCON2<7>); this forces the module to run in Synchronous mode with the odd module, regardless of its trigger setting.
- 4. Use the odd module's ICI bits (ICxCON1<6:5>) to the desired interrupt frequency.
- 5. Use the ICTRIG bit of the odd module (ICxCON2<7>) to configure Trigger or Synchronous mode operation.
- Note: For Synchronous mode operation, enable the sync source as the last step. Both input capture modules are held in Reset until the sync source is enabled.
- 6. Use the ICM bits of the odd module (ICxCON1<2:0>) to set the desired capture mode.

The module is ready to capture events when the time base and the trigger/sync source are enabled. When the ICBNE bit (ICxCON1<3>) becomes set, at least one capture value is available in the FIFO. Read input capture values from the FIFO until the ICBNE clears to '0'.

For 32-bit operation, read both the ICxBUF and ICyBUF for the full 32-bit timer value (ICxBUF for the Isw, ICyBUF for the msw). At least one capture value is available in the FIFO buffer when the odd module's ICBNE bit (ICxCON1<3>) becomes set. Continue to read the buffer registers until ICBNE is cleared (perform automatically by hardware).

### REGISTER 13-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

-0 1								
- bit 9								
V-0								
0 <sup>(1)</sup>								
bit 0								
11 = Interrupt on every fourth capture event								
10 = Interrupt on every third capture event								
1 - mput capture overnow occurred0 = No input capture overflow occurred								
ICBNE: Input Capture x Buffer Empty Status bit (read-only)								
1 = Input capture buffer is not empty, at least one more capture value can be read								
ICM<2:0>: Input Capture Mode Select bits <sup>(1)</sup>								
111 = Interrupt mode: Input capture functions as interrupt pin only when device is in Sleep or Idle mode								
(rising edge detect only, all other control bits are not applicable)								
101 = Prescaler Capture mode: Capture on every 16th rising edge								
011 = Simple Capture mode: Capture on every rising edge								
do not								
e mod								

Note 1: The ICx input must also be configured to an available RPn pin. For more information, see Section 10.4 "Peripheral Pin Select".

bits

## EQUATION 14-2: CALCULATION FOR MAXIMUM PWM RESOLUTION<sup>(1)</sup>

Maximum PWM Resolution (bits) =  $\frac{\log_{10} \left( \frac{FCY}{FPWM \bullet (Timer Prescale Value)} \right)}{1 + \frac{FCY}{FPWM \bullet (Timer Prescale Value)}}$ 

 $\log_{10}(2)$ 

**Note 1:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

## EXAMPLE 14-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS<sup>(1)</sup>

1.	<ol> <li>Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where FOSC = 8 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.</li> </ol>							
	TCY = 2 * TOSC = 62.5  ns							
	PWM Period = $1/PWM$ Frequency = $1/52.08$ kHz = $19.2 \mu s$							
	PWM Period = $(PR2 + 1) \bullet TCY \bullet (Timer2 Prescale Value)$							
	19.2 $\mu$ s = (PR2 + 1) • 62.5 ns • 1							
	PR2 = 306							
2.	Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:							
	PWM Resolution = $\log_{10}(FCY/FPWM)/\log_{10}2)$ bits							
	= $(\log_{10}(16 \text{ MHz}/52.08 \text{ kHz})/\log_{10}2)$ bits							
	= 8.3 bits							
N	ote 1: Based on Tcy = 2 * Tosc, Doze mode and PLL are disabled.							

## TABLE 14-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (Fcy = 4 MHz)<sup>(1)</sup>

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

**Note 1:** Based on Fcy = Fosc/2, Doze mode and PLL are disabled.

### TABLE 14-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (Fcy = 16 MHz)<sup>(1)</sup>

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

**Note 1:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

## 17.1 UART Baud Rate Generator (BRG)

The UART module includes a dedicated 16-bit Baud Rate Generator. The UxBRG register controls the period of a free-running, 16-bit timer. Equation 17-1 shows the formula for computation of the baud rate with BRGH = 0.

#### EQUATION 17-1: UART BAUD RATE WITH BRGH = $0^{(1,2)}$

Baud Rate =  $\frac{FCY}{16 \cdot (UxBRG + 1)}$ UxBRG =  $\frac{FCY}{16 \cdot Baud Rate} - 1$ 

**Note 1:** FCY denotes the instruction cycle clock frequency (FOSC/2).

**2:** Based on FCY = FOSC/2, Doze mode and PLL are disabled.

Example 17-1 shows the calculation of the baud rate error for the following conditions:

• Fcy = 4 MHz

EXAMPLE 17-1:

• Desired Baud Rate = 9600

The maximum baud rate (BRGH = 0) possible is FCY/16 (for UxBRG = 0) and the minimum baud rate possible is FCY/(16 \* 65536).

Equation 17-2 shows the formula for computation of the baud rate with BRGH = 1.

## EQUATION 17-2: UART BAUD RATE WITH BRGH = $1^{(1,2)}$

Baud Rate =	$\frac{FCY}{4 \bullet (UxBRG + 1)}$	
UxBRG =	FCY 4 • Baud Rate	- 1

- **Note 1:** FCY denotes the instruction cycle clock frequency.
  - 2: Based on Fcy = Fosc/2, Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 1) possible is FcY/4 (for UxBRG = 0) and the minimum baud rate possible is FcY/(4 \* 65536).

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

#### Desired Baud Rate = FCY/(16 (UxBRG + 1))Solving for UxBRG value: UxBRG = ((FCY/Desired Baud Rate)/16) - 1UxBRG = ((400000/9600)/16) - 1**UxBRG** = 25 Calculated Baud Rate = 400000/(16(25+1))= 9615 Error = (Calculated Baud Rate – Desired Baud Rate) Desired Baud Rate = (9615 - 9600)/9600= 0.16% Note 1: Based on FCY = FOSC/2, Doze mode and PLL are disabled.

BAUD RATE ERROR CALCULATION (BRGH = 0)<sup>(1)</sup>

## FIGURE 20-2: CRC SHIFT ENGINE DETAIL



### 20.1 User Interface

#### 20.1.1 DATA INTERFACE

To start serial shifting, a '1' must be written to the CRCGO bit.

The module incorporates a FIFO that is 8 deep when PLEN<3:0> (CRCCON<3:0>) > 7 and 16 deep, otherwise. The data for which the CRC is to be calculated must first be written into the FIFO. The smallest data element that can be written into the FIFO is one byte. For example, if PLEN = 5, then the size of the data is PLEN + 1 = 6. When loading data, the two MSbs of the data byte are ignored.

Once data is written into the CRCWDAT MSb (as defined by PLEN), the value of VWORD<4:0> (CRCCON<12:8>) increments by one. When CRCGO = 1 and VWORD > 0, a word of data to be shifted is moved from the FIFO into the shift engine. When the data word moves from the FIFO to the shift engine, the VWORD bits decrement by one. The serial shifter continues to receive data from the FIFO, shifting until the VWORD bits reach 0. The last bit of data will be shifted through the CRC module (PLEN + 1)/2 clock cycles after the VWORD bits reach 0. This is when the module is completed with the CRC calculation.

Therefore, for a given value of PLEN, it will take (PLEN + 1)/2 \* VWORD number of clock cycles to complete the CRC calculations.

When VWORD<4:0> reach 8 (or 16), the CRCFUL bit will be set. When VWORD<4:0> reach 0, the CRCMPT bit will be set.

To continually feed data into the CRC engine, the recommended mode of operation is to initially "prime" the FIFO with a sufficient number of words so no interrupt is generated before the next word can be written. Once that is done, start the CRC by setting the CRCGO bit to '1'. From that point onward, the VWORD bits should be polled. If they read less than 8 or 16, another word can be written into the FIFO.

To empty words already written into a FIFO, the CRCGO bit must be set to '1' and the CRC shifter allowed to run until the CRCMPT bit is set.

Also, to get the correct CRC reading, it will be necessary to wait for the CRCMPT bit to go high before reading the CRCWDAT register.

If a word is written when the CRCFUL bit is set, the VWORD Pointer will roll over to 0. The hardware will then behave as if the FIFO is empty. However, the condition to generate an interrupt will not be met; therefore, no interrupt will be generated (See Section 20.1.2 "Interrupt Operation").

At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORD bits is done.

#### 20.1.2 INTERRUPT OPERATION

When the VWORD<4:0> bits make a transition from a value of '1' to '0', an interrupt will be generated. Note that the CRC calculation is not complete at this point; an additional time of (PLEN + 1)/2 clock cycles is required before the output can be read.

## 20.2 Operation in Power Save Modes

#### 20.2.1 SLEEP MODE

If Sleep mode is entered while the module is operating, the module will be suspended in its current state until clock execution resumes.

### 20.2.2 IDLE MODE

To continue full module operation in Idle mode, the CSIDL bit must be cleared prior to entry into the mode.

If CSIDL = 1, the module will behave the same way as it does in Sleep mode; pending interrupt events will be passed on, even though the module clocks are not available.

## 23.0 COMPARATOR VOLTAGE REFERENCE

Note:	This data sheet summarizes the features of								
	this group	of PIC	24F devices	. It is not					
	intended to be a comprehensive reference								
	source. For more information, refer to the								
	"PIC24F Family Reference Manual",								
	Section	20. "(	Comparator	Voltage					
	Reference	Module	" (DS39709)						

### 23.1 Configuring the Comparator Voltage Reference

The voltage reference module is controlled through the CVRCON register (Register 23-1). The comparator voltage reference provides two ranges of output

voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF Selection bits (CVR<3:0>), with one range offering finer resolution.

The comparator reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<4>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.



### FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



#### FIGURE 28-14: SPIX MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 1)

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param No.	Symbol	Characteristic	Min	Тур <sup>(1)</sup>	Max	Units	Conditions
SP70	TscL	SCKx Input Low Time	30	_	_	ns	
SP71	TscH	SCKx Input High Time	30	_	_	ns	
SP72	TscF	SCKx Input Fall Time <sup>(2)</sup>	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time <sup>(2)</sup>	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time <sup>(2)</sup>	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time <sup>(2)</sup>	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}} \downarrow$ to SCKx $\downarrow$ or SCKx $\uparrow$ Input	120	_	_	ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance <sup>(3)</sup>	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 TCY + 40	_		ns	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	_	50	ns	

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

**3:** Assumes 50 pF load on all SPIx pins.

## **Revision E (November 2010)**

Added 64-Kbyte device variants – PIC24FJ64GA106, PIC24FJ64GA108 and PIC24FJ64GA110.

Changed the CON bit to CEN to match other existing PIC24F, PIC24H and dsPIC® products.

Changed the VREFS bit to PMSLP to match other existing PIC24F, PIC24H and dsPIC® products.

Corrected the OCxCON2 and ICxCON2 Reset values in the register descriptions.

Defined SOSC and RTCC behavior during  $\overline{\text{MCLR}}$  events.

Corrected the RCFGCAL Reset values in the register descriptions.

Updated Configuration Word unprogrammed information to more accurately reflect the devices' behavior.

Added electrical specifications from the "PIC24F Family Reference Manual".

Corrected errors in the ENVREG pin operation descriptions.

Other minor typographic corrections throughout the document.