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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga108-i-pt

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64/80/100-Pin, 16-Bit, General Purpose Flash Microcontrollers with Peripheral Pin Select

Power Management:

- On-Chip 2.5V Voltage Regulator
- Switch between Clock Sources in Real Time
- Idle, Sleep and Doze modes with Fast Wake-up and Two-Speed Start-up
- Run mode: 1 mA/MIPS, 2.0V Typical
- Standby Current with 32 kHz Oscillator: 2.6 μ A, 2.0V Typical

High-Performance CPU:

- Modified Harvard Architecture
- Up to 16 MIPS Operation at 32 MHz
- 8 MHz Internal Oscillator
- 17-Bit x 17-Bit Single-Cycle Hardware Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16 x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture with Flexible Addressing modes
- Linear Program Memory Addressing, Up to 12 Mbytes
- Linear Data Memory Addressing, Up to 64 Kbytes
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Analog Features:

- 10-Bit, Up to 16-Channel Analog-to-Digital (A/D) Converter at 500 ksp/s:
 - Conversions available in Sleep mode
- Three Analog Comparators with Programmable Input/Output Configuration
- Charge Time Measurement Unit (CTMU)

Peripheral Features:

- Peripheral Pin Select:
 - Allows independent I/O mapping of many peripherals at run time
 - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
 - Up to 46 available pins (100-pin devices)
- Three 3-Wire/4-Wire SPI modules (supports 4 Frame modes) with 8-Level FIFO Buffer
- Three I²C™ modules support Multi-Master/Slave modes and 7-Bit/10-Bit Addressing
- Four UART modules:
 - Supports RS-485, RS-232, LIN/J2602 protocols and IrDA®
 - On-chip hardware encoder/decoder for IrDA
 - Auto-wake-up and Auto-Baud Detect (ABD)
 - 4-level deep FIFO buffer
- Five 16-Bit Timers/Counters with Programmable Prescaler
- Nine 16-Bit Capture Inputs, each with a Dedicated Time Base
- Nine 16-Bit Compare/PWM Outputs, each with a Dedicated Time Base
- 8-Bit Parallel Master Port (PMP/PSP):
 - Up to 16 address pins
 - Programmable polarity on control lines
- Hardware Real-Time Clock/Calendar (RTCC):
 - Provides clock, calendar and alarm functions
- Programmable Cyclic Redundancy Check (CRC) Generator
- Up to 5 External Interrupt Sources

PIC24FJ Device	Pins	Program Memory (Bytes)	SRAM (Bytes)	Remappable Peripherals						I ² C™	10-Bit A/D (ch)	Comparators	PMP/PSP	JTAG	CTMU
				Remappable Pins	Timers 16-Bit	Capture Input	Compare/PWM Output	UART w/ IrDA®	SPI						
64GA106	64	64K	16K	31	5	9	9	4	3	3	16	3	Y	Y	Y
128GA106	64	128K	16K	31	5	9	9	4	3	3	16	3	Y	Y	Y
192GA106	64	192K	16K	31	5	9	9	4	3	3	16	3	Y	Y	Y
256GA106	64	256K	16K	31	5	9	9	4	3	3	16	3	Y	Y	Y
64GA108	80	64K	16K	42	5	9	9	4	3	3	16	3	Y	Y	Y
128GA108	80	128K	16K	42	5	9	9	4	3	3	16	3	Y	Y	Y
192GA108	80	192K	16K	42	5	9	9	4	3	3	16	3	Y	Y	Y
256GA108	80	256K	16K	42	5	9	9	4	3	3	16	3	Y	Y	Y
64GA110	100	64K	16K	46	5	9	9	4	3	3	16	3	Y	Y	Y
128GA110	100	128K	16K	46	5	9	9	4	3	3	16	3	Y	Y	Y
192GA110	100	192K	16K	46	5	9	9	4	3	3	16	3	Y	Y	Y
256GA110	100	256K	16K	46	5	9	9	4	3	3	16	3	Y	Y	Y

PIC24FJ256GA110 FAMILY

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA110 FAMILY: 100-PIN DEVICES

Features	PIC24FJ64GA110	PIC24FJ128GA110	PIC24FJ192GA110	PIC24FJ256GA110
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	64K	128K	192K	256K
Program Memory (instructions)	22,016	44,032	67,072	87,552
Data Memory (bytes)	16,384			
Interrupt Sources (soft vectors/NMI traps)	66 (62/4)			
I/O Ports	Ports A, B, C, D, E, F, G			
Total I/O Pins	85			
Remappable Pins	46 (32 I/O, 14 input only)			
Timers:				
Total Number (16-bit)	5 ⁽¹⁾			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	9 ⁽¹⁾			
Output Compare/PWM Channels	9 ⁽¹⁾			
Input Change Notification Interrupt	85			
Serial Communications:				
UART	4 ⁽¹⁾			
SPI (3-wire/4-wire)	3 ⁽¹⁾			
I ² C™	3			
Parallel Communications (PMP/PSP)	Yes			
JTAG Boundary Scan	Yes			
10-Bit Analog-to-Digital Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Resets (and delays)	POR, BOR, RESET Instruction, MCLR, WDT; Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	100-Pin TQFP			

Note 1: Peripherals are accessible through remappable pins.

TABLE 4-6: TIMER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Timer1 Period Register																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																0000
TMR3	010A	Timer3 Register																0000
PR2	010C	Timer2 Period Register																FFFF
PR3	010E	Timer3 Period Register																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																0000
TMR5	0118	Timer5 Register																0000
PR4	011A	Timer4 Period Register																FFFF
PR5	011C	Timer5 Period Register																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 7-19: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPF1IP2	SPF1IP1	SPF1IP0	—	T3IP2	T3IP1	T3IP0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	U1RXIP<2:0>: UART1 Receiver Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 11	Unimplemented: Read as '0'
bit 10-8	SPI1IP<2:0>: SPI1 Event Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 7	Unimplemented: Read as '0'
bit 6-4	SPF1IP<2:0>: SPI1 Fault Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled
bit 3	Unimplemented: Read as '0'
bit 2-0	T3IP<2:0>: Timer3 Interrupt Priority bits
	111 = Interrupt is priority 7 (highest priority interrupt)
	•
	•
	•
	001 = Interrupt is priority 1
	000 = Interrupt source is disabled

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REGISTER 7-38: IPC23: INTERRUPT PRIORITY CONTROL REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC9IP2	IC9IP1	IC9IP0	—	OC9IP2	OC9IP1	OC9IP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **IC9IP<2:0>:** Input Capture Channel 9 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **OC9IP<2:0>:** Output Compare Channel 9 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

PIC24FJ256GA110 FAMILY

8.5 Reference Clock Output

In addition to the CLKO output ($F_{osc}/2$) available in certain oscillator modes, the device clock in the PIC24FJ256GA110 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register ([Register 8-4](#)). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the Primary Oscillator modes (EC, HS or XT); otherwise, if the POSCEN bit is also not set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

PIC24FJ256GA110 FAMILY

REGISTER 10-26: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP9R5	RP9R4	RP9R3	RP9R2	RP9R1	RP9R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP8R5	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
 bit 13-8 **RP9R<5:0>:** RP9 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP9 (see [Table 10-3](#) for peripheral function numbers).
 bit 7-6 **Unimplemented:** Read as '0'
 bit 5-0 **RP8R<5:0>:** RP8 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP8 (see [Table 10-3](#) for peripheral function numbers).

REGISTER 10-27: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
 bit 13-8 **RP11R<5:0>:** RP11 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP11 (see [Table 10-3](#) for peripheral function numbers).
 bit 7-6 **Unimplemented:** Read as '0'
 bit 5-0 **RP10R<5:0>:** RP10 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP10 (see [Table 10-3](#) for peripheral function numbers).

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REGISTER 10-32: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP21R<5:0>:** RP21 Output Pin Mapping bits

Peripheral output number n is assigned to pin, RP21 (see [Table 10-3](#) for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R<5:0>:** RP20 Output Pin Mapping bits

Peripheral output number n is assigned to pin, RP20 (see [Table 10-3](#) for peripheral function numbers).

REGISTER 10-33: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP23R<5:0>:** RP23 Output Pin Mapping bits

Peripheral output number n is assigned to pin, RP23 (see [Table 10-3](#) for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP22R<5:0>:** RP22 Output Pin Mapping bits

Peripheral output number n is assigned to pin, RP22 (see [Table 10-3](#) for peripheral function numbers).

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16.3 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator reload value, use [Equation 16-1](#).

EQUATION 16-1: COMPUTING BAUD RATE RELOAD VALUE^(1,2)

$$F_{SCL} = \frac{F_{CY}}{I2CxBRG + 1 + \frac{F_{CY}}{10,000,000}}$$

or

$$I2CxBRG = \left(\frac{F_{CY}}{F_{SCL}} - \frac{F_{CY}}{10,000,000} \right) - 1$$

Note 1: Based on $F_{CY} = F_{OSC}/2$, Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

16.4 Slave Address Masking

The I2CxMSK register ([Register 16-3](#)) designates address bit positions as “don’t care” for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the slave module to respond whether the corresponding address bit value is a ‘0’ or a ‘1’. For example, when I2CxMSK is set to ‘00010000’, the slave module will detect both addresses: ‘00000000’ and ‘00100000’.

To enable address masking, the IPMI (Intelligent Peripheral Management Interface) must be disabled by clearing the IPMIEN bit (I2CxCON<11>).

Note: As a result of changes in the I²C™ protocol, the addresses in [Table 16-2](#) are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 16-1: I²C™ CLOCK RATES^(1,2)

Required System F _{SCL}	F _{CY}	I2CxBRG Value		Actual F _{SCL}
		(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	157	9D	100 kHz
100 kHz	8 MHz	78	4E	100 kHz
100 kHz	4 MHz	39	27	99 kHz
400 kHz	16 MHz	37	25	404 kHz
400 kHz	8 MHz	18	12	404 kHz
400 kHz	4 MHz	9	9	385 kHz
400 kHz	2 MHz	4	4	385 kHz
1 MHz	16 MHz	13	D	1.026 MHz
1 MHz	8 MHz	6	6	1.026 MHz
1 MHz	4 MHz	3	3	0.909 MHz

Note 1: Based on $F_{CY} = F_{OSC}/2$, Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

TABLE 16-2: I²C™ RESERVED ADDRESSES⁽¹⁾

Slave Address	R/W Bit	Description
0000 000	0	General Call Address ⁽²⁾
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 010	x	Reserved
0000 011	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 1xx	x	Reserved
1111 0xx	x	10-Bit Slave Upper Byte ⁽³⁾

Note 1: The address bits listed here will never cause an address match, independent of address mask settings.

2: The address will be Acknowledged only if GCEN = 1.

3: Match on this address can only occur on the upper byte in 10-Bit Addressing mode.

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REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables I2Cx module. All I²C pins are controlled by port functions.
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** Stop in Idle Mode bit
1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C Slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software may write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software may only write '1' to release clock). Hardware clear at beginning of slave transmission.
- bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit
1 = IPMI Support mode is enabled; all addresses Acknowledged
0 = IPMI mode disabled
- bit 10 **A10M:** 10-Bit Slave Addressing bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled
- bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with SMBus specification
0 = Disables SMBus input thresholds
- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled
- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receive clock stretching
0 = Disables software or receive clock stretching

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REGISTER 17-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾	—	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/C-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **UARTEN:** UARTx Enable bit⁽¹⁾
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽²⁾
1 = IrDA encoder and decoder enabled
0 = IrDA encoder and decoder disabled
- bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Enable bits
11 = $\overline{\text{UxTX}}$, $\overline{\text{UxRX}}$ and $\overline{\text{BCLKx}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin controlled by port latches
10 = $\overline{\text{UxTX}}$, $\overline{\text{UxRX}}$, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = $\overline{\text{UxTX}}$, $\overline{\text{UxRX}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin controlled by port latches
00 = $\overline{\text{UxTX}}$ and $\overline{\text{UxRX}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS/BCLKx}}$ pins controlled by port latches
- bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
1 = UARTx will continue to sample the $\overline{\text{UxRX}}$ pin; interrupt generated on falling edge, bit cleared in hardware on following rising edge
0 = No wake-up enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Enable Loopback mode
0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0 = Baud rate measurement disabled or completed

Note 1: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPN pin. See [Section 10.4 “Peripheral Pin Select”](#) for more information.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

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REGISTER 18-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PMPEN:** Parallel Master Port Enable bit
 1 = PMP enabled
 0 = PMP disabled, no off-chip access performed
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PSIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
 11 = Reserved
 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 3 bits are multiplexed on PMA<10:8>
 00 = Address and data appear on separate pins
- bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
 1 = PMBE port enabled
 0 = PMBE port disabled
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 1 = PMWR/PMENB port enabled
 0 = PMWR/PMENB port disabled
- bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
 1 = PMRD/ $\overline{\text{PMWR}}$ port enabled
 0 = PMRD/ $\overline{\text{PMWR}}$ port disabled
- bit 7-6 **CSF<1:0>:** Chip Select Function bits
 11 = Reserved
 10 = PMCS1 and PMCS2 function as chip select
 01 = PMCS2 functions as chip select, PMCS1 functions as address bit 14
 00 = PMCS1 and PMCS2 function as address bits 15 and 14
- bit 5 **ALP:** Address Latch Polarity bit⁽¹⁾
 1 = Active-high (PMALL and PMALH)
 0 = Active-low (PMALL and PMALH)
- bit 4 **CS2P:** Chip Select 2 Polarity bit⁽¹⁾
 1 = Active-high (PMCS2/PMCS2)
 0 = Active-low (PMCS2/PMCS2)
- bit 3 **CS1P:** Chip Select 1 Polarity bit⁽¹⁾
 1 = Active-high (PMCS1/PMCS1)
 0 = Active-low (PMCS1/PMCS1)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

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REGISTER 18-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB1 ⁽¹⁾	WAITB0 ⁽¹⁾	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1 ⁽¹⁾	WAITE0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)

- 1 = Port is busy (not useful when the processor stall is active)
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

- 11 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
- 10 = No interrupt generated, processor stall activated
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

- 11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
- 10 = Decrement ADDR<10:0> by 1 every read/write cycle
- 01 = Increment ADDR<10:0> by 1 every read/write cycle
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-Bit Mode bit

- 1 = 16-bit mode: Data register is 16 bits; a read or write to the Data register invokes two 8-bit transfers
- 0 = 8-bit mode: Data register is 8 bits; a read or write to the Data register invokes one 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

- 11 = Master Mode 1 (PMCS1, PMRD/PMWR, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
- 10 = Master Mode 2 (PMCS1, PMRD, PMWR, PMBE, PMA<x:0> and PMD<7:0>)
- 01 = Enhanced PSP, control signals (PMRD, PMWR, PMCS1, PMD<7:0> and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1 and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Wait State Configuration bits⁽¹⁾

- 11 = Data wait of 4 Tcy; multiplexed address phase of 4 Tcy
- 10 = Data wait of 3 Tcy; multiplexed address phase of 3 Tcy
- 01 = Data wait of 2 Tcy; multiplexed address phase of 2 Tcy
- 00 = Data wait of 1 Tcy; multiplexed address phase of 1 Tcy

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits

- 1111 = Wait of additional 15 Tcy
- ...
- 0001 = Wait of additional 1 Tcy
- 0000 = No additional wait cycles (operation forced into one Tcy)⁽²⁾

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits⁽¹⁾

- 11 = Wait of 4 Tcy
- 10 = Wait of 3 Tcy
- 01 = Wait of 2 Tcy
- 00 = Wait of 1 Tcy

Note 1: WAITB and WAITE bits are ignored whenever WAITM<3:0> = 0000.

2: A single cycle delay is required between consecutive read and/or write operations.

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FIGURE 18-5: MASTER MODE, PARTIALLY MULTIPLEXED ADDRESSING (SEPARATE READ AND WRITE STROBES, TWO CHIP SELECTS)

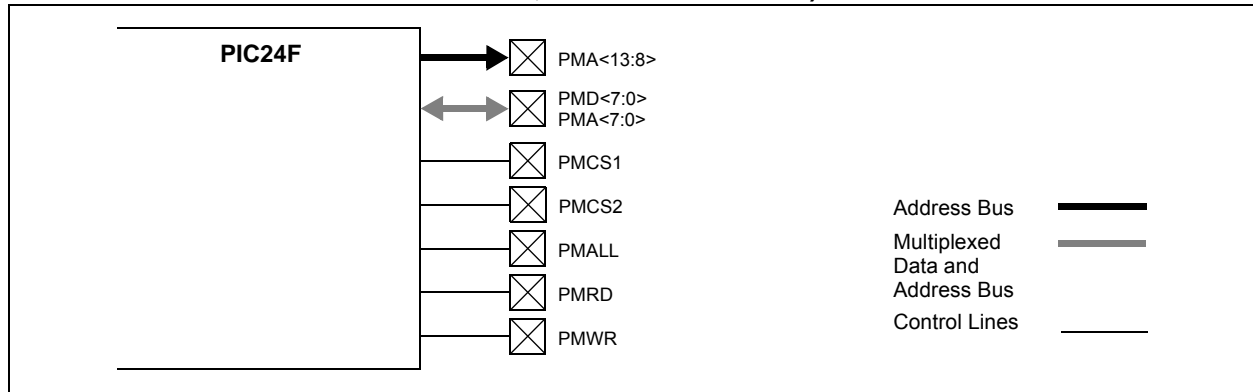


FIGURE 18-6: MASTER MODE, FULLY MULTIPLEXED ADDRESSING (SEPARATE READ AND WRITE STROBES, TWO CHIP SELECTS)

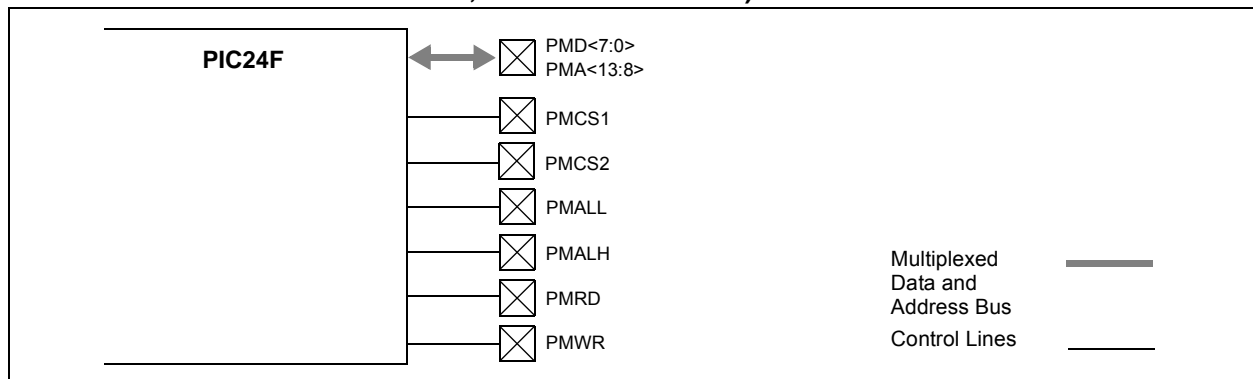
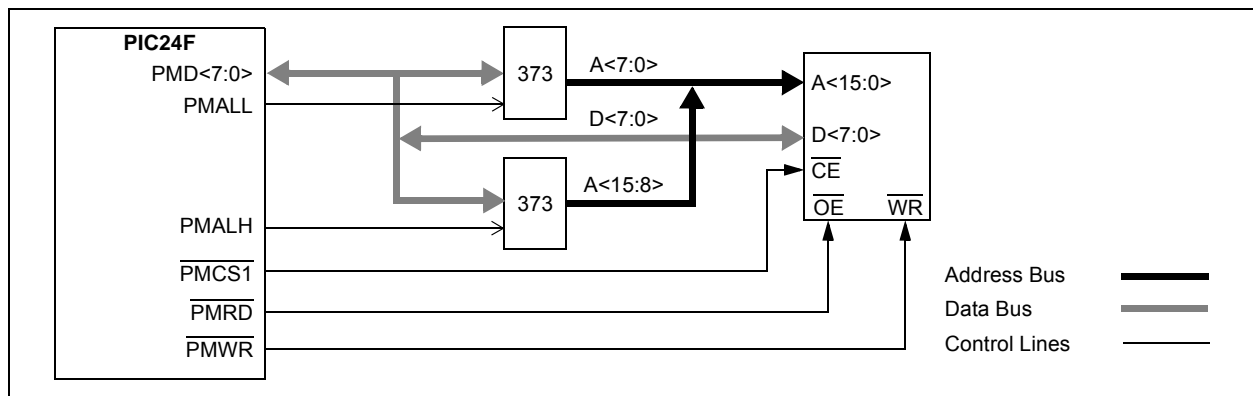


FIGURE 18-7: EXAMPLE OF A MULTIPLEXED ADDRESSING APPLICATION



19.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS39696).

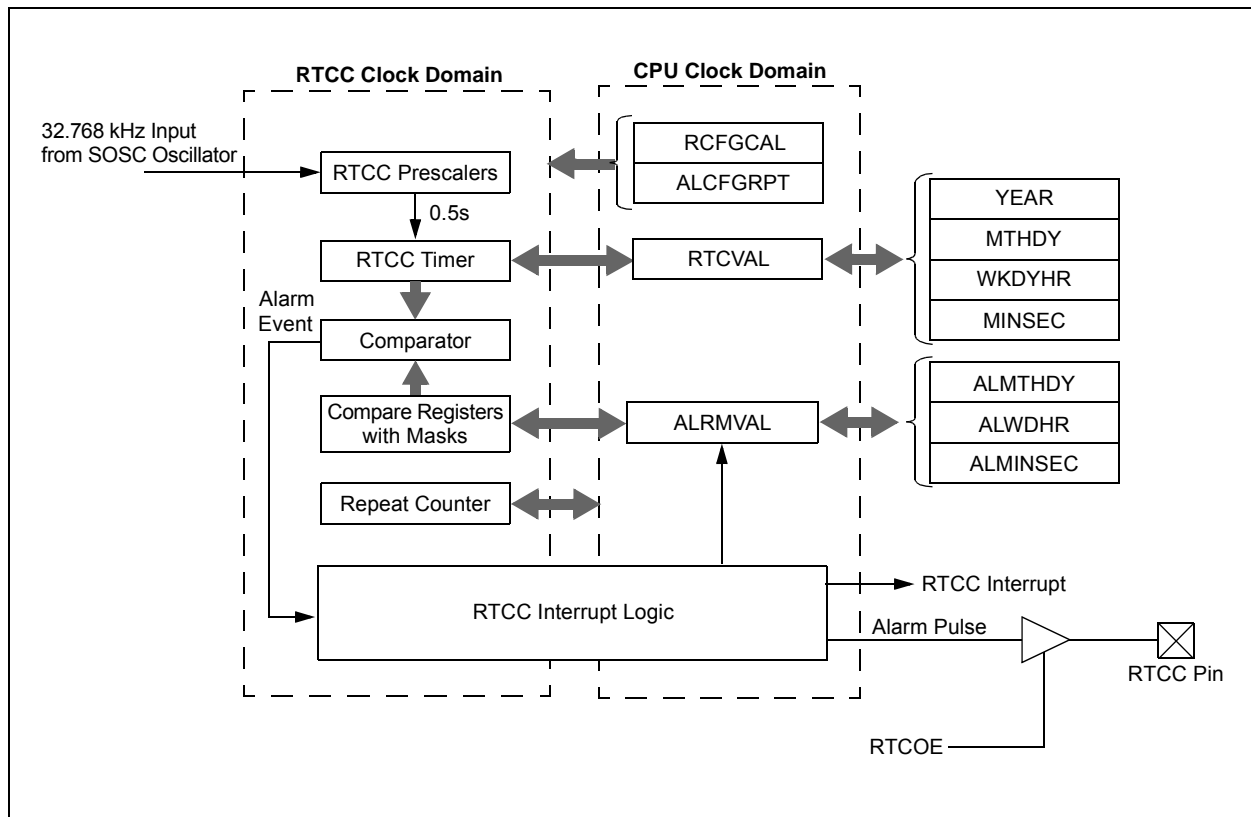
The Real-Time Clock and Calendar (RTCC) provides on-chip, hardware-based clock and calendar functionality with little or no CPU overhead. It is intended for applications where accurate time must be maintained for extended periods with minimal CPU activity and with limited power resources, such as battery-powered applications.

Key features include:

- Time data in hours, minutes and seconds, with a granularity of one-half second
- 24-hour format (military time) display option
- Calendar data as date, month and year
- Automatic, hardware-based day of week and leap year calculations for dates from 2000 through 2099
- Time and calendar data in BCD format for compact firmware
- Highly configurable alarm function
- External output pin with selectable alarm signal or seconds “tick” signal output
- User calibration feature with auto-adjust

A simplified block diagram of the module is shown in [Figure 19-1](#). The SOSC and RTCC will both remain running while the device is held in Reset with MCLR and will continue running after MCLR is released.

FIGURE 19-1: RTCC BLOCK DIAGRAM



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REGISTER 20-2: CRCXOR: CRC XOR POLYNOMIAL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X15	X14	X13	X12	X11	X10	X9	X8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X7	X6	X5	X4	X3	X2	X1	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **X<15:1>**: XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented:** Read as '0'

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TABLE 28-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Typical ⁽¹⁾	Max	Units	Conditions	
Idle Current (IDLE): Core Off, Clock On Base Current, PMD Bits are Set ⁽²⁾					
DC51	4.3	13.0	μA	-40°C	2.0V ⁽³⁾ LPRC (31 kHz)
DC51a	4.5	13.0	μA	+25°C	
DC51b	10	32	μA	+85°C	
DC51c	40	115	μA	+125°C	
DC51d	44	77	μA	-40°C	
DC51e	44	77	μA	+25°C	
DC51f	70	132	μA	+85°C	
DC51g	130	217	μA	+125°C	

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{IDLE} current is measured with core off, clock on, all modules off and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator disabled (ENVREG tied to V_{SS}).

4: On-chip voltage regulator enabled (ENVREG tied to V_{DD}).

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FIGURE 28-6: CLKO AND I/O TIMING CHARACTERISTICS

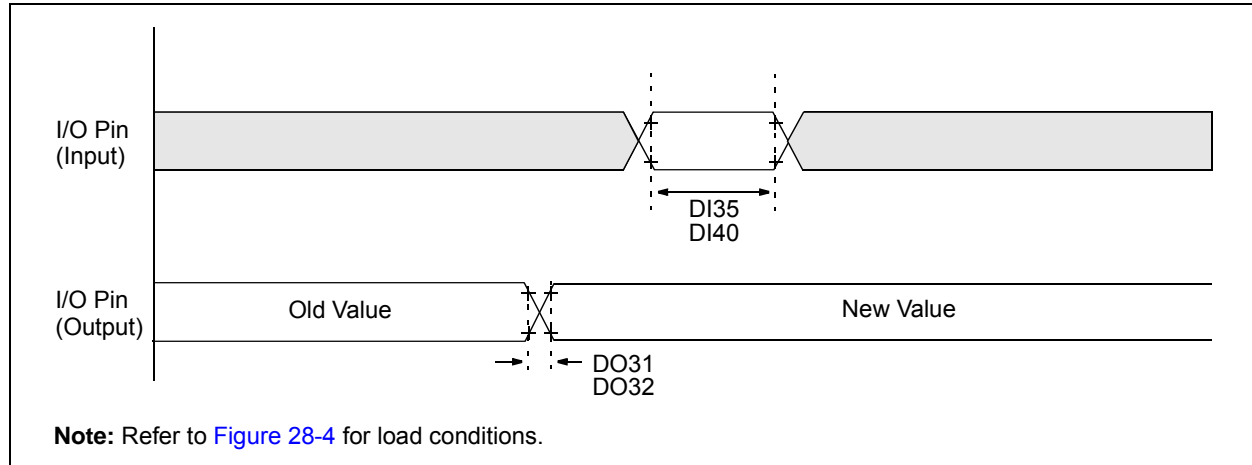


TABLE 28-17: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	
DO32	TioF	Port Output Fall Time	—	10	25	ns	
DI35	TiNP	INTx pin High or Low Time (output)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

TABLE 28-18: RESET SPECIFICATIONS

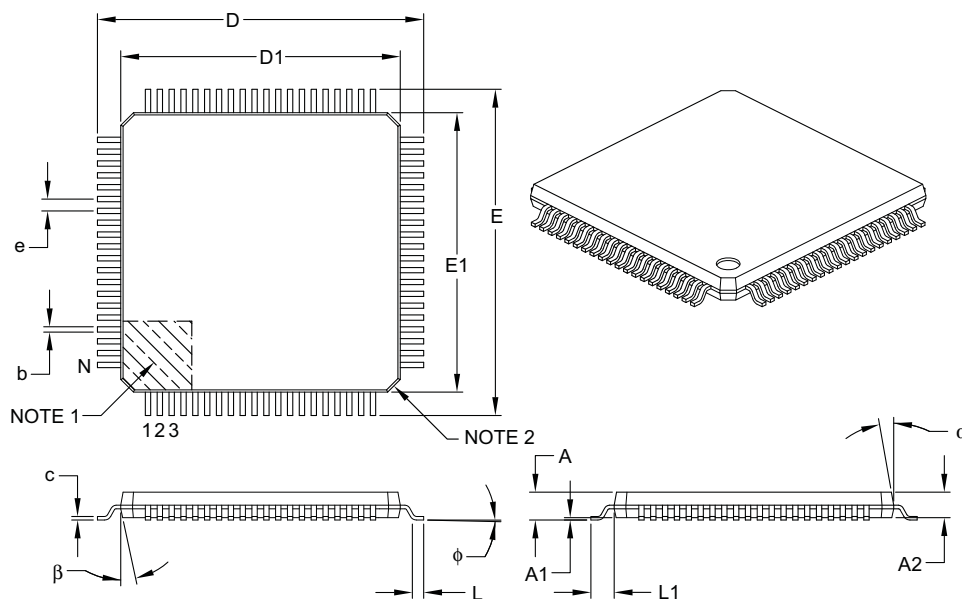
AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)				
		Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
TPOR	Power-up Time	—	2	—	μs	
TRST	Internal State Reset Time	—	50	—	μs	
TPWRT		—	64	—	ms	ENVREG tied to Vss

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

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80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	80		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B