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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga110t-i-pf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 2.2 Power Supply Pins

## 2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1  $\mu$ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu$ F to 0.001  $\mu$ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1  $\mu$ F in parallel with 0.001  $\mu$ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

## 2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7  $\mu$ F to 47  $\mu$ F.

# 2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the  $\overline{\text{MCLR}}$  pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the  $\overline{\text{MCLR}}$  pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the  $\overline{\text{MCLR}}$  pin should be placed within 0.25 inch (6 mm) of the pin.

### FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Overstress (EOS). Ensure that the MCLR pin

VIH and VIL specifications are met.

## TABLE 4-6: TIMER REGISTER MAP

DS39	
905E-	
page	
42	

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100		Timer1 Register										0000					
PR1	0102								Timer1 Peri	iod Registe	r							FFFF
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	_	TSYNC	TCS	_	0000
TMR2	0106								Timer2	Register								0000
TMR3HLD	0108						Timer	3 Holding F	Register (for	32-bit time	r operation:	s only)						0000
TMR3	010A								Timer3	Register								0000
PR2	010C		Timer2 Period Register FFFF								FFFF							
PR3	010E								Timer3 Peri	iod Registe	r							FFFF
T2CON	0110	TON	_	TSIDL	_	_	—		_	_	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_	0000
T3CON	0112	TON	_	TSIDL	_	_	—		_	_	TGATE	TCKPS1	TCKPS0		—	TCS	_	0000
TMR4	0114								Timer4	Register								0000
TMR5HLD	0116						Tim	ner5 Holdin	g Register (	for 32-bit o	perations o	nly)						0000
TMR5	0118								Timer5	Register								0000
PR4	011A								Timer4 Peri	iod Registe	r							FFFF
PR5	011C								Timer5 Peri	iod Registe	r							FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	_	_	TCS	_	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-10: UART REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	_	USIDL	IREN	RTSMD		UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	_	—	_	—	_	—				Tra	nsmit Regist	ter				XXXX
U1RXREG	0226	—	_	—	_	—	_	—				Re	ceive Regist	er				0000
U1BRG	0228							Bau	d Rate Ger	erator Presc	aler							0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	_	_	—	_	—	_				Tra	insmit Regist	ter				xxxx
U2RXREG	0236	—	—	—	—	—	—					Re	ceive Regist	er				0000
U2BRG	0238							Bau	d Rate Ger	erator Presc	aler							0000
U3MODE	0250	UARTEN	_	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0254	—	_	—	—	—	—	_				Tra	nsmit Regist	ter				XXXX
<b>U3RXREG</b>	0256	—	_	—	—	—	—	_				Re	ceive Regist	er				0000
U3BRG	0258							Bau	d Rate Ger	erator Presc	aler							0000
U4MODE	02B0	UARTEN	_	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4							XXXX										
U4RXREG	02B6	—	_	—	_	—	—					Re	ceive Regist	er				0000
U4BRG	02B8	Baud Rate Generator Prescaler 000							0000									
Lanandi		malamaatad	read as 'o'	Depatycelus	a ara ahau	n in hovoda	aimal											

ed, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-11: SPI REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	_	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	_	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	SPIFPOL	_	—	—	—	—	_	—	—	—	—	—	SPIFE	SPIBEN	0000
SPI1BUF	0248							Tra	ansmit and I	Receive Bu	ffer							0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	SPIFPOL	—	—	_	_	—	_	—	—	—	—	_	SPIFE	SPIBEN	0000
SPI2BUF	0268							Tra	ansmit and I	Receive Bu	ffer							0000
SPI3STAT	0280	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI3CON1	0282	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI3CON2	0284	FRMEN	SPIFSD	SPIFPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	SPIBEN	0000
SPI3BUF	0288							Tra	ansmit and I	Receive Bu	ffer							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# 5.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user to erase blocks of eight rows (512 instructions) at a time and to program one row at a time. It is also possible to program single words.

The 8-row erase blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

When data is written to program memory using TBLWT instructions, the data is not written directly to memory. Instead, data written using table writes is stored in holding latches until the programming sequence is executed.

Any number of TBLWT instructions can be executed and a write will be successfully performed. However, 64 TBLWT instructions are required to write the full row of memory.

To ensure that no data is corrupted during a write, any unused addresses should be programmed with FFFFFFh. This is because the holding latches reset to an unknown state, so if the addresses are left in the Reset state, they may overwrite the locations on rows which were not rewritten.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

**Note:** Writing to a location multiple times without erasing is *not* recommended.

All of the table write operations are single-word writes (2 instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

## 5.3 JTAG Operation

The PIC24F family supports JTAG boundary scan. Boundary scan can improve the manufacturing process by verifying pin to PCB connectivity.

## 5.4 Enhanced In-Circuit Serial Programming

Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the program executive, to manage the programming process. Using an SPI data frame format, the program executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

## 5.5 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to **Section 5.6 "Programming Operations"** for further details.

## 5.6 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

	Vector		ΑΙντ	Inte	errupt Bit Locat	ions
Interrupt Source	Number	IVT Address	Address	Flag	Enable	Priority
ADC1 Conversion Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
Comparator Event	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>
CRC Generator	67	00009Ah	00019Ah	IFS4<3>	IEC4<3>	IPC16<14:12>
CTMU Event	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
External Interrupt 3	53	00007Eh	00017Eh	IFS3<5>	IEC3<5>	IPC13<6:4>
External Interrupt 4	54	000080h	000180h	IFS3<6>	IEC3<6>	IPC13<10:8>
I2C1 Master Event	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>
I2C2 Master Event	50	000078h	000178h	IFS3<2>	IEC3<2>	IPC12<10:8>
I2C2 Slave Event	49	000076h	000176h	IFS3<1>	IEC3<1>	IPC12<6:4>
I2C3 Master Event	85	0000BEh	0001BEh	IFS5<5>	IEC5<5>	IPC21<6:4>
I2C3 Slave Event	84	0000BCh	0001BCh	IFS5<4>	IEC5<4>	IPC21<2:0>
Input Capture 1	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Capture 2	5	00001Eh	00011Eh	IFS0<5>	IEC0<5>	IPC1<6:4>
Input Capture 3	37	00005Eh	00015Eh	IFS2<5>	IEC2<5>	IPC9<6:4>
Input Capture 4	38	000060h	000160h	IFS2<6>	IEC2<6>	IPC9<10:8>
Input Capture 5	39	000062h	000162h	IFS2<7>	IEC2<7>	IPC9<14:12>
Input Capture 6	40	000064h	000164h	IFS2<8>	IEC2<8>	IPC10<2:0>
Input Capture 7	22	000040h	000140h	IFS1<6>	IEC1<6>	IPC5<10:8>
Input Capture 8	23	000042h	000142h	IFS1<7>	IEC1<7>	IPC5<14:12>
Input Capture 9	93	0000CEh	0001CEh	IFS5<13>	IEC5<13>	IPC23<6:4>
Input Change Notification	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
LVD Low-Voltage Detect	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC18<2:0>
Output Compare 1	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>
Output Compare 2	6	000020h	000120h	IFS0<6>	IEC0<6>	IPC1<10:8>
Output Compare 3	25	000046h	000146h	IFS1<9>	IEC1<9>	IPC6<6:4>
Output Compare 4	26	000048h	000148h	IFS1<10>	IEC1<10>	IPC6<10:8>
Output Compare 5	41	000066h	000166h	IFS2<9>	IEC2<9>	IPC10<6:4>
Output Compare 6	42	000068h	000168h	IFS2<10>	IEC2<10>	IPC10<10:8>
Output Compare 7	43	00006Ah	00016Ah	IFS2<11>	IEC2<11>	IPC10<14:12>
Output Compare 8	44	00006Ch	00016Ch	IFS2<12>	IEC2<12>	IPC11<2:0>
Output Compare 9	92	0000CCh	0001CCh	IFS5<12>	IEC5<12>	IPC23<2:0>
Parallel Master Port	45	00006Eh	00016Eh	IFS2<13>	IEC2<13>	IPC11<6:4>
Real-Time Clock/Calendar	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>
SPI2 Error	32	000054h	000154h	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Event	33	000056h	000156h	IFS2<1>	IEC2<1>	IPC8<6:4>
SPI3 Error	90	0000C8h	0001C8h	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 Event	91	0000CAh	0001CAh	IFS5<11>	IEC5<11>	IPC22<14:12>

TABLE 7-2:	<b>IMPLEMENTED INTERRUPT VECTORS</b>

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—			_	_		
bit 15	·	·	·	·			bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_	AD1IP2	AD1IP1	AD1IP0		U1TXIP2	U1TXIP1	U1TXIP0
bit 7			•				bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 15-7	Unimplemen	ted: Read as '	o'				
bit 6-4	AD1IP<2:0>:	A/D Conversio	n Complete In	terrupt Priority	bits		
	111 = Interru	ot is priority 7 (l	highest priority	interrupt)			
	•						
	•						
	001 = Interru	ot is priority 1					
	000 = Interru	ot source is dis	abled				
bit 3	Unimplemen	ted: Read as '	o'				
bit 2-0	U1TXIP<2:0>	: UART1 Trans	smitter Interrup	ot Priority bits			
	111 = Interru	ot is priority 7 (I	highest priority	interrupt)			
	•						
	•						
	•	at is priority 1					
	001 = Interru	ot is priority. I at source is dis	abled				
			abiou				

## REGISTER 7-20: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
_	_		_	_	INT4IP2	INT4IP1	INT4IP0
bit 15				·		•	bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	INT3IP2	INT3IP1	INT3IP0	_	_	_	_
bit 7			•	·			bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 15-11	Unimplemen	ted: Read as '	כי				
bit 10-8	INT4IP<2:0>:	External Interr	upt 4 Priority b	oits			
	111 = Interru	pt is priority 7 (I	nighest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	abled				
bit 7	Unimplemen	ted: Read as '	כי				
bit 6-4	INT3IP<2:0>:	External Interr	upt 3 Priority b	oits			
	111 = Interru	pt is priority 7 (I	nighest priority	interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	abled				
bit 3-0	Unimplemen	ted: Read as '	י)				

## REGISTER 7-30: IPC13: INTERRUPT PRIORITY CONTROL REGISTER 13

## 10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

## 10.2 Configuring Analog Port Pins

The AD1PCFGL and TRIS registers control the operation of the A/D port pins. Setting a port pin as an analog input also requires that the corresponding TRIS bit be set. If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

## 10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

# 10.2.2 ANALOG INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins are always to be avoided. Table 10-1 summarizes the input capabilities. Refer to **Section 28.1 "DC Characteristics"** for more details.

**Note:** For easy identification, the pin diagrams at the beginning of this data sheet also indicate 5.5V tolerant pins with dark grey shading.

TABLE 10-1:

INPUT VOLTAGE LEVELS<sup>(1)</sup>

Port or Pin	Tolerated Input	Description
PORTA<10:9>	Vdd	Only VDD input
PORTB<15:0>		levels tolerated.
PORTC<15:12>		
PORTD<7:6>		
PORTF<0>		
PORTG<9:6>		
PORTA<15:14>,	5.5V	Tolerates input
PORTA<7:0>		levels above
PORTC<4:1>		VDD, useful for
PORTD<15:8>,		most standard
PORTD<5:0>		logic.
PORTE<9:0>		
PORTF<13:12>,		
PORTF<8:1>		
PORTG<15:12>,		
PORIG<3:0>		

Note 1: Not all port pins shown here are implemented on 64-pin and 80-pin devices. Refer to Section 1.0 "Device Overview" to confirm which ports are available in specific devices.

## EXAMPLE 10-1: PORT WRITE/READ EXAMPLE

MOV 0xFF00, W0 MOV W0, TRISB NOP BTSS PORTB, #13 ; Configure PORTB<15:8> as inputs
; and PORTB<7:0> as outputs

- ; Delay 1 cycle
- ; Next Instruction

Input Name	Function Name	Register	Function Mapping Bits
External Interrupt 1	INT1	RPINR0	INT1R<5:0>
External Interrupt 2	INT2	RPINR1	INT2R<5:0>
External Interrupt 3	INT3	RPINR1	INT3R<5:0>
External Interrupt 4	INT4	RPINR2	INT4R<5:0>
Input Capture 1	IC1	RPINR7	IC1R<5:0>
Input Capture 2	IC2	RPINR7	IC2R<5:0>
Input Capture 3	IC3	RPINR8	IC3R<5:0>
Input Capture 4	IC4	RPINR8	IC4R<5:0>
Input Capture 5	IC5	RPINR9	IC5R<5:0>
Input Capture 6	IC6	RPINR9	IC6R<5:0>
Input Capture 7	IC7	RPINR10	IC7R<5:0>
Input Capture 8	IC8	RPINR10	IC8R<5:0>
Input Capture 9	IC9	RPINR15	IC9R<5:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<5:0>
Output Compare Fault B	OCFB	RPINR11	OCFBR<5:0>
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R<5:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<5:0>
SPI1 Slave Select Input	SS1IN	RPINR21	SS1R<5:0>
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R<5:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<5:0>
SPI2 Slave Select Input	SS2IN	RPINR23	SS2R<5:0>
SPI3 Clock Input	SCK3IN	RPINR23	SCK3R<5:0>
SPI3 Data Input	SDI3	RPINR28	SDI3R<5:0>
SPI3 Slave Select Input	SS3IN	RPINR29	SS3R<5:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<5:0>
Timer4 External Clock	T4CK	RPINR4	T4CKR<5:0>
Timer5 External Clock	T5CK	RPINR4	T5CKR<5:0>
UART1 Clear To Send	U1CTS	RPINR18	U1CTSR<5:0>
UART1 Receive	U1RX	RPINR18	U1RXR<5:0>
UART2 Clear To Send	U2CTS	RPINR19	U2CTSR<5:0>
UART2 Receive	U2RX	RPINR19	U2RXR<5:0>
UART3 Clear To Send	U3CTS	RPINR21	U3CTSR<5:0>
UART3 Receive	U3RX	RPINR17	U3RXR<5:0>
UART4 Clear To Send	U4CTS	RPINR27	U4CTSR<5:0>
UART4 Receive	U4RX	RPINR27	U4RXR<5:0>

# TABLE 10-2: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)<sup>(1)</sup>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.



## FIGURE 12-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM

3: The ADC event trigger is available only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode.



FIGURE 12-3: TIMER3 AND TIMER5 (16-BIT ASYNCHRONOUS) BLOCK DIAGRAM



# 14.0 OUTPUT COMPARE WITH DEDICATED TIMER

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, Section 35. "Output Compare with Dedicated Timer" (DS39723)

Devices in the PIC24FJ256GA110 family all feature 9 independent enhanced output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the enhanced output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 30 user-selectable trigger/sync sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

# 14.1 General Operating Modes

## 14.1.1 SYNCHRONOUS AND TRIGGER MODES

By default, the enhanced output compare module operates in a free-running mode. The internal, 16-bit counter, OCxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow, with its period synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs. In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-running mode is selected by default, or any time that the SYNCSEL bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSEL bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSEL bits determine the sync/trigger source.

## 14.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-Bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, modules 1 and 2 are paired, as are modules 3 and 4, and so on.) The odd-numbered module (OCx) provides the Least Significant 16 bits of the 32-bit register pairs, and the even module (OCy) provides the Most Significant 16 bits. Wraparounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bits (OCxCON2<8>) for both modules.



### FIGURE 14-2: OUTPUT COMPARE BLOCK DIAGRAM (DOUBLE-BUFFERED, 16-BIT PWM MODE)

### 14.3.1 PWM PERIOD

The PWM period is specified by writing to PRy, the Timer Period register. The PWM period can be calculated using Equation 14-1.

### EQUATION 14-1: CALCULATING THE PWM PERIOD<sup>(1)</sup>

PWM Period =  $[(PRy) + 1] \bullet TCY \bullet (Timer Prescale Value)$ 

where: PWM Frequency = 1/[PWM Period]

- **Note 1:** Based on TCY = TOSC \* 2, Doze mode and PLL are disabled.
- Note: A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7 written into the PRy register will yield a period consisting of 8 time base cycles.

### 14.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 14-1 for PWM mode timing details. Table 14-1 and Table 14-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

# 17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:	This data sheet summarizes the features of
	this group of PIC24F devices. It is not
	intended to be a comprehensive reference
	source. For more information, refer to the
	"PIC24F Family Reference Manual",
	Section 21. "UART" (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA<sup>®</sup> encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- · One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins

- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- · Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- · IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UART is shown in Figure 17-1. The UART module consists of these key important hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver





## REGISTER 23-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
_	—		—	—	—	—	—		
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own		
bit 15-8	Unimplemen	ted: Read as 'o	)'						
bit 7	CVREN: Com	nparator Voltage	e Reference E	nable bit					
	1 = CVREF ci	rcuit powered c	n						
<b>h</b> # 0		rcuit powered c	IOWN	L :4					
DIT 6				DIC					
	1 = CVREF VC 0 = CVREF VC	oltage level is d	isconnected fr	om CVREF pin					
bit 5	CVRR: Comparator VREF Range Selection bit								
	1 = CVRSRC	range should b	e 0 to 0.625 C	VRSRC with CVF	RSRC/24 step s	ize			
	0 = CVRSRC	range should b	e 0.25 to 0.719	OVRSRC with	CVRSRC/32 ste	p size			
bit 4	CVRSS: Com	parator VREF S	ource Selection	on bit					
	1 = Compara	tor reference s	ource, CVRSRO	C = VREF+ – VRI	EF-				
	0 = Compara	itor reference s		c = AVDD – AVS	S				
bit 3-0	CVR<3:0>: C	omparator VRE	F Value Select	ion, $0 \le CVR < 3$	$:0> \le 15$ , bits				
	CVREF = (CVI	<u>= 1:</u> R<3:0>/ 24) ● ((	CVRSRC)						
	When CVRR	= 0:							
	$CVREF = 1/4 \bullet (CVRSRC) + (CVR<3:0>/32) \bullet (CVRSRC)$								

## REGISTER 24-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 3-2
   EDG1SEL<1:0>: Edge 1 Source Select bits

   11 = CTED1 pin
   10 = CTED2 pin

   01 = OC1 module
   00 = Timer1 module

   bit 1
   EDG2STAT: Edge 2 Status bit

   1 = Edge 2 event has occurred
   0 = Edge 2 event has not occurred

   bit 0
   EDG1STAT: Edge 1 Status bit

   1 = Edge 1 event has occurred
   0 = Edge 1 event has not occurred
- **Note 1:** If TGEN = 1, the CTEDGx inputs and CTPLS outputs must be assigned to available RPn pins before use. See **Section 10.4 "Peripheral Pin Select"** for more information.

REGISTER 24-2:	<b>CTMUICON: CTMU CURRENT CONTROL REGISTE</b>	R

	_							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	_	_	—	—	—	—	_	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-10 ITRIM<5:0>: Current Source Trim bits 01111 = Maximum positive change from nominal current 01110 000001 = Minimum positive change from nominal current 000000 = Nominal current output specified by IRNG<1:0> 111111 = Minimum negative change from nominal current 100010 100001 = Maximum negative change from nominal current								
bit 9-8 bit 7-0	IRNG<1:0>:0 11 = 100 × Ba 10 = 10 × Ba 01 = Base cu 00 = Current Unimplemen	Current Source ase Current se Current Irrent level (0.55 source disable ited: Read as '0	Range Select 5 μA nominal) d	bits				

## 26.0 INSTRUCTION SET SUMMARY

**Note:** This chapter is a brief summary of the PIC24F instruction set architecture, and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC<sup>®</sup> MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- · Literal operations
- Control operations

Table 26-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 26-2 lists all of the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, 'Wb', without any address modifier
- The second source operand, which is typically a register, 'Ws', with or without an address modifier
- The destination of the result, which is typically a registe,r 'Wd', with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, 'f'
- The destination, which could either be the file register, 'f', or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, 'Wb', without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The control instructions may use some of the following operands:

- · A program memory address
- The mode of the table read and table write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles.

Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

TADLE 20-7:	DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)						
		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise s					
DC CHARACTI	ERISTICS	Operating temperature	-40°C < TA < +85°C for Industrial				

CUADACTEDICTICS, 1/0 DIN INDUT ODECIFICATIONS (CONTINUED)

DC CHARACTERISTICS		Operating temperature		$\label{eq:constraint} \begin{array}{l} -40^\circ C \leq TA \leq +85^\circ C \text{ for Industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \text{ for Extended} \end{array}$				
Param No.	Sym	Characteristic	Min	Min Typ <sup>(1)</sup>		Units	Conditions	
	lı∟	Input Leakage Current <sup>(2,3)</sup>						
DI50		I/O Ports	—	—	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &VSS \leq VPIN \leq VDD, \\ &Pin \ at \ high-impedance \end{split}$	
DI51		Analog Input Pins	—	_	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &P{\rm in \ at \ high-impedance} \end{split}$	
DI55		MCLR	—	—	<u>+</u> 1	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$	
DI56		OSC1	_	-	<u>+</u> 1	μA	VSS $\leq$ VPIN $\leq$ VDD, XT and HS modes	

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-4 for I/O pins buffer types.

5: VIH requirements are met when internal pull-ups are enabled.

## TABLE 28-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Sym	Characteristic	Min	Typ <sup>(1)</sup>	Мах	Units	Conditions
	Vol	Output Low Voltage					
DO10		I/O Ports	—	_	0.4	V	IOL = 8.5 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 6.0 mA, VDD = 2.0V
DO16		OSC2/CLKO	—	—	0.4	V	IOL = 8.5 mA, VDD = 3.6V
					0.4	V	IOL = 6.0 mA, VDD = 2.0V
	Vон	Output High Voltage					
DO20		I/O Ports	3.0	_	—	V	Юн = -3.0 mA, VDD = 3.6V
			2.4	_	—	V	Юн = -6.0 mA, VDD = 3.6V
			1.65	_	—	V	Юн = -1.0 mA, VDD = 2.0V
			1.4	—	—	V	Юн = -3.0 mA, VDD = 2.0V
DO26		OSC2/CLKO	2.4	—	—	V	Юн = -6.0 mA, VDD = 3.6V
			1.4		—	V	ЮН = -3.0 mA, VDD = 2.0V

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

- 3: Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-4 for I/O pins buffer types.
- **5:** VIH requirements are met when internal pull-ups are enabled.

## FIGURE 28-10: INPUT CAPTURE TIMINGS



## TABLE 28-23: INPUT CAPTURE

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time –	No Prescaler	Tcy + 20	_	ns	Must also meet parameter IC15
		Synchronous Timer	With Prescaler	20	-	ns	
IC11	IC11 TccH	ICx Input Low Time – Synchronous Timer	No Prescaler	Tcy + 20	-	ns	Must also meet
			With Prescaler	20	_	ns	parameter IC15
IC15	TccP	ICx Input Period – Synchronous Timer		<u>2 * Tcy + 40</u> N	—	ns	N = prescale value (1, 4, 16)

NOTES: