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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2810ag20ag

Table 5. ZNEO CPU Control Registers

Address (Hex)	Register Description	Register Mnemonic
FF_E004-FF_E007	Program counter overflow	PCOV
FF_E00C-FF_E00F	Stack pointer overflow	SPOV
FF_E010	Flags	FLAGS
FF_E012	CPU control	CPUCTL

External Memory

Many ZNEO CPU products support external data and address buses for connecting to additional external memories and/or memory-mapped peripherals. The external addresses are used for storing program code, data, constants and stack, etc. Attempts to read from or write to unavailable external addresses is undefined.

Endianness

The ZNEO CPU accesses data in big endian order, that is, the address ofa multi-byte word or quad points to the most significant byte. Figure 7 displays the Endianness of the ZNEO CPU.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
Timers: Base Address = FFF_E300				
Timer 0 (General-Purpose Timer) Base Address = FF_E300				
FF_E300	Timer 0 High Byte	T0H	00	107
FF_E301	Timer 0 Low Byte	T0L	01	107
FF_E302	Timer 0 Reload High Byte	T0RH	FF	108
FF_E303	Timer 0 Reload Low Byte	T0RL	FF	108
FF_E304	Timer 0 PWM High Byte	T0PWMH	00	109
FF_E305	Timer 0 PWM Low Byte	T0PWML	00	109
FF_E306	Timer 0 Control 0	T0CTL0	00	110
FF_E307	Timer 0 Control 1	T0CTL1	00	111
Timer 1 (General-Purpose Timer) Base Address = FF_E310				
FF_E310	Timer 1 High Byte	T1H	00	107
FF_E311	Timer 1 Low Byte	T1L	01	107
FF_E312	Timer 1 Reload High Byte	T1RH	FF	108
FF_E313	Timer 1 Reload Low Byte	T1RL	FF	108
FF_E314	Timer 1 PWM High Byte	T1PWMH	00	109
FF_E315	Timer 1 PWM Low Byte	T1PWML	00	109
FF_E316	Timer 1 Control 0	T1CTL0	00	110
FF_E317	Timer 1 Control 1	T1CTL1	00	111
Timer 2 (General-Purpose Timer) Base Address = FF_E320				
FF_E320	Timer 2 High Byte	T2H	00	107
FF_E321	Timer 2 Low Byte	T2L	01	107
FF_E322	Timer 2 Reload High Byte	T2RH	FF	108
FF_E323	Timer 2 Reload Low Byte	T2RL	FF	108
FF_E324	Timer 2 PWM High Byte	T2PWMH	00	109
FF_E325	Timer 2 PWM Low Byte	T2PWML	00	109
FF_E326	Timer 2 Control 0	T2CTL0	00	110
FF_E327	Timer 2 Control 1	T2CTL1	00	111
Pulse Width Modulator (PWM) Base Address = FF_E380				
FF_E380	PWM Control 0	PWMCTL0	00	125
FF_E381	PWM Control 1	PWMCTL1	00	126
FF_E382	PWM Deadband	PWMDB	00	127

XX = Undefined.

External Interface Timing

The following sections describe the ZNEO Z16F Series MCU's external interface timing.

External Interface Write Timing, Normal Mode

Figure 11 and Table 14 provide timing information for the external interface performing a write operation. In Figure 11, it is assumed that the wait state generator is configured to provide 1 wait state during write operations. The external $\overline{\text{WAIT}}$ input pin is generating an additional Wait period. It is assumed in Figure 11 that the chip select ($\overline{\text{CS}}$) signal has been configured for active Low operation. Though the internal system clock is not provided as an external signal, it provides a useful reference for control signal events.

Note: At the completion of a Write cycle, the deassertion of the $\overline{\text{WR}}$ signal is fed back from the pin and used on chip to control the deassertion of the data, $\overline{\text{CS}}$, address and byte enable signals to assure proper timing of the data hold.

Table 14. External Interface Timing for a Write Operation, Normal Mode

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
T_1	SYS CLK Rise to Address Valid Delay		10
T_2	$\overline{\text{WR}}$ Rise to Address Output Hold Time	3	
T_3	SYS CLK Rise to Data Valid Delay		10
T_4	$\overline{\text{WR}}$ Rise to Data Output Hold Time	3	
T_5	SYS CLK Rise to $\overline{\text{CS}}$ Assertion Delay		10
T_6	$\overline{\text{WR}}$ Rise to $\overline{\text{CS}}$ Deassertion Hold Time	3	
T_7	SYS CLK Rise to $\overline{\text{WR}}$ Assertion Delay		$1/2T_{CLK}$ +10
T_8	SYS CLK Rise to $\overline{\text{WR}}$ Deassertion Hold Time	3	
T_9	$\overline{\text{WAIT}}$ Input Pin Assertion to X_{IN} Rise Setup Time	1	
T_{10}	$\overline{\text{WAIT}}$ Input Pin Deassertion to X_{IN} Rise Setup Time	1	
T_{11}	SYS CLK Rise to $\overline{\text{DMAACK}}$ Assertion Delay		10
T_{12}	SYS CLK Rise to $\overline{\text{DMAACK}}$ Deassertion Hold Time	3	
T_{13}	SYS CLK Rise to $\overline{\text{BHEN}}$ or $\overline{\text{BLEN}}$ Assertion Delay		10
T_{14}	$\overline{\text{WR}}$ Rise to $\overline{\text{BHEN}}$ or $\overline{\text{BLEN}}$ Deassertion Hold Time	3	

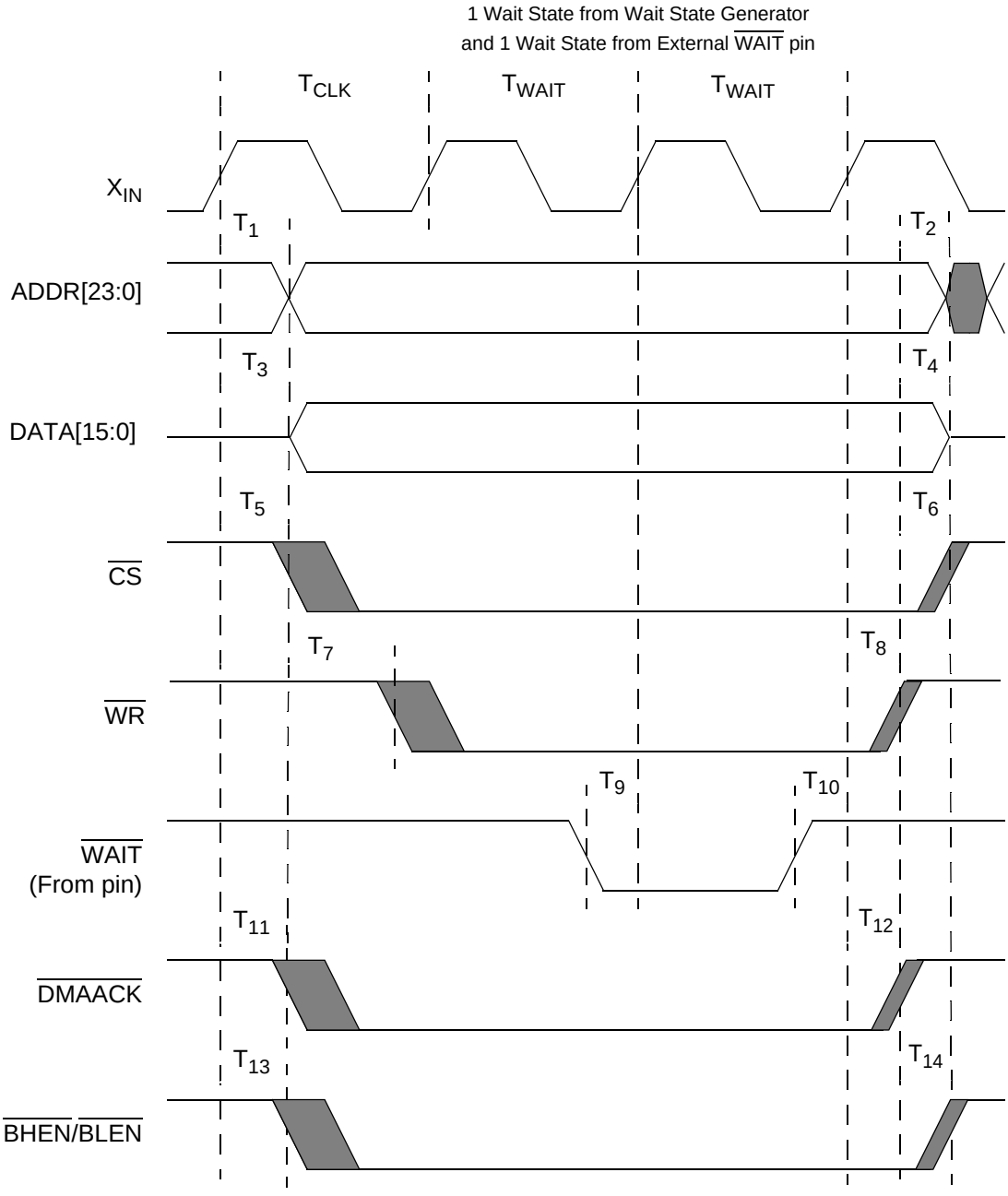


Figure 11. External Interface Timing for a Write Operation, Normal Mode

PWM Minimum Pulse Width Filter

The value in the PWMMPF Register, shown in Table 73, determines the minimum width pulse, either High or Low, generated by the PWM module. The minimum pulse width period is calculated as:

$$T_{minPulseOut} = \frac{PWMDB + PWMMPF}{T_{systemClock} \cdot PwmPrescale}$$

Table 73. PWM Minimum Pulse Width Filter (PWMMPF)

Bits	7	6	5	4	3	2	1	0
Field	PWMMPF[7:0]							
RESET	00h							
R/W	R/W							
Addr	FF_E383h							

Bit	Description
[7:0] PWMDB[7:0]	**Minimum Pulse Filter** Sets the minimum allowed output pulse width in PWM clock cycles.

Note: This register can only be written when PWMEN is cleared.

PWM Fault Mask Register

The PWM Fault Mask Register, shown in Table 74, enables individual fault sources. When an input is asserted, PWM behavior is determined by the PWM Fault Control Register (PWMFCTL). The Comparator 0–3 outputs generate PWM faults and the associated fault system exception. The bits in this register can only be set; all other writes are ignored.

asynchronous data format employed by the LIN-UART, without parity and with parity, respectively.

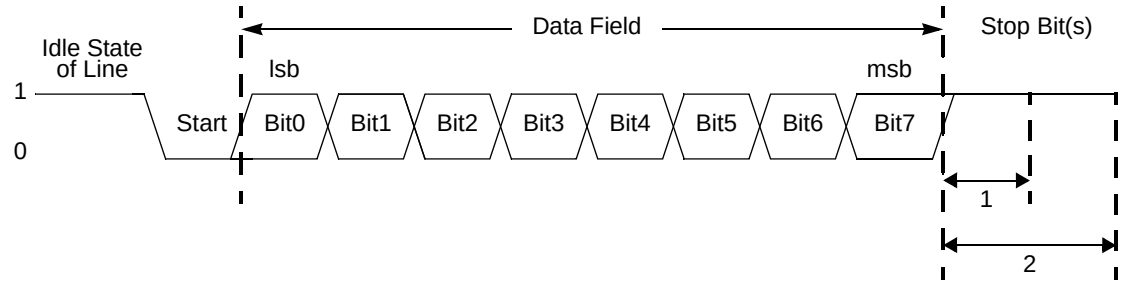


Figure 25. LIN-UART Asynchronous Data Format without Parity

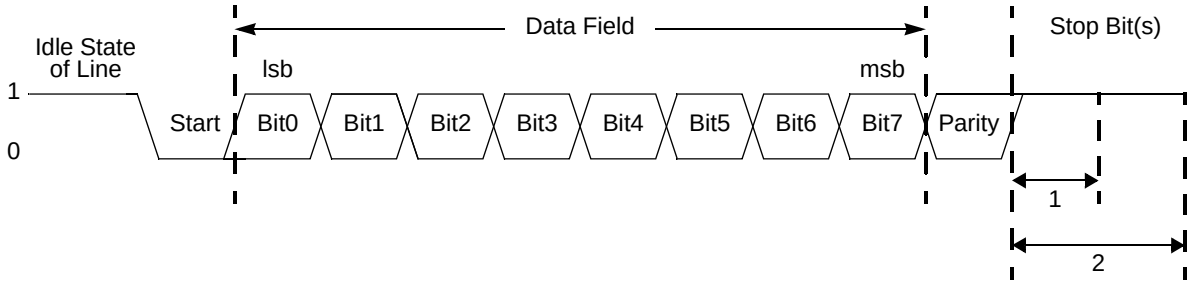


Figure 26. LIN-UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Observe the following steps to transmit data using the polled operating method:

1. Write to the LIN-UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the LIN-UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. If Multiprocessor Mode is required, write to the LIN-UART Control 1 Register to enable MULTIPROCESSOR (9-Bit) Mode functions by setting the Multiprocessor Mode select bit (MPEN) to enable Multiprocessor Mode.
4. Write to the LIN-UART Control 0 Register to:
   a. Set the transmit enable bit (TEN) to enable the LIN-UART for data transmission.

Table 96. LIN-UART Baud Rates (Continued)

5.5296 MHz System Clock				3.579545 MHz System Clock			
Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	345.6	38.24	250.0	1	223.72	–10.51
115.2	3	115.2	0.00	115.2	2	111.9	–2.90
57.6	6	57.6	0.00	57.6	4	55.9	–2.90
38.4	9	38.4	0.00	38.4	6	37.3	–2.90
19.2	18	19.2	0.00	19.2	12	18.6	–2.90
9.60	36	9.60	0.00	9.60	23	9.73	1.32
4.80	72	4.80	0.00	4.80	47	4.76	–0.83
2.40	144	2.40	0.00	2.40	93	2.41	0.23
1.20	288	1.20	0.00	1.20	186	1.20	0.23
0.60	576	0.60	0.00	0.60	373	0.60	–0.04
0.30	1152	0.30	0.00	0.30	746	0.30	–0.04

Slave Select

The $\overline{SS}$ signal is a bidirectional framing signal with several modes of operation to support SPI and other synchronous serial interface protocols. The Slave Select Mode is selected by the SSMD field of the ESPI Mode Register. The direction of the $\overline{SS}$ signal is controlled by the SSIO bit of the ESPI Mode Register. The $\overline{SS}$ signal is an input on slave devices and is an output on the active master device. Slave devices ignore transactions on the bus unless their slave select input is asserted. In SPI Master Mode, additional GPIO pins are required to provide Slave Selects if there is more than one slave device.

ESPI Register Overview

The ESPI Control/Status Registers are summarized in Table 97. These registers are accessed by either Word (16-bit) or Byte operations.

Table 97. ESPI Registers

Word Address	Even Address	Odd Address
XXXXX0	Data	Transmit Data Command
XXXXX2	Control	Mode
XXXXX4	Status	State
XXXXX6	Baud Rate High	Baud Rate Low

Comparison with Basic SPI Block

The ESPI module includes many enhancements when compared to the simpler SPI module in other Z8 Encore!® parts. This section highlights the differences between the ESPI module and the SPI module as follows:

- Transmit and receive data buffer register added to support higher performance.
- Multiple interrupt sources (transmit data, receive data, errors). SPI module only has data transfer complete interrupt.
- DMA Controller interface (separate transmit and receive interfaces).
- Register addresses redefined to facilitate 16-bit transfers on the ZNEO® Z16F Series.
- Transmit data command register – new register to facilitate DMA interface and improve performance with 16-bit transfers. SSV and TEOF is set on same cycle on which the data register is written.
- Control register:
  - IRQE changed to DIRQE. This allows data interrupts to be disabled when using DMA but still allow error interrupts.

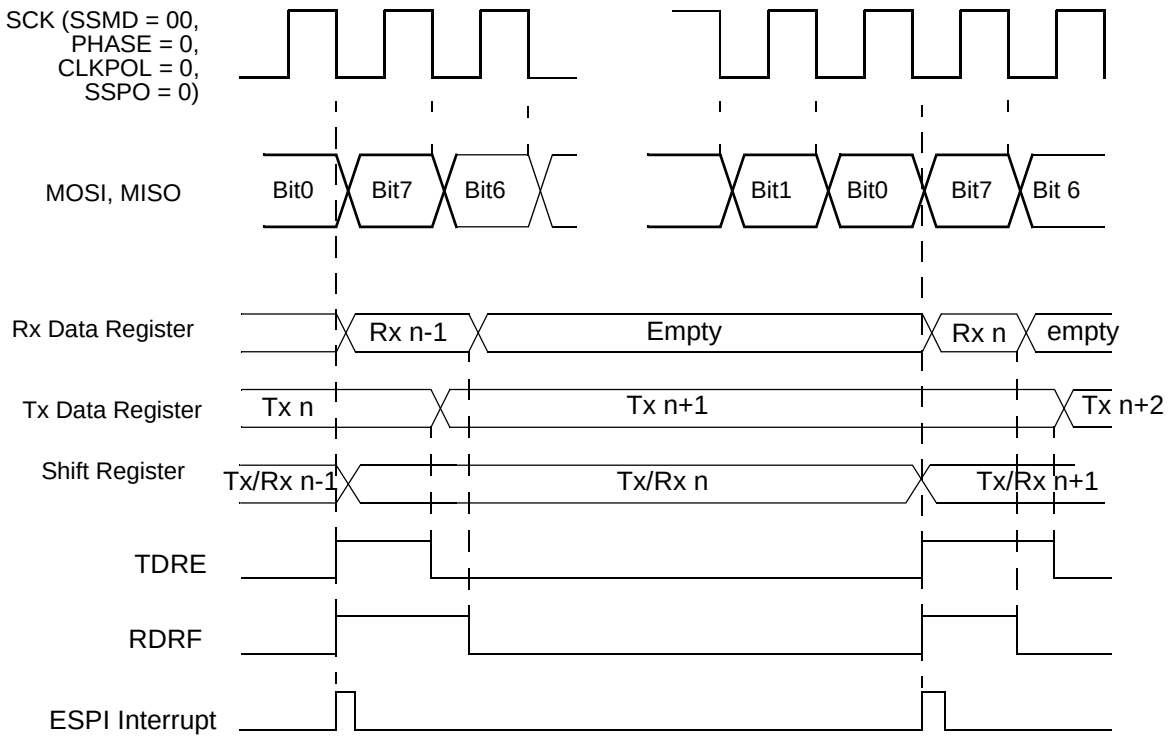


Figure 38. SPI Mode (SSMD = 000)

I2S (Inter-IC Sound) Mode

This mode is selected by setting the SSMD field of the mode register to 010. The PHASE and CLKPOL bits of the control register must be set to 0. This mode is illustrated in Figure 39 with $\overline{SS}$ alternating between consecutive frames. A frame consists of a fixed number of data bytes as defined in the DMA buffer descriptor or by software. I^2S (Inter-IC Sound) mode is typically used to transfer left or right channel audio data.

The SSV indicates whether the corresponding bytes are left or right channel data. The SSV value must be updated when servicing the TDRE interrupt/request for the first byte in a left or write channel frame. This update is accomplished by performing a word write when writing the first byte of the audio word, which updates both the ESPI data and transmit data command words or by doing a byte write to update SSV followed by a byte write to the data register. The $\overline{SS}$ signal leads the data by one SCK period.

If a DMA Channel is controlling data transfer, each sequence of left (or right) channel byte is considered a frame with a buffer descriptor. The SSV bit is defined in the buffer descriptor command field and is automatically written to the transmit data command register just prior to or in synchronous with the first data byte of the frame being written. Note that the

Table 108. ESPISTATE Values and Description (Continued)

ESPISTATE Value	Description
10_1100	Bit 6 Receive
10_1101	Bit 6 Transmit
10_1010	Bit 5 Receive
10_1011	Bit 5 Transmit
10_1000	Bit 4 Receive
10_1001	Bit 4 Transmit
10_0110	Bit 3 Receive
10_0111	Bit 3 Transmit
10_0100	Bit 2 Receive
10_0101	Bit 2 Transmit
10_0010	Bit 1 Receive
10_0011	Bit 1 Transmit
10_0000	Bit 0 Receive
10_0001	Bit 0 Transmit

ESPI Baud Rate High and Low Byte Registers

The ESPI Baud Rate High and Low Byte registers, shown in Tables 109 and 110, combine to form a 16-bit reload value, BRG[15:0], for the ESPI Baud Rate Generator. The ESPI baud rate is calculated using the following equation:

$$\text{SPI Baud Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG}[15:0]}$$

Minimum baud rate is obtained by setting BRG[15:0] to 0000h for a clock divisor value of (2 x 65536 = 131072)

When the ESPI function is disabled, the BRG functions as a basic 16-bit timer with interrupt on time-out.

Observe the following procedure to configure the BRG as a general purpose timer with interrupt on time-out:

1. Disable the ESPI by setting ESPIEN[1:0] = 00 in the SPI Control register.
2. Load the appropriate 16-bit count value into the ESPI Baud Rate High and Low Byte registers.
3. Enable the BRG timer function and associated interrupt by setting the BRGCTL bit in the ESPI Control register to 1.

tion is complete, the Flash Controller returns to its locked state. Only pages located in unprotected sectors are erased.

The four steps to performing a Page Erase operation are:

1. Write the page to be erased to the Flash Page Select Register.
2. Write the first unlock command 73h to the Flash Command Register.
3. Write the second unlock command 8Ch to the Flash Command Register.
4. Write the Page Erase command 95h to the Flash Command Register.

Mass Erase

The Flash memory cannot be Mass Erased by user code.

Flash Controller Bypass

The Flash Controller is bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Programming algorithms by controlling the Flash programming signals directly.

Flash Controller Bypass is recommended for large volume gang programming applications, which do not require in-circuit programming of the Flash memory.

Flash Controller Behavior using the On-Chip Debugger

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Controller does not have to be unlocked for program and erase operations.
- The Flash Write Protect option bit is ignored.
- The Flash Sector Protect register is ignored for programming and erase operations.
- Programming operations are not limited to the page selected in the Flash Page Select Register.
- Bits in the Flash Sector Protect register is written to 1 or 0.
- The Flash Page Select Register is written when the Flash Controller is unlocked.
- The Mass Erase command is enabled.

Bit	Description (Continued)
[6] LPOPT	**Low Power Option** 0 = The part will come up in low power mode. The Clock is divided by 8 and Flash memory will only be accessed the last half of the last cycle of the divide. This reduces Flash power consumption. 1 = The part will come up normally.
[5:0]	**Reserved** These option bits are reserved for future use and must always be 1. This setting is the default for unprogrammed (erased) Flash.

Information Area

Data in the information area of memory cannot be altered directly. If you wish to alter the factory settings, it must be done by writing to the Register Address identified. The part defaults to the factory settings after reset and the registers must be rewritten to have the user settings in effect. Read the information area address to determine the factory settings.

IPO Trim Registers (Information Area Address 0021h and 0022h)

Tables 165 and 166 define the IPO Trim settings, which are altered after reset by accessing the IPOTRIM1 and IPOTRIM2 registers.

Table 165. IPO Trim 1 (IPOTRIM1)

Bits	7	6	5	4	3	2	1	0
Field	IPO TEMP TRIM						IPO TRIM	
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF25h							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

Table 166. IPO Trim 2 (IPOTRIM2)

Bits	7	6	5	4	3	2	1	0
Field	IPO TRIM							
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF26							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

On-Chip Debugger

The ZNEO® Z16F Series products have an integrated On-Chip Debugger (OCD) that provides the following features:

- Reading and writing memory
- Reading and writing CPU registers
- Execution of CPU instructions
- In-circuit programming and erasing of the Flash
- Unlimited number of software breakpoints
- Four hardware breakpoints
- Instruction execution trace
- Single-pin serial communication interface

Architecture

The OCD consists of two main blocks: the transmitter/receiver unit and the debug control logic. Figure 62 displays the architecture of the OCD.

Bit	Description (Continued)
[5:4]	**Reserved** These bits are reserved and must be programmed to 00.
[3] CRCEN	**CRC Enable** If this bit is set, a CRC is appended to the end of each debug command. Clearing this bit will disable transmission of the CRC. 0 = CRC disabled 1 = CRC enabled
[2] UARTEN	**UART Enable** This bit is used to enable or disable the UART. This bit is ignored when OCDEN is set. 0 = UART Disabled. 1 = UART Enabled.
[1] ABCHAR	**Auto-Baud Character** This bit selects the character used during auto-baud detection. This bit cannot be written by the CPU if OCDEN is set. 0 = Auto-baud character to be measured is 80h. 1 = Auto-baud character to be measured is 0Dh.
[0] ABSRCH	**Auto-Baud Search Mode** This bit enables auto-baud search mode. When this bit is set, the next character received is measured to set the Baud Rate Reload register. This bit clears itself to 0 after the reload register has been written. This bit is automatically set when OCDEN is set if a serial communication error occurs. This bit cannot be written by the CPU if the OCDEN bit is set. 0 = Auto-baud search disabled. 1 = Auto-baud search enabled.

OCD Control Register

The OCD Control Register (OCDCTL), shown in Table 176, controls the state of the CPU. This register puts the CPU in DEBUG Halt Mode, enables breakpoints, or single-steps an instruction.

Table 176. OCD Control Register (OCDCTL)

Bits	7	6	5	4	3	2	1	0
Field	DBGHALT	BRKHALT	BRKEN	DBGSTOP	Reserved			STEP
RESET	0	0	0	0	000			0
R/W	R/W	R/W	R/W	R/W	R			R/W

Bit	Description
[7] DBGHALT	**Debug Halt** Setting this bit to 1 causes the device to enter DEBUG HALT Mode. When in DEBUG HALT Mode, the CPU stops fetching instructions. Clearing this bit causes the CPU to start running again. This bit is automatically set to 1 when a breakpoint occurs if the BRKHALT bit is set. 0 = The device is running. 1 = The device is in DEBUG HALT Mode.
[6] BRKHALT	**Breakpoint Halt** This bit determines what action the OCD takes when a Breakpoint occurs. If this bit is set to 1, then the DBGHALT bit is automatically set to 1 when a breakpoint occurs. If BRKHALT is zero, then the CPU will loop on the breakpoint. 0 = CPU loops on current instruction when breakpoint occurs. 1 = A Breakpoint sets DBGHALT to 1.
[5] BRKEN	**Enable Breakpoints** This bit controls the behavior of the BRK instruction and the hardware breakpoint. By default, these generate an illegal instruction system trap. If this bit is set to 1, these events generate a Breakpoint instead of a system trap. The resulting action depends upon the BRKHALT bit. 0 = BRK instruction and hardware breakpoint generates system trap. 1 = BRK instruction and hardware breakpoint generates a breakpoint.
[4] DBGSTOP	**Debug Stop Mode** This bit controls the system clock behavior in Stop Mode. When set to 1, the system clock will continue to operate in Stop Mode. 0 = Stop Mode debug disabled. system clock stops in Stop Mode. 1 = Stop Mode debug enabled. system clock runs in Stop Mode.

DC Characteristics

Table 186 lists the DC characteristics of the ZNEO® Z16F Series products. All voltages are referenced to V_{SS}, the primary system ground. Any parameter value in the typical column is from characterization at 3.3 V and 0°C. These values are provided for design guidance only and are not tested in production.

Table 186. DC Characteristics

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{DD}	Supply Voltage	2.7	—	3.6	V	
V_{IL1}	Low Level Input Voltage	–0.3		0.3*V_{DD}	V	For all input pins except $\overline{\text{RESET}}$, DBG, X_{IN}
V_{IL2}	Low Level Input Voltage	–0.3	—	0.2*V_{DD}	V	For $\overline{\text{RESET}}$, DBG and X_{IN}
V_{IH1}	High Level Input Voltage	0.7*V_{DD}	—	5.5	V	Port A, C, D, E, F and G pins[1] except pins PC0 and PC1
V_{IH2}	High Level Input Voltage	0.7*V_{DD}	—	V_{DD}+0.3	V	Port B, H and pins PC0 and PC1
V_{IH3}	High Level Input Voltage	0.8*V_{DD}	—	V_{DD}+0.3	V	$\overline{\text{RESET}}$, DBG and X_{IN} pins
V_{OL1}	Low Level Output Voltage Standard Drive	—	—	0.4	V	I_{OL} = 2 mA; V_{DD} = 3.0 V High Output Drive disabled
V_{OH1}	High Level Output Voltage Standard Drive	2.4	—	—	V	I_{OH} = –2 mA; V_{DD} = 3.0 V High Output Drive disabled
V_{OL2}	Low Level Output Voltage High Drive	—	—	0.6	V	I_{OL} = 20 mA; V_{DD} = 3.3 V High Output Drive enabled T_A = –40°C to +70°C
V_{OH2}	High Level Output Voltage High Drive	2.4	—	—	V	I_{OH} = –20 mA; V_{DD} = 3.3 V High Output Drive enabled; T_A = –40°C to +70°C
V_{OL3}	Low Level Output Voltage High Drive	—	—	0.6	V	I_{OL} = 15 mA; V_{DD} = 3.3 V High Output Drive enabled; TA = +70°C to +125°C
V_{OH3}	High Level Output Voltage High Drive	2.4	—	—	V	I_{OH} = 15 mA; V_{DD} = 3.3 V High Output Drive enabled; TA = +70°C to +125°C
I_{IL}	Input Leakage Current	–5	v	+5	µA	V_{DD} = 3.6 V; V_{IN} = V_{DD} or V_{SS}[1]

Note:
1. This condition excludes all pins that have on-chip pull-ups enabled, when driven Low.

SPI Master Mode Timing

Figure 77 and Table 197 provides timing information for SPI Master Mode pins. Timing is shown with SCK rising edge used to source MOSI output data, SCK falling edge used to sample MISO input data. Timing on the SS output pin(s) is controlled by software.

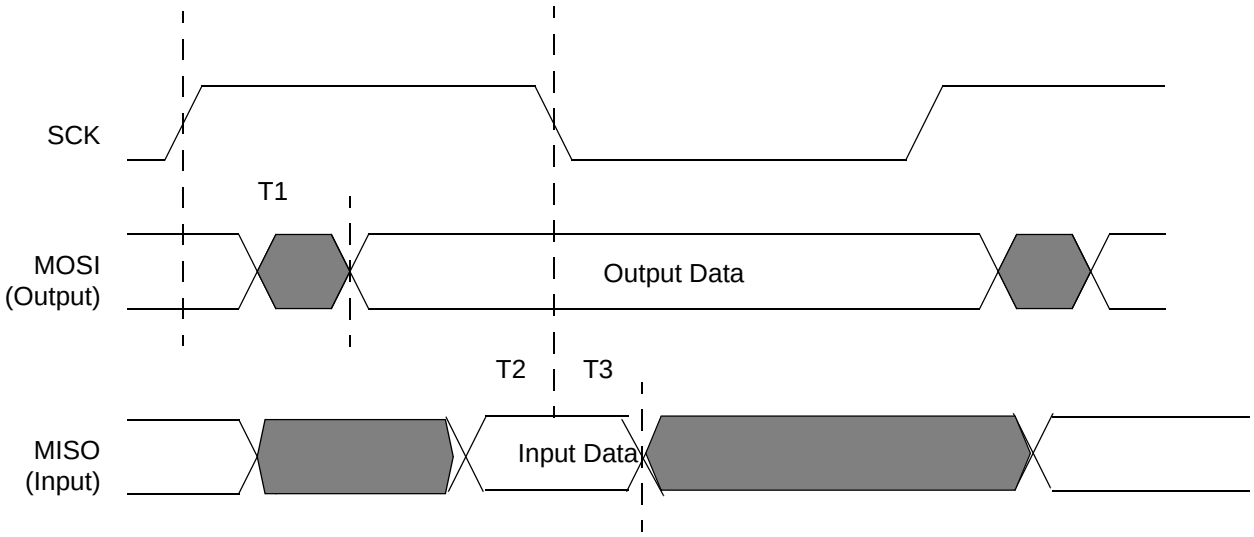


Figure 77. SPI Master Mode Timing

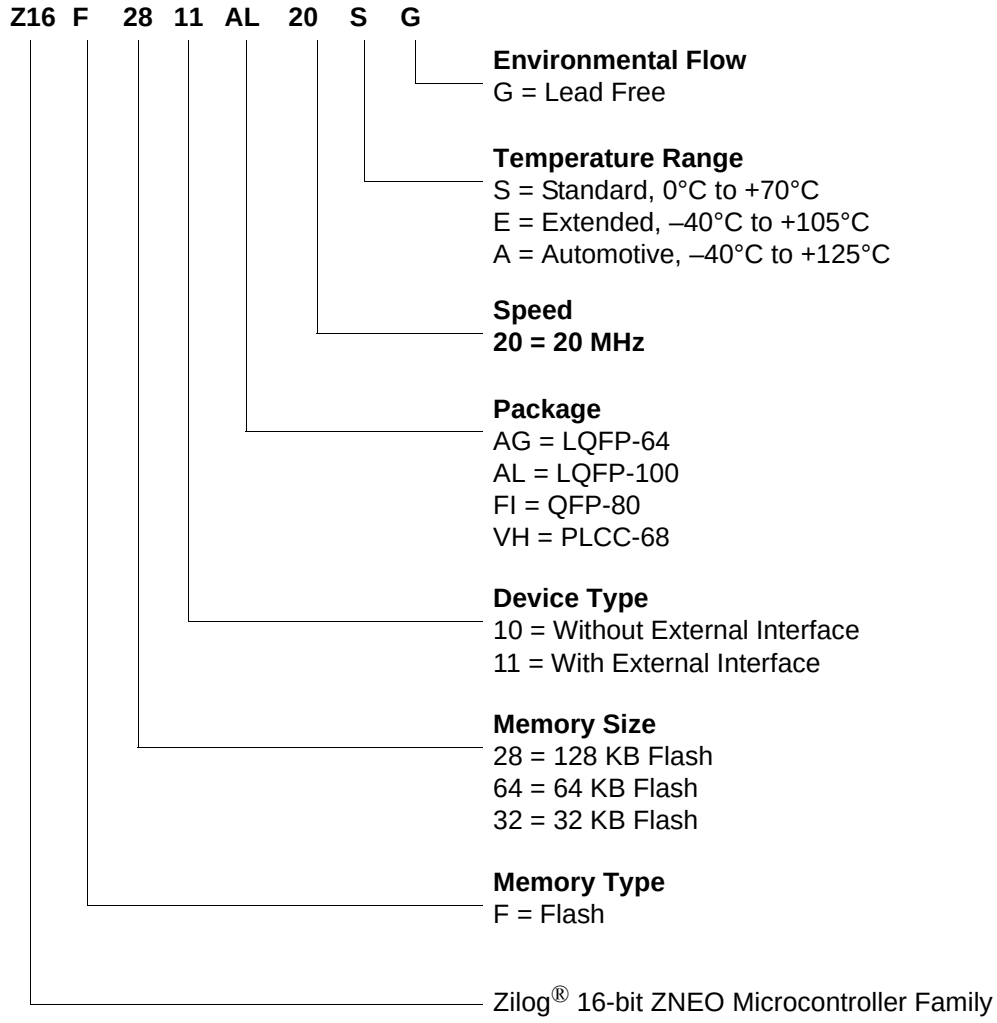
Table 197. SPI Master Mode Timing

		Delay (ns)	
Parameter	**Description**	**Min**	**Max**
SPI Master			
T_1	SCK Rise to MOSI output Valid Delay	–5	+5
T_2	MISO input to SCK (receive edge) Setup Time	20	
T_3	MISO input to SCK (receive edge) Hold Time	0	

SPI Slave Mode Timing

Figure 78 and Table 198 provide timing information for the SPI Slave Mode pins. Timing is shown with SCK rising edge used tosource MISO output data, SCK falling edge used to sample MOSI input data.

Part Number Suffix Designations



Note: Packages are not available for all memory sizes. See the Ordering Information section on page 356 for available packages.

Precharacterization Product

The product represented by this document is newly introduced and Zilog® has not completed the full characterization of the product. The document states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery might be uncertain at times, due to start-up yield issues. For more information, please visit www.zilog.com.