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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2810ag20eg

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E399	PWM 2 High Side Duty Cycle Low Byte	PWMH2DL	00	125
FF_E39A	PWM 2 Low Side Duty Cycle High Byte	PWML2DH	00	124
FF_E39B	PWM 2 Low Side Duty Cycle Low Byte	PWML2DL	00	125
FF_E39C-FF_E3BF	Reserved for PWM	—	—	—
DMA Block Base Address = FF_E400				
DMA Request Selection Control				
FF_E400	DMA0 Request Select	DMA0REQSEL	00	282
FF_E401	DMA1 Request Select	DMA1REQSEL	00	282
FF_E402	DMA2 Request Select	DMA2REQSEL	00	282
FF_E403	DMA3 Request Select	DMA3REQSEL	00	282
FF_E404-F	Reserved	—	—	—
DMA Channel 0 Base Address = FF_E410				
FF_E410	DMA0 Control 0	DMA0CTL0	00	285
FF_E411	DMA0 Control 1	DMA0CTL1	00	285
FF_E412	DMA0 Transfer Length High	DMA0TXLNH	00	286
FF_E413	DMA0 Transfer Length Low	DMA0TXLNL	00	287
FF_E414	Reserved	—	—	—
FF_E415	DMA0 Destination Address Upper	DMA0DARU	00	287
FF_E416	DMA0 Destination Address High	DMA0DARH	00	287
FF_E417	DMA0 Destination Address Low	DMA0DARL	00	287
FF_E418	Reserved	—	—	—
FF_E419	DMA0 Source Address Upper	DMA0SARU	00	288
FF_E41A	DMA0 Source Address High	DMA0SARH	00	288
FF_E41B	DMA0 Source Address Low	DMA0SARL	00	288
FF_E41C	Reserved	—	—	—
FF_E41D	DMA0 List Address Upper	DMA0LARU	00	289
FF_E41E	DMA0 List Address High	DMA0LARH	00	289
FF_E41F	DMA0 List Address Low	DMA0LARL	00	289

XX = Undefined.

tem clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, the ZNEO Z16F Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state 16 system clock cycles following $\overline{\text{RESET}}$ pin deassertion. If the $\overline{\text{RESET}}$ pin is released before the System Reset time-out, the $\overline{\text{RESET}}$ pin is driven Low by the chip until the completion of the time-out as described in the next section. In Stop Mode, the digital filter is bypassed as the system clock is disabled.

Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status and Control Register is set to 1.

External Reset Indicator

During System Reset, the $\overline{\text{RESET}}$ pin functions as an open drain (active Low) RESET Mode indicator in addition to the input functionality. This Reset output feature allows a ZNEO Z16F Series device to Reset other components to which it is connected, even if the Reset is caused by internal sources such as POR, VBO or WDT events and as an indication of when the reset sequence completes.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 18 on page 56 has elapsed.

User Reset

A System Reset is initiated by setting RSTSCR[0]. If the Write was caused by the OCD, the OCD is not Reset.

Fault Detect Logic Reset

Fault detect circuitry exists to detect *illegal* state changes which is caused by transient power or electrostatic discharge events. When such a fault is detected, a system reset is forced. Following the system reset, the FLTD bit in the Reset Status and Control Register is set.

Stop Mode Recovery

Stop Mode is entered by execution of a Stop instruction by the ZNEO CPU. For detailed information about Stop Mode, see the Low-Power Modes chapter on page 64. During Stop Mode Recovery, the device is held in Reset for 66 cycles of the internal precision oscillator.

Reset Status and Control Register

The Reset Status and Control Register (RSTSCR), shown in Table 21, records the cause of the most recent RESET or Stop Mode Recovery. All status bits are updated on each RESET or Stop Mode Recovery event. Table 22 indicates the possible states of the Reset status bits following a RESET or Stop Mode Recovery event.

Table 21. Reset Status and Control Register (RSTSCR)

Bits	7	6	5	4	3	2	1	0
Field	POR	STOP	WDT	EXT	FLT	USR	Reserved	USER_RST
RESET	See Table 22 for a description of these bits.							
R/W	R	R	R	R	R	R	R	W
Addr	FF–E050h							

Bit	Description
[7] POR	For a description of bits [7:2], see Table 22.
[6] STOP	
[5] WDT	
[4] EXT	
[3] FLT	
[2] USR	
[1]	**Reserved** These bits are reserved and must be programmed to 0.
[0] USER_RST	The USER_RST bit in this register allows software controlled RESET of the part pin. This bit is a Write Only bit that causes a System Reset with the result identified by the USR bit after being executed. 0 = No action. 1 = Causes System Reset.

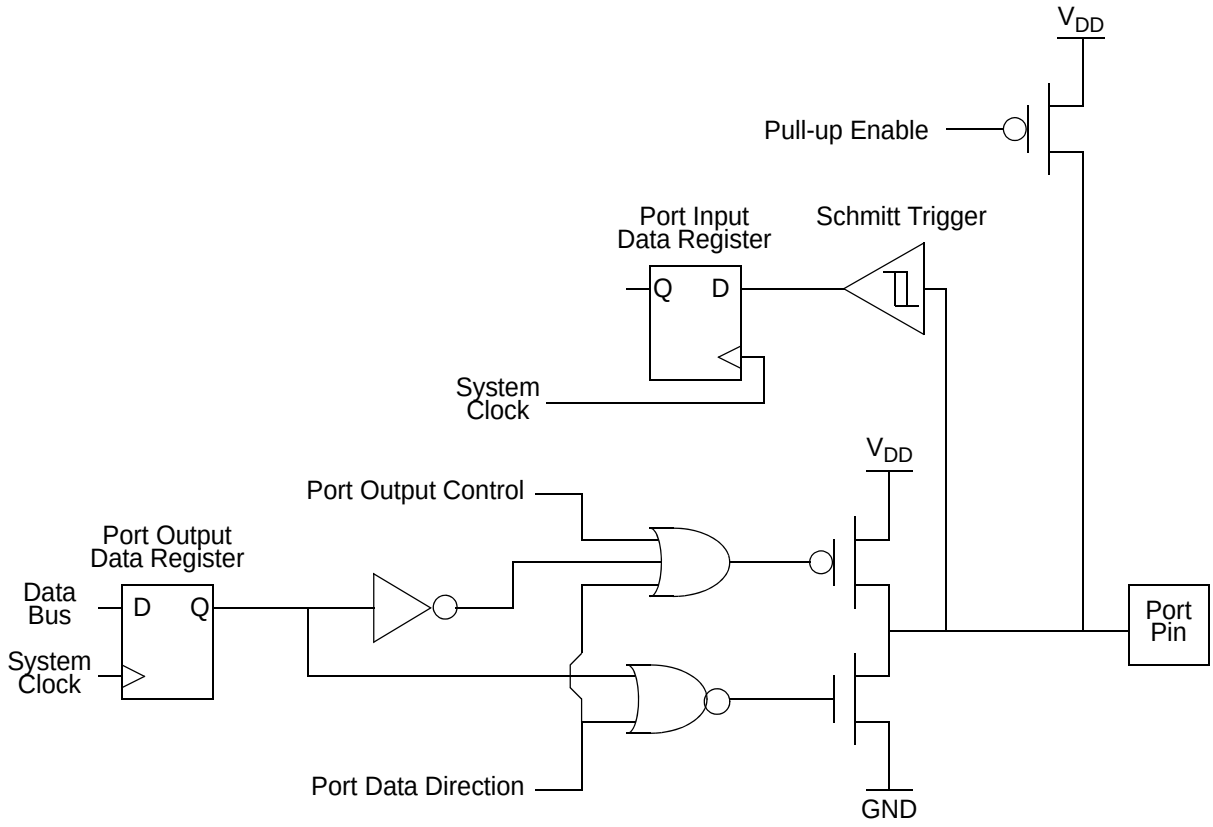

Figure 18. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many GPIO port pins are used for GPIO and to provide access to the on-chip peripheral functions such as timers, serial communication devices and external data and address bus. The Port A–K alternate function registers configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (I/O) is passed from the Port A–K data direction registers to the alternate function assigned to this pin. Table 24 on page 68 lists the alternate functions associated with each port pin.

For detailed information about enabling the external interface data signals, see the External Interface chapter on page 37. When the external interface data signals are enabled for an 8-bit port, the other GPIO functionality including alternate functions cannot be used.

Port A-K Output Data Registers

The Port A-K Output Data registers, shown in Table 26, write output data to the pins.

Table 26. Port A-K Output Data Registers (P*x*OUT)

Bits	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E101, FF_E111, FF_E121, FF_E131, FF_E141, FF_E151, FF_E161, FF_E171, FF_E181, FF_E191							

Bit	Description
[7:0] POUT[7:0]	**Port Output Data** These bits contain the data to be driven out from the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation. 0 = Drive a logical 0 (Low). 1= Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding port output control register bit to 1.

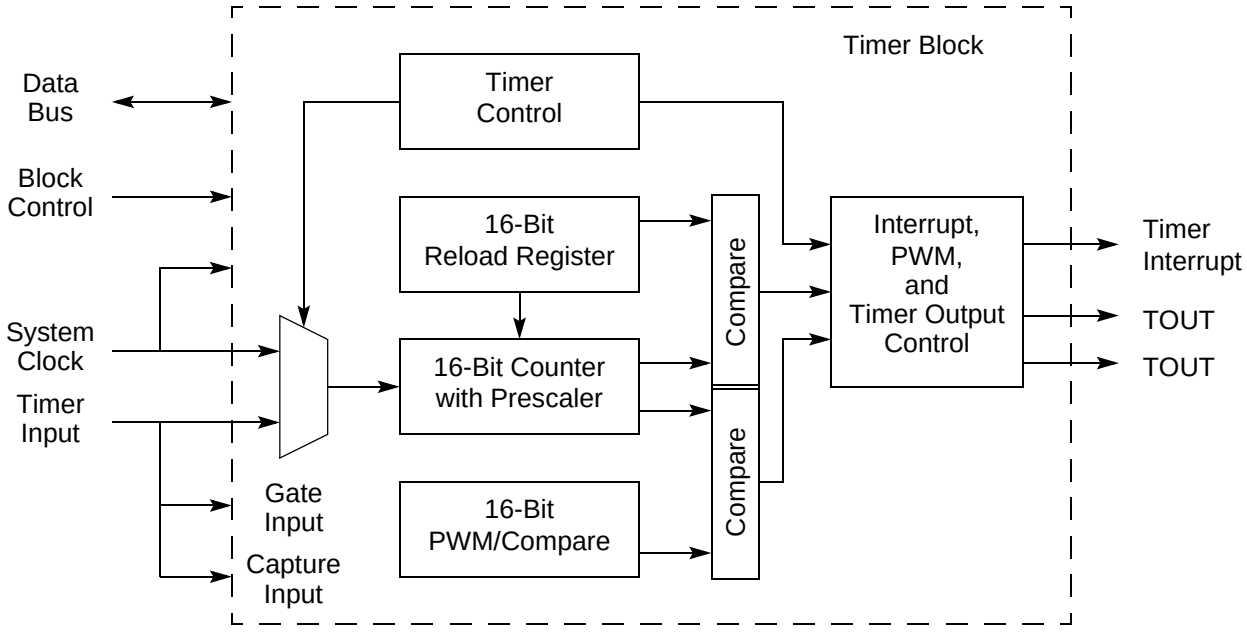

Figure 20. Timer Block Diagram

Operation

The general-purpose timer is a 16-bit up-counter. In normal operation, the timer is initialized to 0001h. When the timer is enabled, it counts up to the value contained in the Reload High and Low Byte registers, then resets to 0001h. The counter either halts or continues depending on the mode.

Minimum time-out delay (1 system clock) is set by loading the value 0001h into the Timer Reload High and Low byte registers and setting the prescale value to 1.

Maximum time-out delay ($2^{16} * 2^7$ system clocks) is set by loading the value 0000h into the Timer Reload High and Low byte registers and setting the prescale value to 128. When the timer reaches FFFFh, the timer rolls over to 0000h.

If the reload register is set to a value less than the current counter value, the counter continues counting until it reaches FFFFh and then resets to 0000h. Then the timer continues to count until it reaches the reload value and it resets to 0001h.

Note: When T0IN0, T0IN1 and T0IN2 functions are enabled on the PB0, PB1 and PB2 pins, each Timer 0 input will have the same effect as the single Timer 0 Input pin T0IN. For example, if the Timer 0 is in Capture Mode, any transitions on any of the PB0, PB1 and PB2 pins will cause a Capture.

c. Set or clear the CTSE bit to enable or disable control from the remote receiver through the $\overline{CTS}$ pin.

7. Execute an EI instruction to enable interrupts.

The LIN-UART is now configured for interrupt-driven data transmission. As the LIN-UART Transmit Data Register is empty, an interrupt is generated immediately. When the LIN-UART transmit interrupt is detected and there is transmit data ready to send, the associated interrupt service routine (ISR) performs the following operations:

1. If operating in Multiprocessor Mode, write the LIN-UART Control 1 Register to select the outgoing address bit by setting the multiprocessor bit transmitter (MPBT) if sending an address byte; clear it if sending a data byte.
2. Write the data byte to the LIN-UART Transmit Data Register. The transmitter automatically transfers the data to the transmit shift register and transmits the data.
3. Execute the IRET instruction to return from the interrupt service routine and waits for the Transmit Data Register to again become empty.

If a transmit interrupt occurs and there is no transmit data ready to send, the interrupt service routine executes the IRET instruction. When the application contains data to transmit, software sets the appropriate interrupt request bit in the interrupt controller to initiate a new transmit interrupt. Another alternative would be for software to write the data to the Transmit Data Register instead of invoking the ISR.

Receiving Data Using the Polled Method

Observe the following steps to configure the LIN-UART for polled data reception:

1. Write to the LIN-UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the LIN-UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Write to the LIN-UART Control 1 Register to enable Multiprocessor Mode functions.
4. Write to the LIN-UART Control 0 Register to:
   a. Set the receive enable bit (REN) to enable the LIN-UART for data reception.
   b. Enable parity, if Multiprocessor Mode is not enabled and select either even or odd parity.
5. Check the RDA bit in the LIN-UART Status 0 Register to determine if the Receive Data Register contains a valid data byte (indicated by a 1). If RDA is set to 1 to indicate available data, continue to Step 6. If the Receive Data Register is empty (indicated by a 0), continue to monitor the RDA bit awaiting reception of the valid data.

- Parity error (PE bit in Status 0 Register) is redefined as the Physical Layer Error (PLE) bit. The PLE bit indicates that receive data does not match transmit data when the LIN-UART is transmitting. This applies to both Master and Slave operating modes.
- The break detect interrupt (BRKD bit in Status 0 Register) indicates when a Break is detected by the slave (break condition for at least 11 bit times). Software uses this interrupt to start a timer checking for message frame time-out. The duration of the break is read in the RxBreakLength[3:0] field of the Mode Status Register.
- The break detect interrupt (BRKD bit in Status 0 Register) indicates when a wake-up message has been received if the LIN-UART is in a LINSLEEP state.
- In LIN Slave Mode, if the BRG counter overflows while measuring the autobaud period (Start bit to beginning of bit 7 of autobaud character) an overrun error is indicated (OE bit in the Status 0 Register). In this case, software sets the LinState field back to `10b`, where the slave ignores the current message and waits for the next Break signal. The baud reload high and low registers are not updated by hardware if this autobaud error occurs. The OE bit is also set if a data overrun error occurs.

LIN System Clock Requirements

The LIN master provides the timing reference for the LIN network and is required to have a clock source with a tolerance of ±0.5%. A slave with autobaud capability is required to have a baud clock matching the master oscillator within ±14%. The slave nodes autobaud to lock onto the master timing reference with an accuracy of ±2%. If a slave does not contain autobaud capability, it must include a baud clock which deviates from the masters by no more than ±1.5%. These accuracy requirements must include effects such as voltage and temperature drift during operation.

Before sending or receiving messages, the baud reload High/Low registers must be initialized. Unlike standard UART modes, the baud reload High/Low registers must be loaded with the baud interval rather than 1/16 of the baud interval.

In order to autobaud with the required accuracy, the LIN slave system clock must be at least 100 times the baud rate.

LIN Mode Initialization and Operation

A LIN protocol mode is selected by setting either the LIN master (LMST) or LIN slave (LSLV) and optionally (for LIN slave) the autobaud enable (ABEN) bits in the LIN Control Register. To access the LIN Control Register, the mode select (MSEL) field of the LIN-UART Mode Select/Status Register must be `010b`. The LIN-UART Control 0 Register must be initialized with TEN = 1, REN = 1, all other bits = 0.

In addition to the LMST, LSLV and ABEN bits in the LIN Control Register, a LinState[1:0] field exists that defines the current state of the LIN logic. This field is initially

request enable (DIRQE) bit is set. The TDRE and RDRF signals also generate transmit and receive DMA requests.

In many cases the software application is only moving information in one direction. In such a case, either the TDRE or RDRF interrupts/DMA requests is disabled to minimize software/DMA overhead. Unidirectional data transfer is supported by setting the ESPIEN1, 0 bits in the control register to 10 or 01. If the DMA engine is being used to move the data, the transmit and receive data interrupts are disabled through the DIRQE bit of the control register. In this case error interrupts still occurs and must be handled directly by the software.

Throughput

In Master Mode, the maximum supported SCK rate is one-half the system clock frequency. This rate is achieved by programming the value 0001h into the baud rate high/low register pair. Though each character is transferred at this rate, it is unlikely that software interrupt routines or DMA keeps up with this rate. In SPI Mode, the transfer will automatically pause between characters until the current receive character is read and the next transmit data value is written.

In Slave Mode, the transfer rate is controlled by the master. As long as the TDRE and RDRF interrupt or DMA requests are serviced before the next character transfer completes the slave will keep up with the master. In Slave Mode, the baud rate is restricted to a maximum of one-fourth of the system clock frequency to allow for synchronization of the SCK input to the internal system clock.

ESPI Clock Phase and Polarity Control

The ESPI supports four combinations of SCK phase and polarity using two bits in the ESPI Control Register. The clock polarity bit, CLKPOL, selects an active High or active Low clock and has no effect on the transfer format. The clock phase bit, PHASE, selects one of two fundamentally different transfer formats. The data is output a half-cycle before the receive clock edge which provides a half cycle of setup and hold time. Table 98 lists the ESPI clock phase and polarity operation parameters.

Table 98. ESPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High

Bit	Description (Continued)
[2] WOR	**Wire-OR (Open-Drain) Mode Enabled** 0 = ESPI signal pins not configured for open-drain. 1 = All four ESPI signal pins (SCK, $\overline{SS}$, MISO, MOSI) configured for open-drain function. This setting is used for Multi-Master and/or Multi-Slave configurations.
[1] MMEN	**ESPI Master Mode Enable** This bit controls the data I/O pin selection and SCK direction. 0 = Data-out on MISO, data-in on MOSI (used in SPI Slave Mode), SCK is an input. 1 = Data-out on MOSI, data-in on MISO (used in SPI Master Mode), SCK is an output.

Caution: If reading the counter one byte at a time while the BRG is counting keep in mind that the values will not be in sync. It is recommended to read the counter using word (2-byte) reads.

I²C Master/Slave Controller Registers

Table 111 summarizes the I²C Master/Slave Controller software-accessible registers.

Table 111. I²C Master/Slave Controller Registers

Name	Abbreviation	Description
I²C Data	I2CDATA	Transmit/Receive Data Register.
I²C Interrupt Status	I2CISTAT	Interrupt Status Register.
I²C Control	I2CCTL	Control Register–basic control functions.
I²C Baud Rate High	I2CBRH	High byte of baud rate generator initialization value.
I²C Baud Rate Low	I2CBRL	Low byte of baud rate generator initialization value.
I²C State	I2CSTATE	State Register.
I²C Mode	I2CMODE	Selects MASTER or SLAVE modes, 7-bit or 10-Bit Address. Configure address recognition, Defines Slave Address bits [9:8].
I²C Slave Address	I2CSLVAD	Defines Slave Address bits [7:0]

Comparison with Master Mode only I²C Controller

Porting code written for the Master-only I²C Controller found on other Z8 Encore!® parts to the I²C Master/Slave Controller is straightforward. The I2CDATA, I2CCTL, I2CBRH and I2CBRL Register definitions are not changed.

The differences between the Master-only I²C Controller and I²C Master/Slave Controller designs are:

- The Status Register (I2CSTATE) from the Master-only I²C Controller is split into the Interrupt Status (I2CISTAT) Register and the State (I2CSTATE) Register because there are more interrupt sources. The ACK, 10b, TAS (now called AS) and DSS (now called DS) bits formerly in the status register are moved to the state register.
- The I2CSTATE Register is called as I2CDST (Diagnostic State) Register in the Master Only Mode version. The I2CDST Register provided diagnostic information. The I2CSTATE Register contains status and state information that are useful to software in operational mode.
- The I2CMODE Register is called as I2CDIAG (Diagnostic Control) Register in the Master Only Mode version. The I2CMODE Register provides control for Slave modes of operation as well as the most significant two bits of the 10-bit Slave address.
- The I2CSLVAD Register is added for programming the Slave address.
- The ACKV bit in the I2CSTATE Register enables the Master to verify the acknowledge from the Slave before sending the next byte.

ADC Timer 0 Capture Register

The ADC Timer 0 Capture Register contains the sixteen bits of the ADC Timer 0 count. The access to the ADC Timer 0 Capture Register is read-only. It reads 8 bits at a time or as a 16-bit word.

Table 133. ADC Timer 0 Capture Register, High Byte (ADCTCAP_H)

Bits	7	6	5	4	3	2	1	0
Field	ADCTCAPH							
RESET	X							
R/W	R							
Addr	FF–E512h							

Bit	Description
[7:0] ADCTCAPH	**ADC Timer 0 Count High Byte** 00h–FFh = The Timer 0 count is held in the data registers until the next ADC conversion is started.

Table 134. ADC Timer 0 Capture Register, Low Byte (ADCTCAP_L)

Bits	7	6	5	4	3	2	1	0
Field	ADCTCAPL							
RESET	X							
R/W	R							
Addr	FF–E513h							

Bit	Description
[7:0] ADCTCAPL	**ADC Timer 0 Count Low Byte** 00h–FFh = The Timer 0 count is held in the data registers until the next ADC conversion is started.

Comparator and Operational Amplifier Overview

ZNeo devices feature a general-purpose comparator and an operational amplifier. The comparator is a moderate speed (200 ns propagation delay) device which is designed for a maximum input offset of 5 mV. The comparator is used to compare two analog input signals. General-purpose input pins (CINP and CINN) provides the comparator inputs. The output is available as an interrupt source.

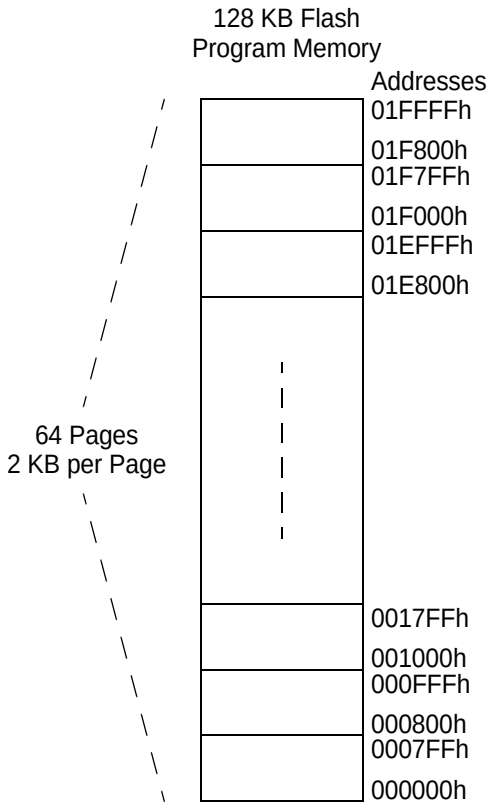

Figure 55. Flash Memory Arrangement

Information Area

Table 138 describes the ZNEO Z16F Series Information Area. This 128-byte Information Area is accessed by setting bit 7 of the Flash Control register to 1. When access is enabled, the Information Area is mapped into program memory and overlays the 128 bytes at addresses 000000h to 00007Fh. When the Information Area access is enabled, instructions access data from the Information Area. The CPU instruction fetches always come from Main Memory regardless of the Information Area access bit. Access to the Information Area is read-only.

Flash Status Register

The Flash Status Register, shown in Table 140, indicates the current state of the Flash Controller. This register is read at any time. The Read-only Flash Status Register shares its address with the Write-only Flash Command Register.

Table 140. Flash Status Register (FSTAT)

Bits	7	6	5	4	3	2	1	0
Field	UNLOCK	Reserved	FSTAT					
RESET	0	0	00h					
R/W	R	R	R					
Addr	FF_E060h							

Bit	Description
[7] UNLOCK	**Unlocked** This status bit is set when the Flash Controller is unlocked. 0 = Flash Controller locked. 1 = Flash Controller unlocked.
[6]	**Reserved** This bit is reserved and must be programmed to 0.
[5:0] FSTAT	**Flash Controller Status** 00_0000 = Flash Controller idle. 00_1xxx = Program operation in progress. 01_0xxx = Page erase operation in progress. 10_0xxx = Mass erase operation in progress.

DMA Watermark

When operating in DIRECT Mode, the DMAxLAR[23:16] byte is used as a watermark interrupt. If these bits are set to any value other than 0, they are compared to the low byte of the decremented transfer length during a transfer. If the IEOB bit is set and the upper byte of DMAxTXLN[15:8] is zero and DMAxTXLN[7:0] == DMAxLAR[23:16] then an interrupt is generated. This function allows the DMA Channel to generate an interrupt prior to the buffer becoming empty.

DMA Peripheral Interface signals

The DMA uses two input signals, four output signals and two 4-bit buses to communicate with the peripherals. The input signals are Request (REQ) and Request EOF. The output signals are Acknowledge (ACK), Command Valid (CMDVLD), End of Frame (EOF-SYNC) and Read Status (RDSTAT). The two 4-bit buses are Command Bus (CMDBUS) and Stat Bus (STATBUS).

A DMA transfer is initiated with the Request (REQ). When the DMA is servicing a Request from a peripheral it will assert its acknowledge signal (ACK) to let the peripheral know that a transfer is in progress. When the first byte of the transfer is written the CMD-VLD is asserted and the command bits are placed on the CMDBUS. The peripheral must latch the command from the bus when it sees this combination of signals.

If the EOF bit is set on the current buffer, then when the TXLN decrements to 0, the EOF-SYNC signal is asserted on the last data transfer to the peripheral. As a result, the periph-eral is informed that it has received the last byte in the frame.

After receiving the EOFSYNC signal, the peripheral must assert the Request EOF signal to the DMA to let the DMA know that the descriptor is closed. This could be immediately or at some later time if the data transferred still must be processed. For peripherals, which do not support a Request EOF, the EOFSYNC is tied to Request EOF to terminate the transfer.

After the Request EOF is asserted the DMA closes the descriptor. The DMA asserts the ACK and RDSTAT signal, if the descriptor EOF bit is set. The peripheral, if it has status, places it on the STATBUS. This status is then placed in the descriptor and DMA status bits when it is closed.

If a peripheral must close a descriptor because of an error or the end of a packet is reached then it asserts it is Request EOF. If the transfer length is not zero, then the DMA will set the EOF bit, close the descriptor and generate an interrupt.

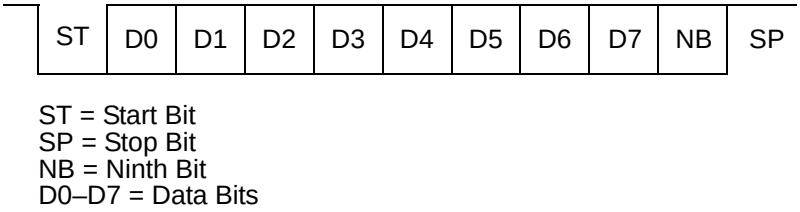

Figure 67. 9-Bit Mode

Start Bit Flow Control

If flow control is required, start bit flow control is used. Start bit flow control requires the receiving device send the start bit. The transmitter waits for the start bit, then transmit its data following the start bit.

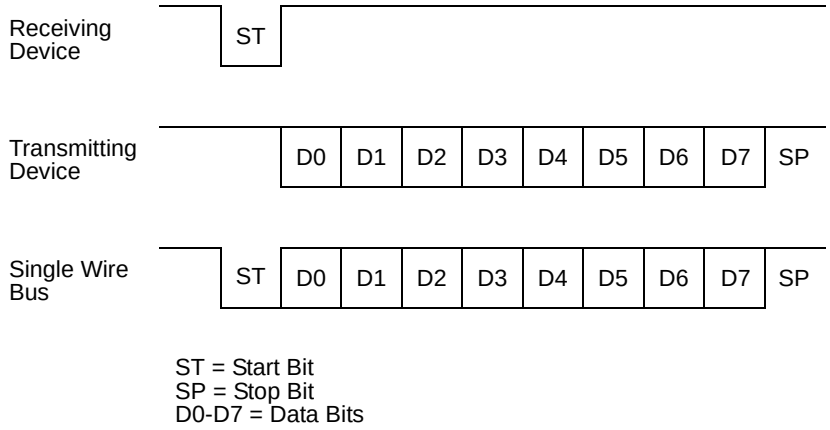

Figure 68. Start Bit Flow Control

If the standard serial port of a PC is used, transmit flow control is enabled on the ZNEO Z16F Series device. The PC sends the start bit when receiving data by transmitting the character FFh. Because the FFh character is also received from a nonresponsive device, space parity (parity bit always zero) must be enabled and used as an acknowledge bit.

Initialization

The OCD ignores any data received until it receives the read revision command 00h. After the read revision command is received, the remaining debug commands are issued. The packet CRC is not sent for the first read revision command issued during initialization.

Clock Failure Detection and Recovery

Primary Oscillator Failure

The ZNEO Z16F Series generates a System Exception when a failure of the primary oscillator occurs if the POFEN bit is set in the OSCCTL Register. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer oscillator to drive the system clock. Although this oscillator runs at a much lower frequency than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the WDT is the primary oscillator.

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 kHz ±50%. For operating frequencies below 2 kHz, do not enable the clock failure circuitry (POFEN must be deserted in the OSCCTL Register).

Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a System Exception is used if the WDFEN bit of the OSCCTL Register is set. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a WDT failure, it is no longer possible to detect a primary oscillator failure.

The Watchdog Timer oscillator failure detection circuit counts system clocks while looking for a WDT clock. The logic counts 8000 system clock cycles before determining that a failure occurred. The system clock rate determines the speed at which the WDT failure is detected. A very slow system clock results in very slow detection times.

If the WDT is the primary oscillator or if the Watchdog Timer oscillator is disabled, deassert the WDFEN bit of the OSCCTL Register.

Oscillator Control Register Definitions

Oscillator Control Register

The Oscillator Control Register (OSCCTL), shown in Table 183, enables or disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry, actively powers down the flash and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Writing the two-step sequence E7h followed by 18h to the Oscillator Control Register address unlocks it. The register locks after completion of a register write to the OSCCTL.

Table 185. Absolute Maximum Ratings (Continued)

Parameter	Minimum	Maximum	Units	Notes
Maximum current into V_{DD} or out of V_{SS}		56	mA	
68-Pin PLCC Maximum Ratings at –40°C to 70°C				
Total power dissipation		1.0	W	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
68-Pin PLCC Maximum Ratings at 70°C to 125°C				
Total power dissipation		500	W	
Maximum current into V_{DD} or out of V_{SS}		140	mA	
64-Pin LQFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		1.0	W	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
64-Pin LQFP Maximum Ratings at 70°C to 125°C				
Total power dissipation		540	W	
Maximum current into V_{DD} or out of V_{SS}		150	mA	

Notes:
1. This voltage applies to 5 V tolerant pins which are Port A, C, D, E, F and G pins (except pins PC0 and PC1).
2. This voltage applies to V_{DD}, AV_{DD}, pins supporting analog input (Ports B and H), Pins PC0 and PC1, RESET, DBG and X_{IN} pins which are non 5 V tolerant pins.

V

W

Z