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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2810ag20sg

Use of the Terms LSB, MSB, lsb, and msb

In this document, the terms LSB and MSB, when appearing in upper case, mean least significant byte and most significant byte, respectively. The lowercase forms, lsb and msb, mean least significant bit and most significant bit, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings and modes in general text.

Example 1. The receiver forces the SCL line to Low.

Example 2. Stop Mode.

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states and commands.

Example 1. The bus is considered BUSY after the Start condition.

Example 2. A Start command triggers the processing of the initialization sequence.

Bit Numbering

Bits are numbered from 0 to *n*–1, in which *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that all users understand the following safety terms, which are defined here.

Caution: Indicates that a procedure or file may become corrupted if you do not follow instructions.

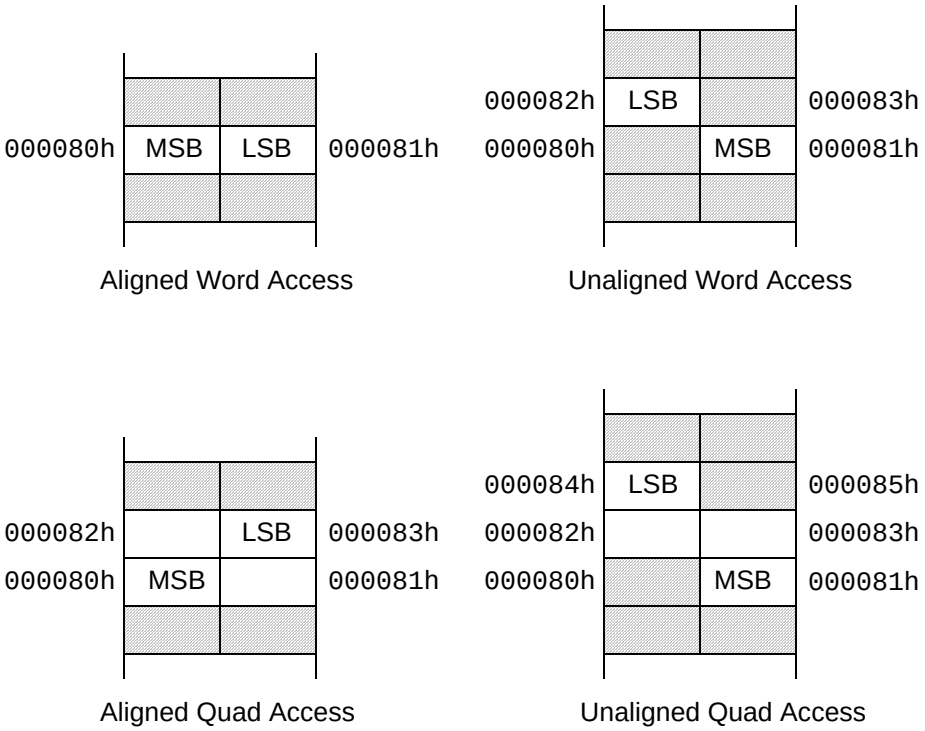

Figure 8. Alignment of Word and Quad Operations on 16-bit Memories

tem clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, the ZNEO Z16F Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state 16 system clock cycles following $\overline{\text{RESET}}$ pin deassertion. If the $\overline{\text{RESET}}$ pin is released before the System Reset time-out, the $\overline{\text{RESET}}$ pin is driven Low by the chip until the completion of the time-out as described in the next section. In Stop Mode, the digital filter is bypassed as the system clock is disabled.

Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status and Control Register is set to 1.

External Reset Indicator

During System Reset, the $\overline{\text{RESET}}$ pin functions as an open drain (active Low) RESET Mode indicator in addition to the input functionality. This Reset output feature allows a ZNEO Z16F Series device to Reset other components to which it is connected, even if the Reset is caused by internal sources such as POR, VBO or WDT events and as an indication of when the reset sequence completes.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 18 on page 56 has elapsed.

User Reset

A System Reset is initiated by setting RSTSCR[0]. If the Write was caused by the OCD, the OCD is not Reset.

Fault Detect Logic Reset

Fault detect circuitry exists to detect *illegal* state changes which is caused by transient power or electrostatic discharge events. When such a fault is detected, a system reset is forced. Following the system reset, the FLTD bit in the Reset Status and Control Register is set.

Stop Mode Recovery

Stop Mode is entered by execution of a Stop instruction by the ZNEO CPU. For detailed information about Stop Mode, see the Low-Power Modes chapter on page 64. During Stop Mode Recovery, the device is held in Reset for 66 cycles of the internal precision oscillator.

Table 29. Port A-K Alternate Function High Registers (PxAFH)

Bits	7	6	5	4	3	2	1	0
Field	AFH[7]	AFH[6]	AFH[5]	AFH[4]	AFH[3]	AFH[2]	AFH[1]	AFH[0]
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E104, FF_E124, FF_E134, FF_E174							

Table 30. Port A-K Alternate Function Low Registers (PxAFL)

Bits	7	6	5	4	3	2	1	0
Field	AFL[7]	AFL[6]	AFL[5]	AFL[4]	AFL[3]	AFL[2]	AFL[1]	AFL[0]
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E105, FF_E115, FF_E125, FF_E135, FF_E155, FF_E165, FF_E175, FF_E195							

Table 31. Alternate Function Enabling

AFH[*x*]	AFL[*x*]	Priority
0	0	No Alternate Function Enabled
0	1	Alternate Function 1 Enabled
1	0	Alternate Function 2 Enabled
1	1	Alternate Function 3 Enabled
Note: *x* indicates the register bits from 0 through 7.		

Port A-K Output Control Registers

Setting the bits in the Port A-K Output Control registers to 1, shown in Table 32, configures the specified port pins for open-drain operation. These registers affect the pins directly and as a result, alternate functions are also affected. Enabling the I^2C controller automatically configures the SCL and SDA pins as open-drain; independent of the setting in the output control registers that have the SCL and SDA alternate functions.

Bit	Description (Continued)
[2] BRGCTL	**Baud Rate Generator Control** This bit causes different LIN-UART behaviors, depending on whether the LIN-UART receiver is enabled (REN = 1 in the LIN-UART Control 0 Register). When the LIN-UART receiver is not enabled, this bit determines whether the baud rate generator issues interrupts. 0 = BRG is disabled. Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value. 1 = BRG is enabled and counting. The BRG generates a receive interrupt when it counts down to 0. Reads from the Baud Rate High and Low Byte registers return the current BRG count value. When the LIN-UART receiver is enabled, this bit allows reads from the baud rate registers to return the BRG count value instead of the Reload Value. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value. 1 = Reads from the Baud Rate High and Low Byte registers return the current BRG count value. Unlike the timers, there is no mechanism to latch the High byte when the Low byte is read.
[1] RDAIRQ	**Receive Data Interrupt Enable** 0 = Received data and receiver errors generates an interrupt request to the interrupt controller. 1 = Received data does not generate an interrupt request to the interrupt controller. Only receiver errors generate an interrupt request.
[0] IREN	**Infrared Encoder/Decoder Enable** 0 = Infrared encoder/decoder is disabled. LIN-UART operates normally. 1 = Infrared encoder/decoder is enabled. The LIN-UART transmits and receives data through the Infrared encoder/decoder.

Table 96. LIN-UART Baud Rates (Continued)

5.5296 MHz System Clock				3.579545 MHz System Clock			
Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	345.6	38.24	250.0	1	223.72	–10.51
115.2	3	115.2	0.00	115.2	2	111.9	–2.90
57.6	6	57.6	0.00	57.6	4	55.9	–2.90
38.4	9	38.4	0.00	38.4	6	37.3	–2.90
19.2	18	19.2	0.00	19.2	12	18.6	–2.90
9.60	36	9.60	0.00	9.60	23	9.73	1.32
4.80	72	4.80	0.00	4.80	47	4.76	–0.83
2.40	144	2.40	0.00	2.40	93	2.41	0.23
1.20	288	1.20	0.00	1.20	186	1.20	0.23
0.60	576	0.60	0.00	0.60	373	0.60	–0.04
0.30	1152	0.30	0.00	0.30	746	0.30	–0.04

Infrared Encoder/Decoder

The ZNEO® Z16F Series products contain two fully-functional, high-performance UART-to-infrared encoder/decoders (endecs). Each infrared endec is integrated with an on-chip UART to allow easy communication between the ZNEO and IrDA physical layer specification, version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers and other infrared-enabled devices.

Architecture

Figure 32 displays the architecture of the infrared endec.

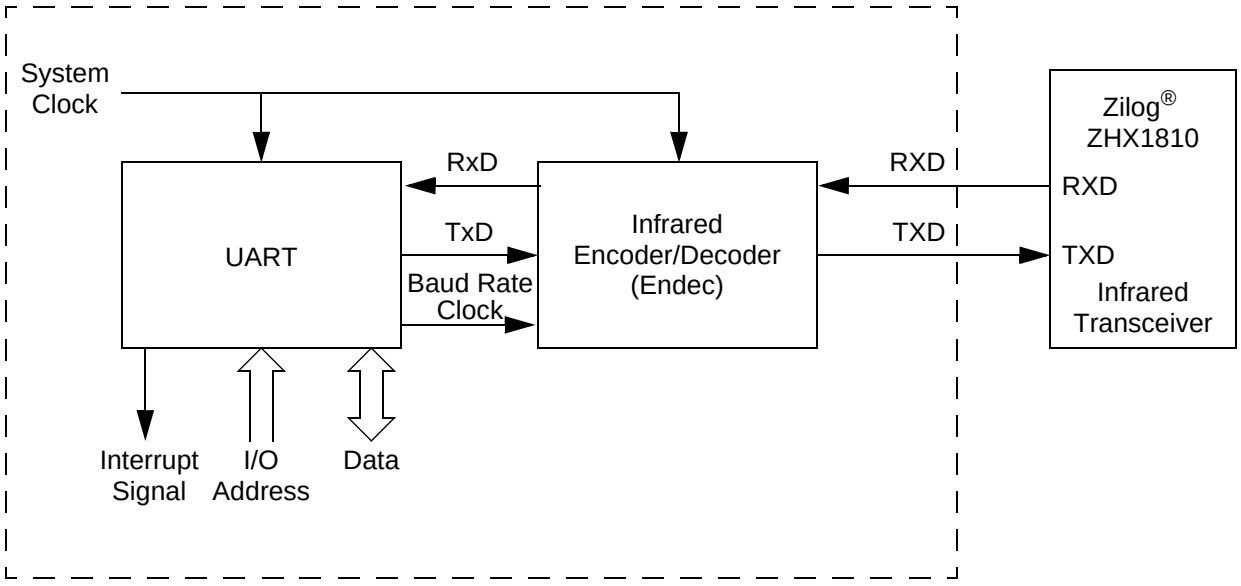

Figure 32. Infrared Data Communication System Block Diagram

Operation

When the infrared endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver via the TXD pin. Similarly, data received from the infrared transceiver is passed to the infrared endec via the RXD pin, decoded by the infrared endec and then

Bit	Description (Continued)
[4:2] NUMBITS[2:0]	**Number of Data Bits Per Character to Transfer** This field contains the number of bits to shift for each character transfer. For information about valid bit positions when the character length is less than 8-bits, see the ESPI Data Register section on page 193. 000 = 8 bits 001 = 1 bit 010 = 2 bits 011 = 3 bits 100 = 4 bits 101 = 5 bits 110 = 6 bits 111 = 7 bits
[1] SSIO	**Slave Select I/O** This bit controls the direction of the $\overline{SS}$ pin. In single Master Mode, SSIO is set to 1 unless a separate GPIO pin is being used to provide the $\overline{SS}$ output function. In the SPI Slave or Multi-Master configuration SSIO is set to 0. 0 = $\overline{SS}$ pin configured as an input (SPI Slave and Multi-Master modes) 1 = $\overline{SS}$ pin configured as an output (SPI single Master Mode)
[0] SSPO	**Slave Select Polarity** This bit controls the polarity of the $\overline{SS}$ pin. 0 = $\overline{SS}$ is active Low. (SSV = 1 corresponds to $\overline{SS}$ = 0) 1 = $\overline{SS}$ is active High. (SSV = 1 corresponds to $\overline{SS}$ = 1)

ESPI Status Register

The ESPI Status Register, shown in Table 106, indicates the current state of the ESPI. All bits revert to their Reset state, if the ESPI is disabled.

Table 106. ESPI Status Register (ESPISTAT)

Bits	7	6	5	4	3	2	1	0
Field	TDRE	TUND	COL	ABT	ROVR	RDRF	TFST	SLAS
RESET	0	0	0	0	0	0	0	1
R/W	R	R/W*	R/W*	R/W*	R/W*	R	R	R
Addr	FF_E264h							
R/W* = Read access. Write a 1 to clear the bit to 0.								

Bit	Description
[7] TDRE	**Transmit Data Register Empty** 0 = Transmit Data Register is full or ESPI is disabled. 1 = Transmit Data Register is empty. A write to the ESPI (Transmit) Data register clears this bit.

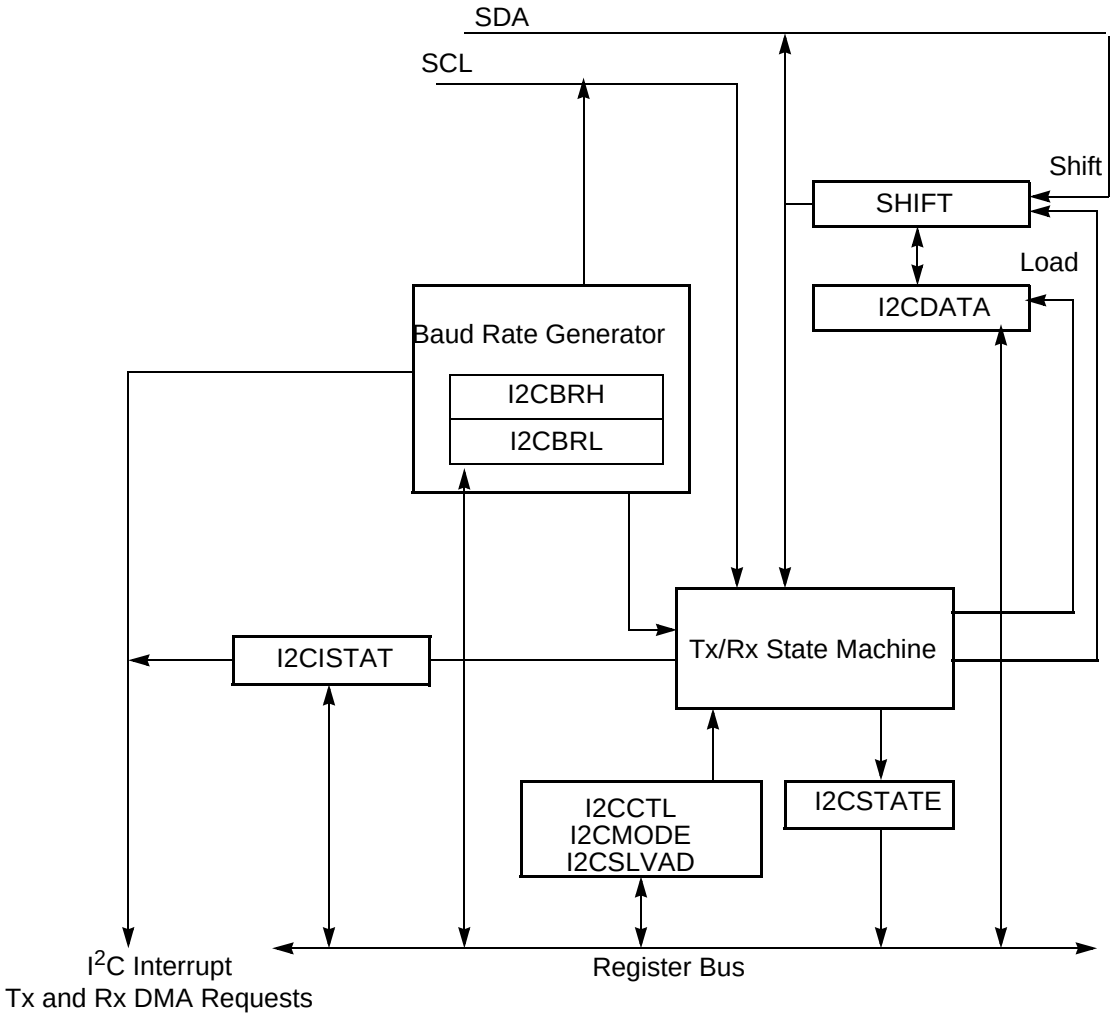

Figure 43. I2C Controller Block Diagram

Each interrupt source other than the baud rate generator interrupt has an associated bit in the I2CISTAT Register, which clears automatically when software reads the register or performs some other task such as reading or writing the data register.

Transmit Interrupts

Transmit interrupts (TDRE bit = 1 in I2CISTAT) occur under the following conditions:

- The Transmit Data Register is empty and the TXI bit = 1 in the I^2C Control Register
- The I^2C Controller is enabled, with any one of the following operations:
  - The first bit of a 10-bit address is shifted out
  - The first bit of the final byte of an address is shifted out and the RD bit is deasserted
  - The first bit of a data byte is shifted out

Writing to the I^2C Data Register always clears the TRDE bit to 0.

Receive Interrupts

Receive interrupts (RDRF bit = 1 in I2CISTAT) occur when a byte of data has been received by the I^2C Controller. The RDRF bit is cleared by reading from the I^2C Data Register. If the RDRF interrupt is not serviced prior to the completion of the next receive byte, the I^2C Controller holds SCL Low during the last data bit of the next byte until RDRF is cleared to prevent receive overruns. A receive interrupt does not occur when a Slave receives an address byte or for data bytes following a Slave address that did not match. An exception is if the interactive receive mode (IRM) bit is set in the I2CMODE Register in which case receive interrupts occur for all receive address and data bytes in Slave Mode.

Slave Address Match Interrupts

Slave address match interrupts (SAM bit = 1 in I2CISTAT) occur when the I^2C Controller is in Slave Mode and an address is received which matches the unique Slave address. The General Call Address (0000_0000) and STARTBYTE (0000_0001) are recognized if the GCE bit = 1 in the I2CMODE Register. Software verifies the RD bit in the I2CISTAT Register to determine if the transaction is a read or write transaction. The General Call Address and STARTBYTE addresses are also distinguished by the RD bit. The general call address (GCA) bit of the I2CISTAT Register indicates whether the address match occurred on the unique Slave address or the General Call/STARTBYTE address. The SAM bit clears automatically when the I2CISTAT Register is read.

If configured using the MODE[1:0] field of the I^2C Mode Register for 7-bit slave addressing, the most significant 7 bits of the first byte of the transaction are compared against the SLA[6:0] bits of the Slave Address Register. If configured for 10-bit slave addressing, the

Bit	Description (Continued)
[1] SCLOUT	**Serial Clock Output** Current value of Serial Clock being output onto the bus. The actual values of the SCL and SDA signals on the I2C bus is observed via the GPIO Input Register.
[0] BUSY	**I2C Bus Busy** 0 = No activity on the I2C Bus. 1 = A transaction is underway on the I2C bus.

Table 118. I2C State Register (I2CSTATE), Description when DIAG = 1

Bits	7	6	5	4	3	2	1	0
Field	I2CSTATE_H				I2CSTATE_L			
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Addr	FF–E245h							

Bit	Description
[7:4] I2CSTATE_H	**I2C State High** This field defines the current state of the I2C Controller. It is the most significant nibble of the internal state machine. Table 119 defines the states for this field.
[3:0] I2CSTATE_L	**I2C State Low** Least significant nibble of the I2C state machine. This field defines the substates for the states defined by I2CSTATE_H. Table 120 defines the values for this field.

Table 119. I2CSTATE_H

State Encoding	State Name	State Description
0000	Idle	I2C bus is idle or I2C Controller is disabled.
0001	Slave Start	I2C Controller has received a start condition.
0010	Slave Bystander	Address did not match–ignore remainder of transaction.
0011	Slave Wait	Waiting for Stop or Restart condition after sending a Not Acknowledge instruction.
0100	Master Stop2	Master completing Stop condition (SCL = 1, SDA = 1).
0101	Master Start/Restart	Master Mode sending Start condition (SCL = 1, SDA = 0).
0110	Master Stop1	Master initiating Stop condition (SCL = 1, SDA = 0).

Flash Memory

The products in the ZNEO® Z16F Series feature up to 128 KB of nonvolatile Flash memory with read/write/erase capability. The Flash memory is programmed and erased in-circuit by either user code or through the OCD.

The Flash memory array is arranged in 2 KB pages. The 2 KB page is the minimum Flash block size that is erased. The Flash memory is also divided into eight sectors, which is protected from programming and erase operations on a per sector basis.

Table 136 describes the Flash memory configuration for each device in the ZNEO Z16F Series. Table 137 lists the sector address ranges. Figure 55 displays the Flash memory arrangement.

Table 136. Flash Memory Configurations

Part Number	Internal Flash Size	Number of Pages	Program Memory Addresses	Sector Size	Number of Sectors	Pages per Sector
Z16F2811	128 KB	64	000000h–01FFFFh	16 KB	8	8
Z16F2810	128 KB	64	000000h–01FFFFh	16 KB	8	8
Z16F6411	64 KB	32	0000h–FFFFh	8 KB	8	4
Z16F3211	32 KB	16	0000h–7FFFh	4 KB	8	2

Table 137. Flash Memory Sector Addresses

Sector Number	Flash Sector Address Ranges		
	Z16F2811/Z16F2810	Z16F6411	Z16F3211
0	000000h–003FFFh	000000h–001FFFh	000000h–000FFFh
1	004000h–007FFFh	002000h–003FFFh	001000h–001FFFh
2	008000h–00BFFFh	004000h–005FFFh	002000h–002FFFh
3	00C000h–00FFFFh	006000h–007FFFh	003000h–003FFFh
4	010000h–013FFFh	008000h–009FFFh	004000h–004FFFh
5	014000h–017FFFh	00A000h–00BFFFh	005000h–005FFFh
6	018000h–01BFFFh	00C000h–00DFFFh	006000h–006FFFh
7	01C000h–01FFFFh	00E000h–00FFFFh	007000h–007FFFh

Flash Control Register Definitions

Flash Command Register

The Flash Command Register, shown in Table 139, unlocks the Flash Controller for programming and erase operations. The Write-only Flash Command Register shares its address with the Read-only Flash Status Register.

Table 139. Flash Command Register (FCMD)

Bits	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	XXH							
R/W	W							
Addr	FF_E060h							

Bit	Description
[7:0] FCMD	**Flash Command** 73h = First unlock command. 8Ch = Second unlock command. 95h = Page erase command. 63h = Mass erase command.

Note: *All other commands, or any commands out of sequence, lock the Flash Controller.

Flash Control Register

The Flash Control Register, shown in Table 141, selects how the Flash memory is accessed.

Table 141. Flash Control Register (FCTL)

Bits	7	6	5	4	3	2	1	0
Field	INFO	Reserved						
RESET	0	00h						
R/W	R/W	R						
Addr	FF_E061h							

Bit	Description
[7] INFO	**Information Area Access** This bit selects access to the information area. 0 = Information Area is not selected. 1 = Information Area is selected. The Information area is mapped into the Program memory address space at addresses 000000h through 00007Fh.
[6:0]	**Reserved** These bits are reserved and must be programmed to 0000000.

Bit	Description (Continued)
[9:8] SRCCTL	**Source Control Register** 00 = Source address does not change. 01 = Source address increments. 10 = Source address decrements. 11 = Reserved.
[7] IEOB	**Interrupt On End Of Buffer** 0 = Do not generate an interrupt when the DMA completes this buffer. 1 = Generate interrupt at the end of this buffer.
[6] TXFR	**Transfer To New List Address** This bit is used only in LINKED LIST Mode. 0 = Increment DMAxLAR by 16 at the end of this buffer. 1 = Load the DMAxLAR with the new List Address value from the descriptor.
[5] EOF	**End Of Frame** 0 = Not a End Of Frame buffer. 1 = This buffer is the end of the current frame.
[4] HALT	**Halt After This Buffer** This bit is used only in LINKED LIST Mode. 0 = Next descriptor is loaded. 1 = The DMA will halt at the end of this buffer.
[3:0] CMDSTAT	**Command Status Field** On the first transfer of a buffer, this field is placed on the CMDBUS and the CMDVALID is asserted. If the EOF bit is set, the DMA requests a status from the peripheral and places it in this field. In LINKED LIST Mode, this field is written back to the descriptor. The DMA does not use this field; it simply passes it on. The definitions of these bits are specified in each peripheral.

DMA X Transfer Length Register

The DMA X Transfer Length High and Low registers, shown in Tables 150 and 151, form a 16-bit transfer length. Each of these registers is decremented each time a DMA transfer occurs.

Table 150. DMA X Transfer Length High Register (DMAxTXLNH)

Bits	7	6	5	4	3	2	1	0
Field	DMAxTXLNH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFE412h, FFE422h, FFE432h, FFE442h							

Bit	Description (Continued)
[1] FWP	**Flash Write Protect** 0 = Programming, Page Erase and Mass Erase through user code is disabled. Flash operations are allowed through the On-Chip Debugger. 1 = Programming, Page Erase and Mass Erase are enabled for all of Flash Program Memory.
[0] RP	**Read Protect** 0 = User program code is inaccessible. Limited control features are available through the OCD. 1 = User program code is accessible. All OCD commands are enabled. This setting is the default for unprogrammed (erased) Flash.

Program Memory Address 0001h

Option bits in this space are altered to change the chip configuration at reset.

Table 162. Options Bits at Program Memory Address 0001h

Bits	7	6	5	4	3	2	1	0
Field	Reserved					MCEN	PWMHI	PWMLO
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	Program Memory 0001h							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:3]	**Reserved** These Option Bits are reserved for future use and must always be 1. This setting is the default for unprogrammed (erased) Flash.
[2] MCEN	**Motor Control Enable** 0 = Motor control pins are enabled on reset. 1 = Normal Pin operation.
[1] PWMHI	**High Side Off Initial Value** 0 = The high side off value is equal to 0. 1 = The high side off value is equal to 1.
[0] PWMLO	**Low Side Off Initial Value** 0 = The low side off value is equal to 0. 1 = The low side off value is equal to 1.

```
DBG <<- regdata[23:16]
DBG <<- regdata[15:8]
DBG <<- regdata[7:0]
DBG --> CRC[0:7]
```

Read PC. The Read Program Counter command returns the contents of the program counter.

```
DBG <-- 0000_0110
DBG --> 00h
DBG --> PC[23:16]
DBG --> PC[15:8]
DBG --> PC[7:0]
DBG --> CRC[0:7]
```

Write PC. The Write Program Counter command writes data to the program counter.

```
DBG <-- 0000_0111
DBG <-- 00h
DBG <-- PC[23:16]
DBG <-- PC[15:8]
DBG <-- PC[7:0]
DBG --> CRC[0:7]
```

Read Flags. The Read Flags command returns the contents of the CPU flags.

```
DBG <-- 0000_1000
DBG --> 00h
DBG --> flags[7:0]
DBG --> CRC[0:7]
```

Write Instruction. The Write Instruction command writes one word of Op Code to the CPU.

```
DBG <-- 0000_1001
DBG <-- opcode[15:8]
DBG <-- opcode[7:0]
DBG --> CRC[0:7]
```

Read Register. The Read Register command returns the contents of a single CPU register.

```
DBG <-- {0100,regno[3:0]}
DBG --> regdata[31:24]
DBG --> regdata[23:16]
DBG --> regdata[15:8]
DBG --> regdata[7:0]
DBG --> CRC[0:7]
```

Write Register. The Write Register command writes data to a single CPU register.

```
DBG <-- {0101,regno[3:0]}
DBG <-- regdata[31:24]
DBG <-- regdata[23:16]
DBG <-- regdata[15:8]
DBG <-- regdata[7:0]
DBG --> CRC[0:7]
```

Table 192 provides electrical characteristics and timing information for the on-chip comparator.

Table 192. Comparator Electrical Characteristics

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{COFF}	Input offset	—	5		mV	V_{DD} = 3.3 V; V_{IN} = V_{DD} ÷ 2
T_{CPROP}	Propagation delay	—	200		ns	V_{COMM} mode = 1 V V_{DIFF} = 100 mV
I_B	Input bias current			1	µA	
CMVR	Common-mode voltage range	–0.3		V_{DD}–1	V	
I_{CC}	Supply current		40		µA	V_{DD} = 3.6 V
T_{wup}	Wake up time from off state			5	µs	CINP = 0.9 V CINN= 1.0 V

Table 193 provides electrical characteristics and timing information for the on-chip operational amplifier.

Table 193. Operational Amplifier Electrical Characteristics

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{OS}	Input offset		5	15	mV	V_{DD} =3.3V; V_{CM} = V_{DD} ÷ 2
TC_{VOS}	Input offset Average Drift		1		µV/C	
I_B	Input bias current		TBD		µA	
I_{OS}	Input offset current		TBD		µA	
CMVR	Common-Mode Voltage Range	–0.3		V_{DD} – 1	V	
V_{OL}	Output Low			0.1	V	I_{SINK} = 100 µA
V_{OH}	Output High	V_{DD} – 1			V	I_{SOURCE} = 100 µA
CMRR	Common-Mode Rejection Ratio		70		dB	0 < V_{CM} < 1.4V; T_A = 25ºC

General Purpose I/O Port Input Data Sample Timing

Figure 76 displays timing of the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is then available to the ZNEO CPU on the second rising clock edge following the change of the port value. Table 195 lists the GPIO port input timing.

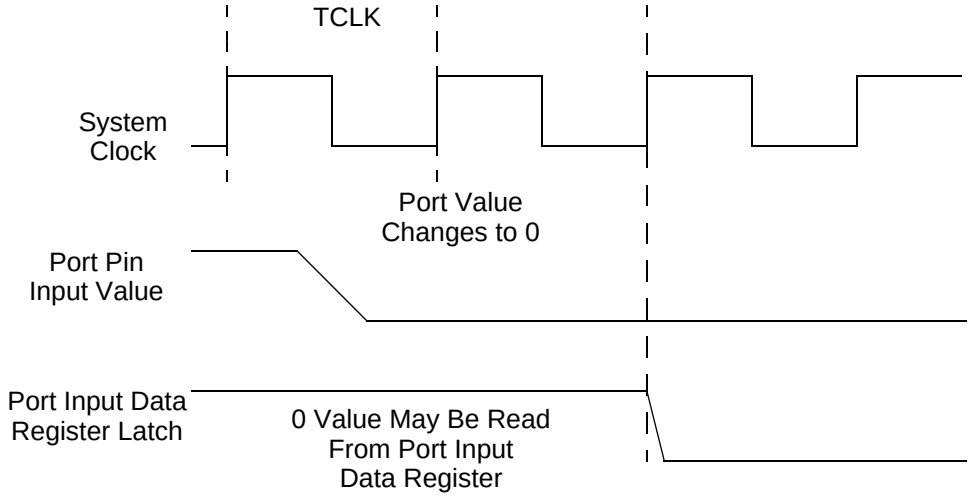

Figure 76. Port Input Sample Timing

Table 195. GPIO Port Input Timing

		Delay (ns)	
Parameter	**Description**	**Min**	**Max**
T_{SMR}	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1µs	

On-Chip Debugger Timing

Table 196 provides timing information for the DBG pin. The DBG pin timing specifications assume a 4µs maximum rise and fall time.

Table 196. On-Chip Debugger Timing

		Delay (ns)	
Parameter	**Description**	**Min**	**Max**
DBG	Debug frequency.	—	System Clock/4