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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ZNEO |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z16f2810vh20sg |

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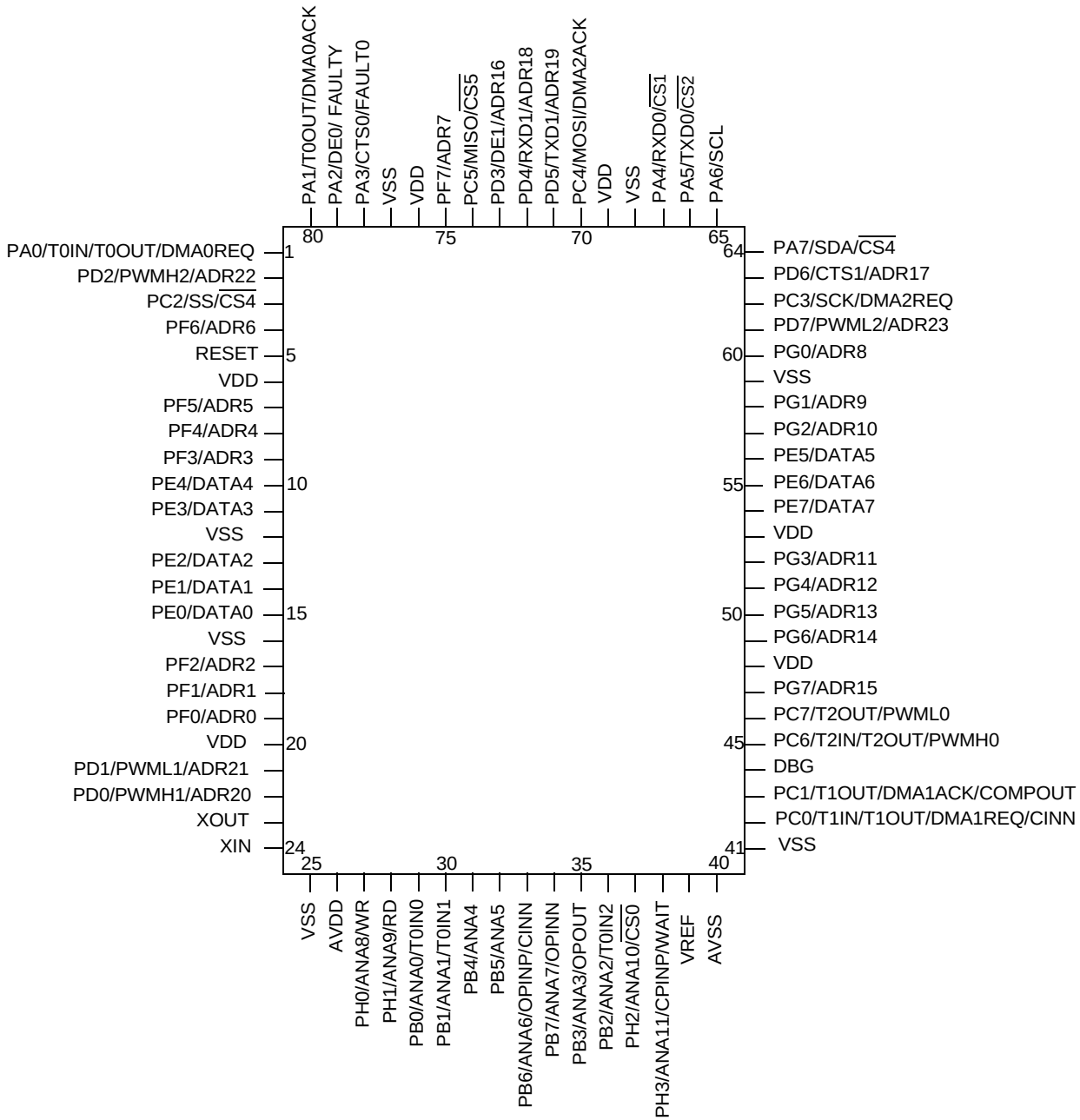



**Figure 4. ZNEO Z16F Series, 80-Pin Quad Flat Package (QFP)**

**Table 2. Signal Descriptions (Continued)**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| $\overline{WR}$ | O | Write output: This pin is the Write output signal from the external interface. Assertion of the $\overline{WR}$ signal indicates that the ZNEO CPU is performing a write operation to the external memory or peripheral. |
| $\overline{CS0}$/$\overline{CS1}$/$\overline{CS2}$ $\overline{CS3}$/$\overline{CS4}$/$\overline{CS5}$ | O | Chip select outputs: These pins are the chip select output signals from the external interface. The $\overline{CS}$ output pins have programmable polarity through the external interface control register. |
| $\overline{BHEN}$/$\overline{BLEN}$ | O | Byte high enable and byte low enable indicators. |
| $\overline{WAIT}$ | I | Wait input: Asserting this input signal will pause the CPU to provide slower external peripherals more time to complete bus transactions through the external interface. |
| **Direct Memory Access Controller** | | |
| $\overline{DMA0REQ}$ DMA1REQ DMA2REQ | I | DMA request inputs: Each of the DMA channels have an external request input which allows external peripherals to request access to the address and data buses for data transfer. |
| $\overline{DMA0ACK}$ DMA1ACK DMA2ACK | O | DMA request outputs: Each of the DMA channels have an acknowledge indicator output to notify external peripherals that their request for access to address and data buses has been approved. |
| **Inter-Integrated Circuit Controller** | | |
| SCL | I/O | Serial clock: an input or an output clock for the $I^2C$. When the GPIO pin is configured for alternate function to enable the SCL function, this pin is open-drain. |
| SDA | I/O | Serial data: This open-drain pin transfers data between the $I^2C$ and a slave. When the GPIO pin is configured for alternate function to enable the SDA function, this pin is open-drain. |
| **Enhanced Serial Peripheral Interface Controller** | | |
| $\overline{SS}$ | I/O | Slave select: This signal is an output or an input. If ZNEO is the SPI master, this pin is configured as the slave select output. If ZNEO is the SPI slave, this pin is an input slave select. |
| SCK | I/O | SPI serial clock: The SPI master supplies this pin. If the ZNEO Z16F Series device is the SPI master, this pin is an output. If the ZNEO Z16F Series device is the SPI slave, this pin is an input. |
| MOSI | I/O | Master-Out/Slave-In: This signal is the data output from the SPI master device and the data input to the SPI slave device. |
| MISO | I/O | Master-In/Slave-Out: This pin is the data input to the SPI master device and the data output from the SPI slave device. |

Table 12 shows the External Chip Select Control Registers Low for $\overline{CS1}$(EXTSC1L). This register sets the number of wait states for Chip Select 1. Waits are only added if the chip select is enabled.

**Table 12. External Chip Select Control Registers Low for $\overline{CS1}$ (EXTCS1L)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RESERVED | | PR1WAIT | | CS1WAIT | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Addr | FF_(E075)H | | | | | | | |

| Bit | Description |
|---|---|
| [7:6] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [5:4]<br>PR1WAIT[2:0] | **Post Read Wait Selection**<br>00 = 0 wait state.<br>01 = 1 wait state.<br>10 = 2 wait states.<br>11 = 3 wait states. |
| [3:0]<br>CS1WAIT | **Chip Select 1 Wait Selection**<br>0000 = 0 wait state.<br>0001 = 1 wait state.<br>0010 = 2 wait states.<br>0011 = 3 wait states.<br>0100 = 4 wait states.<br>0101 = 5 wait states.<br>0110 = 6 wait states.<br>0111 = 7 wait states.<br>1000 = 8 wait states.<br>1001 = 9 wait states.<br>1010 = 10 wait states.<br>1011 = 11 wait states.<br>1100 = 12 wait states.<br>1101 = 13 wait states.<br>1110 = 14 wait states.<br>1111 = 15 wait states. |

Table 13 lists the External Chip Select Control Registers Low for $\overline{CS2}$ to $\overline{CS5}$ (EXTCSxL). This register sets the number of wait states for chip selects 2 through 5. Waits are only added if the chip select is enabled.

**Table 13. External Chip Select Control Registers Low for $\overline{CS2}$ to $\overline{CS5}$ (EXTCSxL)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RESERVED | | PRxWAIT | | CSxWAIT | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Addr | FF_(E077, E079, E07B, E07D)H | | | | | | | |

| Bit | Description |
|---|---|
| [7:6] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [5:4]<br>PRxWAIT[2:0] | **Post Read Wait Selection**<br>00 = 0 wait state.<br>01 = 1 wait state.<br>10 = 2 wait states.<br>11 = 3 wait states. |
| [3:0]<br>CSxWAIT | **Chip Select x Wait Selection**<br>0000 = 0 wait state.<br>0001 = 2 wait state.<br>0010 = 4 wait states.<br>0011 = 6 wait states.<br>0100 = 8 wait states.<br>0101 = 10 wait states.<br>0110 = 12 wait states.<br>0111 = 14 wait states.<br>1000 = 16 wait states.<br>1001 = 18 wait states.<br>1010 = 20 wait states.<br>1011 = 22 wait states.<br>1100 = 24 wait states.<br>1101 = 26 wait states.<br>1110 = 28 wait states.<br>1111 = 30 wait states. |

# System Reset

During a System Reset, the ZNEO Z16F Series device is held in Reset for 66 cycles of the IPO. At the beginning of Reset, all GPIO pins are configured as inputs. All GPIO programmable pull-ups are disabled.

At the start of a System Reset, the motor control PWM outputs are forced to high-impedance momentarily. When the option bits that control the off-state have been properly evaluated, the PWM outputs are forced to the programmed off-state.

During Reset, the ZNEO CPU and on-chip peripherals are nonactive; however, the IPO and WDT oscillator continue to run. During the first 50 clock cycles, the internal option bit registers are initialized, after which the system clock for the core and peripherals begins operating. The ZNEO CPU and on-chip peripherals remain nonactive through the next 16 cycles of the system clock, after which the internal reset signal is deasserted.

On Reset, control registers within the register file that have a defined reset value are loaded with their reset values. Other control registers (including the Flags) and general-purpose RAM are undefined following Reset. The ZNEO CPU fetches the Reset vector at program memory address 0004h and loads that value into the program counter. Program execution begins at the Reset vector address.

Table 19 lists the System Reset sources as a function of the operating mode. The following text provides more detailed information about the individual Reset sources. Note that a POR/VBO event always has priority over all other possible reset sources to ensure that a full System Reset occurs.

**Table 19. System Reset Sources and Resulting Reset Action**

| Operating Mode | System Reset Source | Action |
|---|---|---|
| NORMAL or HALT modes | POR/VBO | System Reset |
| | WDT time-out when configured for Reset | System Reset |
| | $\overline{\text{RESET}}$ pin assertion | System Reset |
| | Write RSTSCR[0] to 1 | System Reset |
| | Fault detect logic reset | System Reset |
| Stop Mode | POR/VBO | System Reset |
| | $\overline{\text{RESET}}$ pin assertion | System Reset |
| | Fault detect logic reset | System Reset |

## Power-On Reset

Each device in the ZNEO Z16F Series contains an internal POR circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold

## Port A-K Data Direction Registers

The Port A-K Data Direction registers, shown in Table 27, configure the specified port pins as either inputs or outputs.

**Table 27. Port A-K Data Direction Registers (PxDD)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DD7 | DD6 | DD5 | DD4 | DD3 | DD2 | DD1 | DD0 |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Addr | FF_E102, FF_E112, FF_E122, FF_E132, FF_E142, FF_E152, FF_E162, FF_E172, FF_E182, FF_E192 | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>DD[7:0] | **Data Direction**<br>These bits control the direction of the associated port pin. Port alternate function operation overrides the data direction register setting.<br>0 = Output<br>Data in the Port A-K Output Data Register is driven onto the port pin.<br>1 = Input<br>The port pin is sampled and the value written into the Port A-K Input Data Register. The output driver is high impedance. |

**Table 69. PWM 0–2 H/L Duty Cycle Low Byte Register (PWMH*x*DL, PWML*x*DL)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | DUTYL | | | | | | | |
| RESET | XXH | | | | | | | |
| R/W | R/W | | | | | | | |
| Addr | FF_E391h, FF_E393h, FF_E395h, FF_E397h, FF_E399h, FF_E39Bh | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>DUTYL | **PWM Duty Cycle High and Low Bytes**<br>The lower byte of two bytes {DUTYH[7:0], DUTYL[7:0]} that form a 14-bit signed value; bits 5 and 6 of the High byte are always 0. The value is compared to the current 12-bit PWM count. |

## PWM Control 0 Register

The PWM Control 0 Register (PWMCTL0) controls PWM operation.

**Table 70. PWM Control 0 Register (PWMCTL0)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PWMOFF | OUTCTL | ALIGN | Reserved | ADCTRIG | Reserved | READY | PWMEN |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Addr | FF_E380h | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>PWMOFF | **Place PWM Outputs in Off State**<br>0 = Disable modulator control of PWM pins. Outputs are in predefined off state; not dependent on the Reload event.<br>1 = Reenable modulator control of PWM pins at next PWM Reload event. |
| [6]<br>OUTCTL | **PWM Output Control**<br>0 = PWM outputs are controlled by the pulse-width modulator.<br>1 = PWM outputs selectively disabled (set to off-state) according to values in the OUT*x* bits of the PWMOUT Register. |
| [5]<br>ALIGN | **PWM Edge Alignment**<br>0 = PWM outputs are edge aligned.<br>1 = PWM outputs are center aligned. |
| [4] | **Reserved**<br>This bit is reserved and must be programmed to 0. |

set by the software. In the LIN Slave Mode, the LinState field is updated by hardware as the slave moves through the Wait for Break, AutoBaud and Active states.

The noise filter is also required to be enabled and configured when interfacing to a LIN bus.

## LIN Master Mode Operation

LIN Master Mode is selected by setting the bits LMST = 1, LSLV = 0, ABEN = 0, LinState[1:0] = 11b. If the LIN bus protocol indicates the bus is required go into the LIN Sleep state, the LinState[1:0] bits must be set = 00b by the software.

The Break is the first part of the message frame transmitted by the master, consisting of at least 13 bit periods of logical zero on the LIN bus. During initialization of the LIN master, the duration (in bit times) of the Break is written to the TxBreakLength field of the LIN Control Register. The transmission of the Break is performed by setting the SBRK bit in the Control 0 Register. The LIN-UART starts the Break after the SBRK bit is set and any character transmission currently underway has completed. The SBRK bit is deasserted by hardware after the break is completed.

The Synch character is transmitted by writing a 55h to the Transmit Data Register (TDRE must be 1 before writing). The Synch character is not transmitted by the hardware until after the Break is complete.

The Identifier character is transmitted by writing the appropriate value to the Transmit Data Register (TDRE must be 1 before writing).

If the master is sending the response portion of the message, these data and checksum characters are written to the Transmit Data Register when the TDRE bit asserts.

If the Transmit Data Register is written after TDRE asserts, but before TXE asserts, the hardware inserts one or two Stop bits between each character as determined by the Stop bit in the Control 0 Register. Additional idle time occurs between characters if TXE asserts before the next character is written.

## LIN Sleep Mode

While the LIN bus is in the Sleep state, the CPU is in either low power Stop Mode, in Halt Mode, or in normal operational state. Any device on the LIN bus issues a Wake-up message (transmits an 80h character) if it requires the master to initiate a LIN message frame. Following the Wake-up message, the master wakes up and initiates a new message.

If the CPU is in Stop Mode, the LIN-UART is not active and the Wake-up message must be detected by a GPIO edge detect Stop Mode Recovery. The duration of the Stop Mode Recovery sequence may preclude making an accurate measurement of the Wake-up message duration.

If the CPU is in HALT or OPERATIONAL Mode, the LIN-UART (if enabled) times the duration of the Wake-up and provides an interrupt following the end of the break sequence if the duration is ≥ 4 bit times. The total duration of the Wake-up message in bit times is

| Bit | Description (Continued) |
|---|---|
| [5]<br>OE | **Receive Data and Autobaud Overrun Error**<br>This bit is set just as in normal UART operation if a receive data overrun error occurs. This bit is also set during LIN slave autobaud if the BRG counter overflows before the end of the autobaud sequence, indicating that the receive activity was not an autobaud character or the master baud rate is too slow. The ATB status bit will also be set in this case. This bit is cleared by reading the Receive Data Register.<br>0 = No autobaud or data overrun error occurred.<br>1 = An autobaud or data overrun error occurred. |
| [4]<br>FE | **Framing Error**<br>This bit indicates that a framing error (no Stop bit following data reception) is detected. Reading the Receive Data Register clears this bit.<br>0 = No framing error occurred.<br>1 = A framing error occurred. |
| [3]<br>BRKD | **Break Detect**<br>This bit is set in LIN Mode if (a) in LinSleep state and a break of at least 4 bit times occurred (Wake-up event) or (b) in Slave Wait Break state and a break of at least 11 bit times occurred (Break event), or (c) in Slave Active state and a break of at least 10 bit times occurs. Reading the Status 0 Register or the Receive Data Register clears this bit.<br>0 = No LIN break occurred.<br>1 = A LIN break occurred. |
| [2]<br>TDRE | **Transmitter Data Register Empty**<br>This bit indicates that the Transmit Data Register is empty and ready for additional data. Writing to the Transmit Data Register resets this bit.<br>0 = Do not write to the Transmit Data Register.<br>1 = The Transmit Data Register is ready to receive an additional byte to be transmitted. |
| [1]<br>TXE | **Transmitter Empty**<br>This bit indicates that the transmit shift register is empty and character transmission is finished.<br>0 = Data is currently transmitting.<br>1 = Transmission is complete. |
| [0]<br>ATB | **LIN Slave AutoBaud Complete**<br>This bit is set in LIN Slave Mode when an autobaud character is received. If the ABIEN bit is set in the LIN Control Register then a receive interrupt is generated when this bit is set. Reading the Status 0 Register clears this bit. This bit will be 0 in LIN Master Mode. |

## LIN-UART Mode Select and Status Register

The LIN-UART Mode Select and Status Register contains mode select and status bits. The four Mode Status options in Table 84 are further described in Tables 85 through 88.

**Table 84. LIN-UART Mode Select and Status Register (UxMDSTAT)**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | MSEL | | | Mode Status | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R | R | R | R | R |
| Addr | FF–E204h, FF–E214h | | | | | | | |

| Bit | Description |
|---|---|
| [7:5] MSEL | **Mode Select**<br>This R/W field determines which control register is accessed when performing a Write or Read to the UART Control 1 Register address. This field also determines which status is returned in the mode status field when reading this register.<br>000 = Multiprocessor and normal UART control/status<br>001 = Noise Filter control/status<br>010 = LIN Protocol control/status<br>011–110: Reserved<br>111 = LIN-UART hardware revision (allows hardware revision to be read in the mode status field) |
| [4:0] Mode Status | **Mode Status**<br>This read-only field returns status corresponding to the mode selected by MSEL as follows:<br>000: MULTIPROCESSOR and NORMAL UART Mode status = {NE, 0, 0, NEWFRM, MPRX}<br>001: Noise filter status = {NE, 0,0,0,0}<br>010: LIN Mode status = {NE, RxBreakLength[3:0]}<br>011–110: Reserved = {0, 0, 0, 0, 0}<br>111: LIN-UART hardware revision |

**Table 108. ESPISTATE Values and Description (Continued)**

| ESPISTATE Value | Description |
|---|---|
| 10_1100 | Bit 6 Receive |
| 10_1101 | Bit 6 Transmit |
| 10_1010 | Bit 5 Receive |
| 10_1011 | Bit 5 Transmit |
| 10_1000 | Bit 4 Receive |
| 10_1001 | Bit 4 Transmit |
| 10_0110 | Bit 3 Receive |
| 10_0111 | Bit 3 Transmit |
| 10_0100 | Bit 2 Receive |
| 10_0101 | Bit 2 Transmit |
| 10_0010 | Bit 1 Receive |
| 10_0011 | Bit 1 Transmit |
| 10_0000 | Bit 0 Receive |
| 10_0001 | Bit 0 Transmit |

## ESPI Baud Rate High and Low Byte Registers

The ESPI Baud Rate High and Low Byte registers, shown in Tables 109 and 110, combine to form a 16-bit reload value, BRG[15:0], for the ESPI Baud Rate Generator. The ESPI baud rate is calculated using the following equation:

$$\text{SPI Baud Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG}[15:0]}$$

Minimum baud rate is obtained by setting BRG[15:0] to 0000h for a clock divisor value of (2 x 65536 = 131072)

When the ESPI function is disabled, the BRG functions as a basic 16-bit timer with interrupt on time-out.

Observe the following procedure to configure the BRG as a general purpose timer with interrupt on time-out:

1. Disable the ESPI by setting ESPIEN[1:0] = 00 in the SPI Control register.
2. Load the appropriate 16-bit count value into the ESPI Baud Rate High and Low Byte registers.
3. Enable the BRG timer function and associated interrupt by setting the BRGCTL bit in the ESPI Control register to 1.

0 for General Call Address). For a General Call Address, the I2C Controller automatically responds during the address acknowledge phase with the value in the NAK bit of the I2CCTL Register. If software processes the data bytes associated with the GCA bit, the IRM bit is optionally set following the SAM interrupt to allow software to examine each received data byte before deciding to set or clear the NAK bit. A Start byte will not be acknowledged (requirement the I2C specification).

**Software Address Recognition Mode.** To disable the hardware address recognition, the IRM bit must be set = 1 prior to the reception of the address byte(s). When IRM = 1 each received byte generates a receive interrupt (RDRF = 1 in the I2CISTAT Register). Software must examine each byte and determine whether to set or clear the NAK bit. The Slave holds SCL Low during the acknowledge phase until software responds by writing to the I2CCTL Register. The value written to the NAK bit is used by the controller to drive the I2C Bus, then releasing the SCL. The SAM and GCA bits are not set when IRM = 1 during the address phase, but the RD bit is updated based on the first address byte.

## Slave Transaction Diagrams

In the following transaction diagrams, shaded regions indicate data transferred from the Master to the Slave and unshaded regions indicate data transferred from the Slave to the Master. The transaction field labels are defined as follows:

S: Start

W: Write

A: Acknowledge

$\overline{A}$: Not Acknowledge

P: Stop

## Slave Receive Transaction with 7-Bit Address

The data transfer format for writing data from Master to Slave in 7-bit address Mode is shown in Figure 47. The following procedure describes the I2C Master/Slave Controller operating as a Slave in 7-bit address Mode, receiving data from the bus Master.

| S | Slave Address | W=0 | A | Data | A | Data | A | Data | A/$\overline{A}$ | P/S |
|---|---|---|---|---|---|---|---|---|---|---|

**Figure 48. Data Transfer Format, Slave Receive Transaction with 7-Bit Addressing**

1. Software configures the controller for operation as a Slave in 7-Bit Address Mode as follows.
   a. Initialize the MODE field in the I2C Mode Register for either Slave Only Mode or Master/Slave Mode with 7-Bit Addressing.

**Table 123. Watchdog Timer Approximate Time-Out Delays**

| WDT Reload Value | WDT Reload Value | Approximate Time-Out Delay (with 10 kHz typical WDT oscillator frequency) | |
|---|---|---|---|
| (Hex) | (Decimal) | Typical | Description |
| 0400 | 1024 | 102.4 ms | Reset value time-out delay |
| FFFF | 65,536 | 6.55 s | Maximum time-out delay |

## Watchdog Timer Refresh

When enabled first, the WDT is loaded with the value in the Watchdog Timer Reload registers. The WDT then counts down to 0000h unless a WDT instruction is executed by the ZNEO CPU. Execution of the WDT instruction causes the downcounter to be reloaded with the WDT reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When the ZNEO Z16F Series device is operating in DEBUG Mode (through the OCD), the WDT is continuously refreshed to prevent spurious WDT time-outs.

## Watchdog Timer Time-Out Response

The WDT times out when the counter reaches 0000h. A time-out of the WDT generates either a system exception or a short reset. The WDT_RES option bit determines the time-out response of the WDT. For information about programming of the WDT_RES option bit, see the Option Bits chapter on page 292.

### WDT System Exception in Normal Operation

If configured to generate a system exception when a time-out occurs, the WDT issues an exception request to the interrupt controller. The ZNEO CPU responds to the request by fetching the System Exception vector and executing code from the vector address. After time-out and system exception generation, the WDT is reloaded automatically and continues counting.

### WDT System Exception in Stop Mode

If configured to generate a system exception when a time-out occurs and the ZNEO Z16F Series device is in Stop Mode, the WDT automatically initiates a Stop Mode Recovery and generates a system exception request. Both the WDT status bit and the Stop bit in the Reset Status and Control Register are set to 1 following WDT time-out in Stop Mode. For detailed information, see the Reset and Stop Mode Recovery chapter on page 56.

| Bit | Description (Continued) |
|---|---|
| [4]<br>CPISEL | **Comparator Input Select**<br>0 = PortB6 provides the comparator - input.<br>1 = PortC0 provides the comparator - input. |
| [3]<br>CMPIRQ | **Comparator Interrupt Edge Select**<br>0 = Interrupt Request on Comparator Rising Edge.<br>1 = Interrupt Request on Comparator Falling Edge. |
| [2]<br>CMPIV | **PWM Fault Comparator Polarity**<br>0 = PWM Fault is active when cp+ > cp-<br>1 = PWM Fault is active when cp- > cp+ |
| [1]<br>CMPOUT | **Comparator Output Value**<br>0 = Comparator output is logical 0.<br>1 = Comparator output is logical 1. |
| [0]<br>CMPEN | **Comparator Enable**<br>0 = Comparator is disabled.<br>1 = Comparator is enabled. |

# DMA Controller

The ZNEO Z16F Series' four DMA channels are used to transfer data from memory to memory, memory to peripherals, peripherals to memory, or peripherals to peripherals.

## DMA Features

The features of the DMA Controller include:

- Four independent DMA channels.
- Memory <=> memory, memory <=> peripheral, peripheral <=> memory, peripheral <=> peripheral transfers
- Direct or Linked List modes of operation
- Byte, word, or quad operation
- DMA and CPU bandwidth sharing control
- Up to 64 K transfers (64 KByte, 64 KWord or 64 KQuad)
- External DMA request and DMA acknowledge signals

### DMA Block Diagram

Figure 56 shows the blocks that comprise the DMA Controller.

| Bit | Description (Continued) |
|---|---|
| [1]<br>FWP | **Flash Write Protect**<br>0 = Programming, Page Erase and Mass Erase through user code is disabled. Flash operations are allowed through the On-Chip Debugger.<br>1 = Programming, Page Erase and Mass Erase are enabled for all of Flash Program Memory. |
| [0]<br>RP | **Read Protect**<br>0 = User program code is inaccessible. Limited control features are available through the OCD.<br>1 = User program code is accessible. All OCD commands are enabled. This setting is the default for unprogrammed (erased) Flash. |

## Program Memory Address 0001h

Option bits in this space are altered to change the chip configuration at reset.

**Table 162. Options Bits at Program Memory Address 0001h**

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | | MCEN | PWMHI | PWMLO |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Addr | Program Memory 0001h | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:3] | **Reserved**<br>These Option Bits are reserved for future use and must always be 1. This setting is the default for unprogrammed (erased) Flash. |
| [2]<br>MCEN | **Motor Control Enable**<br>0 = Motor control pins are enabled on reset.<br>1 = Normal Pin operation. |
| [1]<br>PWMHI | **High Side Off Initial Value**<br>0 = The high side off value is equal to 0.<br>1 = The high side off value is equal to 1. |
| [0]<br>PWMLO | **Low Side Off Initial Value**<br>0 = The low side off value is equal to 0.<br>1 = The low side off value is equal to 1. |

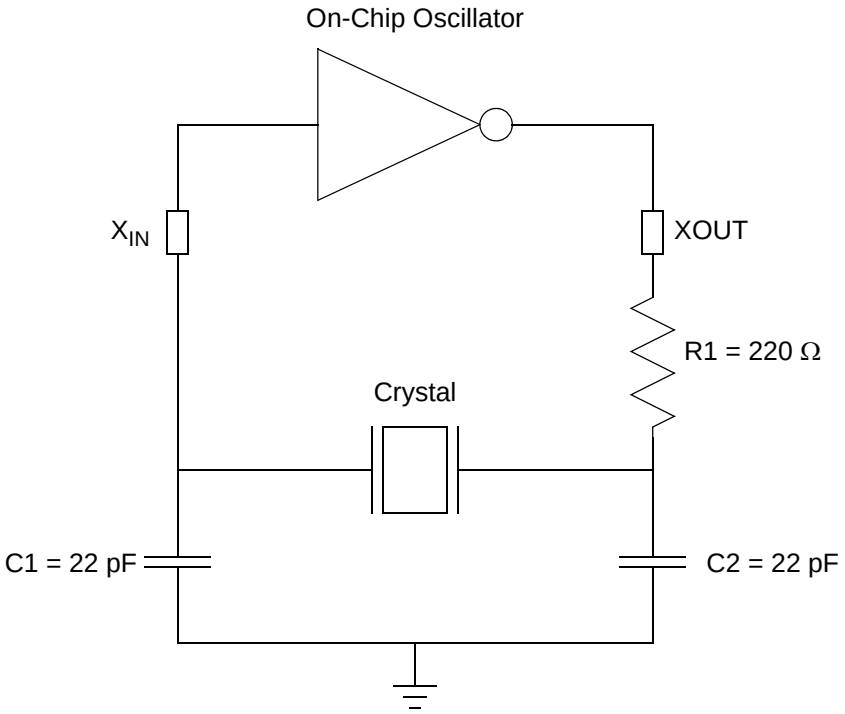



**Figure 70. Recommended 20 MHz Crystal Oscillator Configuration**

**Table 181. Recommended Crystal Oscillator Specifications (20 MHz Operation)**

| Parameter | Value | Units | Comments |
|---|---|---|---|
| Frequency | 20 | MHz | |
| Resonance | Parallel | | |
| Mode | Fundamental | | |
| Series Resistance ($R_S$) | 25 | Ω | Maximum |
| Load Capacitance ($C_L$) | 20 | pF | Maximum |
| Shunt Capacitance ($C_0$) | 7 | pF | Maximum |
| Drive Level | 1 | mW | Maximum |

# Packaging

Zilog's ZNEO Z16F Series is comprised of the Z16FMC28, Z16FMC32 and Z16FMC64 MCUs, which are based on the ZNEO CPU and are available in the 64-pin Low-Profile Quad Flat Package (LQFP).

Current diagrams for this package are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

## Ordering Information

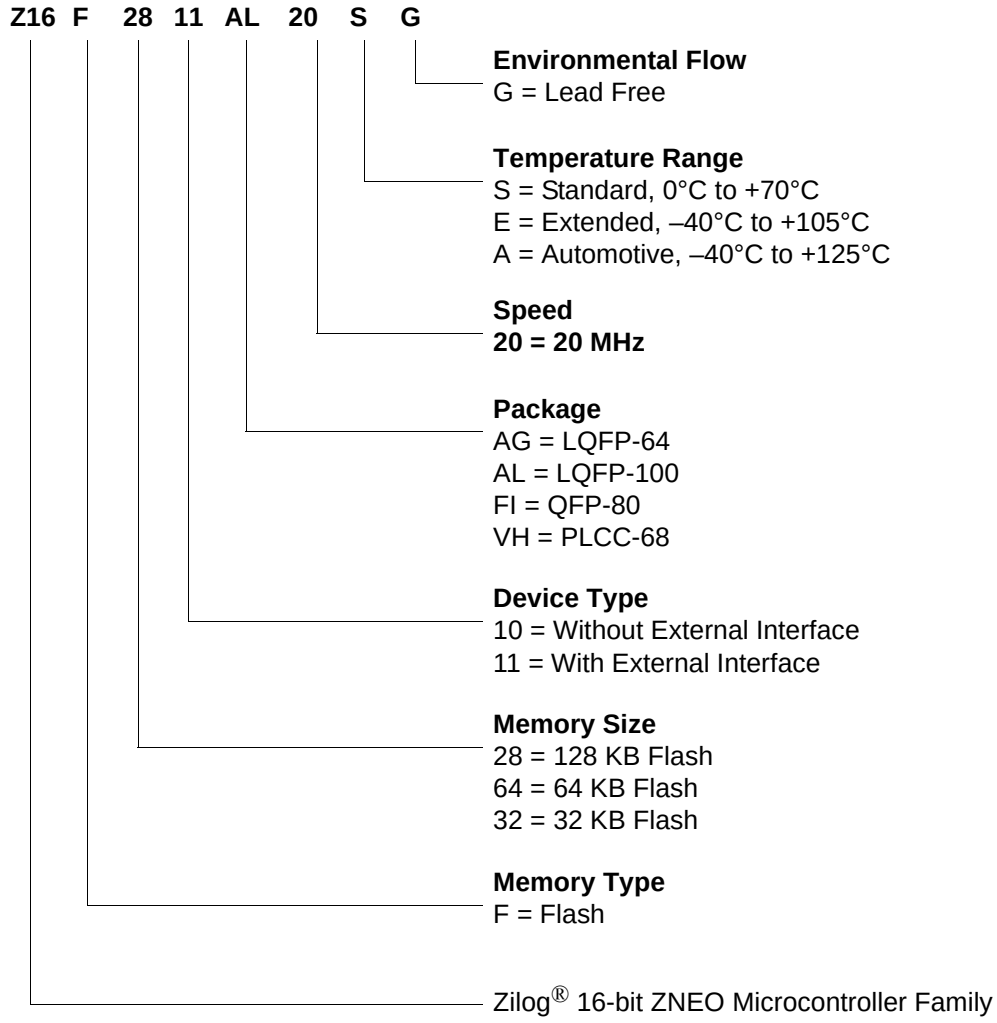
Table 202 identifies the basic features and package styles available for each device within the ZNEO product line.

**Table 202. ZNEO Part Selection Guide**

| Part Number | Flash (KB) | RAM (KB) | External Interface | I/O | Multi-Channel Timers with PWM | Standard Timers with PWM | ADC Inputs | UARTs with LIN and IrDA | $I^2C$ Master/Slave | ESPI | 64/68-pin packages | 80-pin package | 100-pin package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Z16F2811 | 128 | 4 | Yes | 76 | 1 | 3 | 12 | 2 | 1 | 1 | | | X |
| | 128 | 4 | Yes | 60 | 1 | 3 | 12 | 2 | 1 | 1 | | X | |
| Z16F2810 | 128 | 4 | No | 60 | 1 | 3 | 12 | 2 | 1 | 1 | | X | |
| | 128 | 4 | No | 46 | 1 | 3 | 12 | 2 | 1 | 1 | X | | |
| Z16F6411 | 64 | 4 | Yes | 76 | 1 | 3 | 12 | 2 | 1 | 1 | | | X |
| | 64 | 4 | Yes | 60 | 1 | 3 | 12 | 2 | 1 | 1 | | X | |
| Z16F3211 | 32 | 2 | Yes | 76 | 1 | 3 | 12 | 2 | 1 | 1 | | | X |
| | 32 | 2 | Yes | 60 | 1 | 3 | 12 | 2 | 1 | 1 | | X | |

You can order the ZNEO Z16F Series from Zilog® by providing the part numbers listed in Table 203. For more information regarding ordering, contact your local Zilog sales office. Our website (www.zilog.com) lists all regional offices and provides additional information about ZNEO Z16F Series product.

## Part Number Suffix Designations




Note: Packages are not available for all memory sizes. See the Ordering Information section on page 356 for available packages.

## Precharacterization Product

The product represented by this document is newly introduced and Zilog® has not completed the full characterization of the product. The document states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery might be uncertain at times, due to start-up yield issues. For more information, please visit www.zilog.com.