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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2811al20sg

Feb 2007	06	Independent and Complementary PWM Outputs	Corrected PWM Registers. Updated Edge-Aligned PWM Output figure.	117
		Electrical Characteristics	Replaced 105°C with 125°C in Tables 185 through 192. Added Figures 73 through 75.	337
		I2C Master/Slave Controller	Changes to Software Control of I2C Transactions section.	209
		Packaging	Updated Part Number Suffix Designations section.	359
		Enhanced Serial Peripheral Interface	Throughput section modified.	181
Jul 2006	05	External Interface, General-Purpose Input/Output, DMA Controller, Option Bits, On-Chip Debugger and Electrical Characteristics	Modifications done in the following chapters: External Interface, GPIO, DMA Controller, Option bits, on-chip debugger and Electrical characteristics.	37, 66, 267, 292, 298, 337
		Ordering Information	Ordering Information modified.	356
Jan 2006	04	All	Changed zneo to ZNEO in the entire document.	All
		All	Added TM symbol to ZNEO.	All
		Signal and Pin Descriptions, Interrupt Controller and Analog Functions	Modifications done to following chapters: Pin description, Interrupt controller and Analog functions.	7, 80, 242
		Ordering Information	Ordering Information modified.	356

External Interface Timing

The following sections describe the ZNEO Z16F Series MCU ô s external interface timing.

External Interface Write Timing, Normal Mode

Figure 11 and Table 14 provide timing information for the external interface performing a write operation. In Figure 11, it is assumed that the wait state generator is configured to provide 1 wait state during write operations. The external $\overline{\text{WAIT}}$ input pin is generating an additional Wait period. It is assumed in Figure 11 that the chip select ($\overline{\text{CS}}$) signal has been configured for active Low operation. Though the internal system clock is not provided as an external signal, it provides a useful reference for control signal events.

Note: At the completion of a Write cycle, the deassertion of the $\overline{\text{WR}}$ signal is fed back from the pin and used on chip to control the deassertion of the data, $\overline{\text{CS}}$, address and byte enable signals to assure proper timing of the data hold.

Table 14. External Interface Timing for a Write Operation, Normal Mode

		Delay (ns)	
Parameter	Abbreviation	Minimum	Maximum
T_1	SYS CLK Rise to Address Valid Delay		10
T_2	$\overline{\text{WR}}$ Rise to Address Output Hold Time	3	
T_3	SYS CLK Rise to Data Valid Delay		10
T_4	$\overline{\text{WR}}$ Rise to Data Output Hold Time	3	
T_5	SYS CLK Rise to $\overline{\text{CS}}$ Assertion Delay		10
T_6	$\overline{\text{WR}}$ Rise to $\overline{\text{CS}}$ Deassertion Hold Time	3	
T_7	SYS CLK Rise to $\overline{\text{WR}}$ Assertion Delay		$1/2T_{CLK}$ +10
T_8	SYS CLK Rise to $\overline{\text{WR}}$ Deassertion Hold Time	3	
T_9	$\overline{\text{WAIT}}$ Input Pin Assertion to X_{IN} Rise Setup Time	1	
T_{10}	$\overline{\text{WAIT}}$ Input Pin Deassertion to X_{IN} Rise Setup Time	1	
T_{11}	SYS CLK Rise to $\overline{\text{DMAACK}}$ Assertion Delay		10
T_{12}	SYS CLK Rise to $\overline{\text{DMAACK}}$ Deassertion Hold Time	3	
T_{13}	SYS CLK Rise to $\overline{\text{BHEN}}$ or $\overline{\text{BLEN}}$ Assertion Delay		10
T_{14}	$\overline{\text{WR}}$ Rise to $\overline{\text{BHEN}}$ or $\overline{\text{BLEN}}$ Deassertion Hold Time	3	

Reset and Stop Mode Recovery

The reset controller within the ZNEO® Z16F Series controls RESET and Stop Mode Recovery operation. In a typical operation, the following events causes a Reset to occur:

Power-On Reset

Voltage Brown-Out

WDT time-out (when configured through the WDT_RES option bit to initiate a Reset)

External $\overline{\text{RESET}}$ pin assertion

OCD initiated Reset (OCDCTL[0] set to 1)

Fault detect logic

When ZNEO Z16F Series is in Stop Mode, a Stop Mode Recovery is initiated by either of the following operations:

WDT time-out

GPIO port input pin transition on an enabled Stop Mode Recovery source

Reset Types

The ZNEO Z16F Series provides two different types of Reset operation (System Reset and Stop Mode Recovery). The type of Reset is a function of both the current operating mode of the ZNEO Z16F Series device and the source of the Reset. Table 18 lists the types of Reset and their operating characteristics.

Table 18. Reset and Stop Mode Recovery Characteristics and Latency

	Reset Characteristics and Latency		
Reset Type	Peripheral Control Registers	ZNEO CPU	Reset Latency (Delay)
System Reset	Reset (as applicable)	Reset	A minimum of 66 internal precision oscillator cycles.
Stop Mode Recovery	Unaffected, except RST-SRC and OSCCTL registers	Reset	A minimum of 66 internal precision oscillator cycles.

tem clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, the ZNEO Z16F Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state 16 system clock cycles following $\overline{\text{RESET}}$ pin deassertion. If the $\overline{\text{RESET}}$ pin is released before the System Reset time-out, the $\overline{\text{RESET}}$ pin is driven Low by the chip until the completion of the time-out as described in the next section. In Stop Mode, the digital filter is bypassed as the system clock is disabled.

Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status and Control Register is set to 1.

External Reset Indicator

During System Reset, the $\overline{\text{RESET}}$ pin functions as an open drain (active Low) RESET Mode indicator in addition to the input functionality. This Reset output feature allows a ZNEO Z16F Series device to Reset other components to which it is connected, even if the Reset is caused by internal sources such as POR, VBO or WDT events and as an indication of when the reset sequence completes.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 18 on page 56 has elapsed.

User Reset

A System Reset is initiated by setting RSTSCR[0]. If the Write was caused by the OCD, the OCD is not Reset.

Fault Detect Logic Reset

Fault detect circuitry exists to detect illegal state changes which is caused by transient power or electrostatic discharge events. When such a fault is detected, a system reset is forced. Following the system reset, the FLTD bit in the Reset Status and Control Register is set.

Stop Mode Recovery

Stop Mode is entered by execution of a Stop instruction by the ZNEO CPU. For detailed information about Stop Mode, see the Low-Power Modes chapter on page 64. During Stop Mode Recovery, the device is held in Reset for 66 cycles of the internal precision oscillator.

Stop Mode Recovery only affects the contents of the the Reset Status and Control Register (see page 62) and the Oscillator Control Register (see page 333). Stop Mode Recovery does not affect any other values in the register file, including the stack pointer, register pointer, flags, peripheral control registers and general-purpose RAM.

The ZNEO CPU fetches the Reset vector at program memory addresses 0004h-0007h and loads that value into the program counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the Stop bit in the Reset Status and Control Register is set to 1. Table 20 lists the Stop Mode Recovery sources and resulting actions. The following text provides more detailed information about each of the Stop Mode Recovery sources.

Table 20. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
Stop Mode	WDT time-out when configured for Reset	Stop Mode Recovery
	WDT time-out when configured for System Exception	Stop Mode Recovery followed by WDT System Exception
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery

Stop Mode Recovery Using WDT Time-Out

If the WDT times out during Stop Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status and Control Register, the WDT and Stop bits are set to 1. If the WDT is configured to generate a System Exception on time-out, the ZNEO CPU services the WDT System Exception following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins is configured as a Stop Mode Recovery input source. If any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery. The GPIO Stop Mode Recovery signals are filtered to reject pulses less than 10 ns (typical) in duration. In the Reset Status and Control Register, the Stop bit is set to 1.

Short pulses on the port pin initiates Stop Mode Recovery without initiating an interrupt (if enabled for that pin).

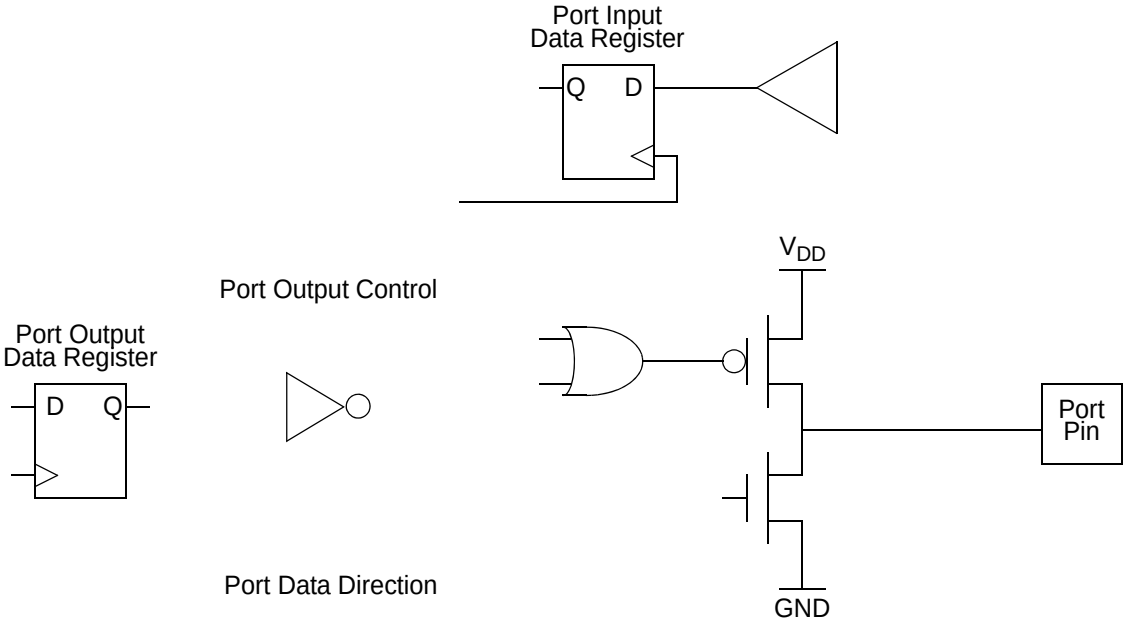

Figure 18. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many GPIO port pins are used for GPIO and to provide access to the on-chip peripheral functions such as timers, serial communication devices and external data and address bus. The Port A ï K alternate function registers configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (I/O) is passed from the Port A ï K data direction registers to the alternate function assigned to this pin. Table 24 on page 68 lists the alternate functions associated with each port pin.

For detailed information about enabling the external interface data signals, see the External Interface chapter on page 37. When the external interface data signals are enabled for an 8-bit port, the other GPIO functionality including alternate functions cannot be used.

Bit	Description (Continued)
[5] DIV0	Divide by Zero If this bit is 1, a divide operation was executed where the denominator was zero. Writing 1 to this bit clear it to 0.
[4] DIVOVF	Divide Over Flow If this bit is 1, a divide overflow occurred. A divide overflow happens when the result is greater than FFFFFFFFh. Writing 1 to this bit clears it to 0.
[3] ILL	Illegal Instruction If this bit is 1, an illegal instruction occurred. Writing 1 to this bit clears it to 0.
[2:0]	Reserved These bits are reserved and must be programmed to 000.

Table 42. System Excepti on Register Low (SYSEXCPL)

Bits	7	6	5	4	3	2	1	0
Field	Reserved					WDTOSC	PRIOSC	WDT
RESET	0	0	0	0	0	0	0	0
R/W	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Addr	FF_E021h							

Bit	Description
[7:3]	Reserved These bits are reserved and must be programmed to 00000.
[2] WDTOSC	WDT Oscillator Fail If this bit is 1, a WDT oscillator fail exception occurred. Writing 1 to this bit clears it to 0.
[1] PRIOSC	Primary Oscillator Fail If this bit is 1, a primary oscillator fail exception occurred. Writing 1 to this bit clears it to 0.
[0] WDT	Watchdog Timer Interrupt If this bit is 1, a WDT exception occurred. Writing 1 to this bit clears it to 0.

Last IRQ Register

When an interrupt occurs, the 5th bit value of the interrupt vector is stored in the Last IRQ Register, shown in Table 43. This register allows the software to determine which interrupt source was last serviced. It is used by RTOS which have a single interrupt entry point. To implement this the software must set all interrupt vectors to the entry point address. The entry point service routine then reads this register to determine which source caused the interrupt or exception and respond accordingly.

The compare time is calculated by the following equation (Start Value = 1):

$$\text{Compare Mode Time (s)} = \frac{\text{Compare Value} - \text{Start Value} + 1 \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Gated Mode

In Gated Mode, the timer counts only when the timer input signal is in its active state as determined by the TPOL bit in the Timer Control 1 Register. When the timer input signal is active, counting begins. A timer interrupt is generated when the timer input signal transits from active to inactive state or a timer reload occurs. To determine if a timer input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. On reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is Reset to 0001h and counting continues as long as the timer input signal is active. If the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for Gated Mode and initiate the count:

1. Write to the timer control registers to:
   - Disable the timer
   - Configure the timer for Gated Mode
   - Set the prescale value
   - Select the active state of the timer input through the TPOL bit
2. Write to the Timer High and Low Byte registers to set the initial count value. This affects only the first pass in Gated Mode. After the first timer Reset in Gated Mode, counting always begins at the reset value of 0001h.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the timer interrupt to be generated only at the input deassertion event, the reload event or both by setting TICONFIG field of the Timer Control 0 Register.
6. Configure the associated GPIO port pin for the timer input alternate function.
7. Write to the Timer Control 1 Register to enable the timer.
8. The timer counts when the timer input is equal to the TPOL bit.

PWM Fault Control Register

The PWM Fault Control (PWMFCTL) Register, shown in Table 76, determines how the PWM recovers from a fault condition. Settings in this register select either an automatic or a software-controlled PWM restart.

Table 76. PWM Fault Control Register (PWMFCTL)

Bits	7	6	5	4	3	2	1	0
Field	Reserved	DBGRST	CMP1INT	CMP1RST	CMPINT	CMPRST	Fault0INT	Fault0RST
RESET	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E388h							

Bit	Description
[7]	Reserved This bit is reserved and must be programmed to 0.
[6] DBGRST	Debug Restart 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered and a new PWM period begins. 1 = Software controlled recovery. PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.
[5] CMP1INT	Comparator 1 Interrupt 0 = Interrupt on comparator assertion disabled. 1 = Interrupt on comparator assertion enabled.
[4] CMP1RST	Comparator 1 Restart 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. Software Controlled Recovery 1 = PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.
[3 CMP0INT	Comparator 0 Interrupt 0 = Interrupt on comparator 0 assertion disabled. 1 = Interrupt on comparator 0 assertion enabled.
[2] CMP0RST	Comparator 0 Restart 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. Software Controlled Recovery 1 = PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.

Note: This register can only be written when PWMEN is cleared.

Bit	Description (Continued)
[2] BRGCTL	Baud Rate Generator Control This bit causes different LIN-UART behaviors, depending on whether the LIN-UART receiver is enabled (REN = 1 in the LIN-UART Control 0 Register). When the LIN-UART receiver is not enabled, this bit determines whether the baud rate generator issues interrupts. 0 = BRG is disabled. Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value. 1 = BRG is enabled and counting. The BRG generates a receive interrupt when it counts down to 0. Reads from the Baud Rate High and Low Byte registers return the current BRG count value. When the LIN-UART receiver is enabled, this bit allows reads from the baud rate registers to return the BRG count value instead of the Reload Value. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value. 1 = Reads from the Baud Rate High and Low Byte registers return the current BRG count value. Unlike the timers, there is no mechanism to latch the High byte when the Low byte is read.
[1] RDAIRQ	Receive Data Interrupt Enable 0 = Received data and receiver errors generates an interrupt request to the interrupt controller. 1 = Received data does not generate an interrupt request to the interrupt controller. Only receiver errors generate an interrupt request.
[0] IREN	Infrared Encoder/Decoder Enable 0 = Infrared encoder/decoder is disabled. LIN-UART operates normally. 1 = Infrared encoder/decoder is enabled. The LIN-UART transmits and receives data through the Infrared encoder/decoder.

Table 96. LIN-UART Baud Rates

20.0MHz System Clock				10.0MHz System Clock			
Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	1	1250.0	0.00	1250.0	N/A	N/A	N/A
625.0	2	625.0	0.00	625.0	1	625.0	0.00
250.0	5	250.0	0.00	250.0	3	208.33	–16.67
115.2	11	113.64	–1.19	115.2	5	125.0	8.51
57.6	22	56.82	–1.36	57.6	11	56.8	–1.36
38.4	33	37.88	–1.36	38.4	16	39.1	1.73
19.2	65	19.23	0.16	19.2	33	18.9	0.16
9.60	130	9.62	0.16	9.60	65	9.62	0.16
4.80	260	4.81	0.16	4.80	130	4.81	0.16
2.40	521	2.399	–0.03	2.40	260	2.40	–0.03
1.20	1042	1.199	–0.03	1.20	521	1.20	–0.03
0.60	2083	0.60	0.02	0.60	1042	0.60	–0.03
0.30	4167	0.299	–0.01	0.30	2083	0.30	0.2

Bit	Description (Continued)
[2:1] SLA[9:8]	Slave Address Bits 9 and 8 Initialize with the appropriate Slave address value when using 10-bit Slave addressing. These bits are ignored when using 7-bit Slave addressing.
[0] DIAG	Diagnostic Mode Selects read back value of the Baud Rate Reload and State registers. 0 = Reading the Baud Rate registers returns the Baud Rate register values. Reading the State Register returns I2C Controller state information. 1 = Reading the Baud Rate registers returns the current value of the baud rate counter. Reading the State Register returns additional state information.

I2C Slave Address Register

The I2C Slave Address Register, shown in Table 122, provides control over the lower order address bits used in 7-bit and 10-bit Slave address recognition.

Table 122. I2C Slave Address Register (I2CSLVAD)

Bits	7	6	5	4	3	2	1	0
Field	SLA[7:0]							
RESET	00h							
R/W	R/W							
Addr	FF Æ247h							

Bit	Description
[7:0] SLA[7:0]	Slave Address Bits 7–0 Initialize with the appropriate Slave address value. When using 7 bit Slave addressing, SLA[9:7] are ignored.

bit 7. For the auto-baud character 0Dh, the auto-baud detector measures the period from the rising edge at the end of the start bit to the rising edge at the beginning of the stop bit. This measured value is automatically written to the BRG reload register after the auto-baud character is received. Once configured, the BRG will generate a bit clock based on this measured character time.

Line Control

When operating at high speeds, it is appropriate to speed up the rise and fall times of the single wire bus. Three control bits are used to control the bus rise and fall times, the high drive strength enable bit, the drive high enable bit and the output enable control bit.

The high drive strength enable bit puts the pin into High Driv eMode. For information about high drive strength, see the Electrical Characteristics chapter on page 337.

If the output enable control bit is set, the line is driven High and Low during transmission. If the drive high control bit is set, it drives the line high for short periods when transmitting a logic one. This rapidly charges the inherent capacitance of the single wire bus.

If both the output enable and drive high control bits are set, the line is driven high for one clock cycle when transmitting a one. If the output enable bit is clear and the drive high bit is set, the line is driven high until the input is detected High or the center of the bit time occurs, whichever is first.

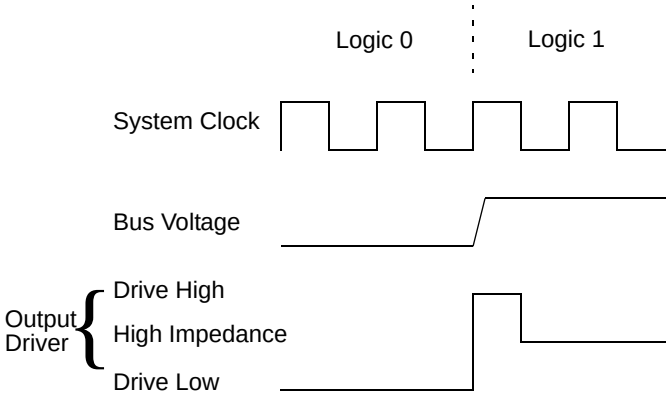

Figure 66. Output Driver when Drive High and Open Drain Enabled

9-Bit Mode

The serial interface is configured to transmit and receive a ninth data bit. This ninth bit is used to transmit or receive a software generated parity bit. It is used as an address/data bit in a multi-node system such as RS-485.