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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2811fi20ag

Document Objectives

This product specification provides detailed operating information about the Z16F2810, Z16F2811, Z16F3211, and Z16F6411 devices within Zilog's ZNEO Family of products. In this document, these four devices are collectively referred as the ZNEO or the ZNEO Z16F Series, unless specifically stated otherwise.

About This Manual

Zilog recommends that you read and understand the content contained in this product specification before setting up and using your ZNEO Z16F Series products. However, because we recognize that there are different styles of learning, this specification is designed to be used either as a procedural manual or a reference guide to important data.

Intended Audience

This document is written for Zilog customers who are experienced at working with micro-controllers, integrated circuits, or printed circuit assemblies.

Manual Conventions

The following assumptions and conventions are adopted to provide clarity and ease of use.

Courier New Typeface

Commands, code lines and fragments, hexadecimal addresses, and various executable items are distinguished from general text by the use of the Courier New typeface. Where the use of the font is not indicated, as in the Index, the name of the entity is presented in upper case.

Example. FLAGS[1] is SMRF.

Hexadecimal Values

Hexadecimal values are designated by lowercase h suffix and appear in the `Courier New` typeface.

Example. R1 is set to `F8h`.

Table 5. ZNEO CPU Control Registers

Address (Hex)	Register Description	Register Mnemonic
FF_E004-FF_E007	Program counter overflow	PCOV
FF_E00C-FF_E00F	Stack pointer overflow	SPOV
FF_E010	Flags	FLAGS
FF_E012	CPU control	CPUCTL

External Memory

Many ZNEO CPU products support external data and address buses for connecting to additional external memories and/or memory-mapped peripherals. The external addresses are used for storing program code, data, constants and stack, etc. Attempts to read from or write to unavailable external addresses is undefined.

Endianness

The ZNEO CPU accesses data in big endian order, that is, the address ofa multi-byte word or quad points to the most significant byte. Figure 7 displays the Endianness of the ZNEO CPU.

version already in progress, the Start bit is read to indicate ADC operation status (busy or available).

ADC Timing

Each ADC measurement consists of three phases:

1. Input sampling (programmable, minimum of 1.0 µs).
2. Sample-and-hold amplifier settling (programmable, minimum of 0.5 µs).
3. Conversion is 12 ADCLK cycles.

Figure 53 displays the timing of an ADC conversion.

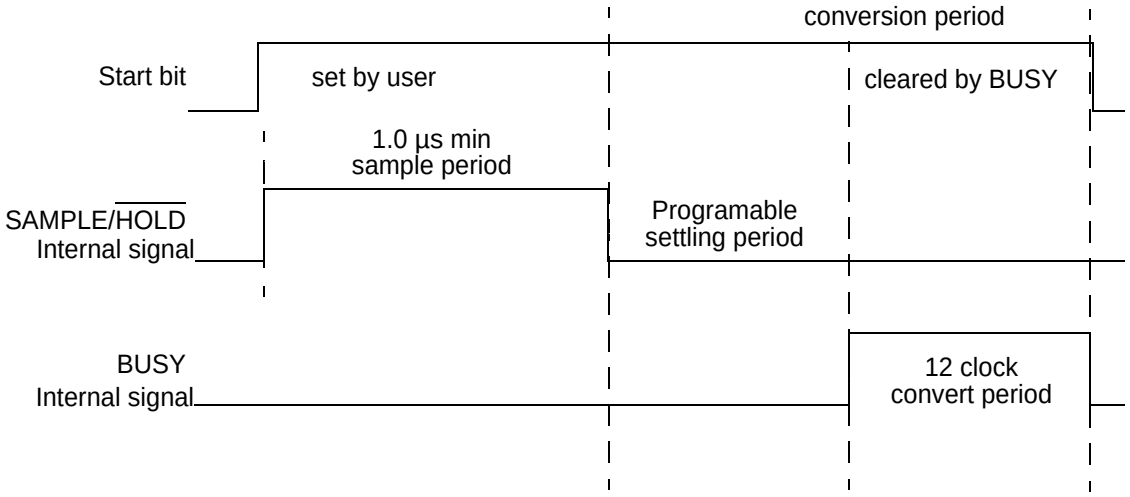

Figure 53. ADC Timing Diagram

Figure 54 displays the timing of convert period showing the 10 bit progression of the output.

ADC Timer 0 Capture Register

The ADC Timer 0 Capture Register contains the sixteen bits of the ADC Timer 0 count. The access to the ADC Timer 0 Capture Register is read-only. It reads 8 bits at a time or as a 16-bit word.

Table 133. ADC Timer 0 Capture Register, High Byte (ADCTCAP_H)

Bits	7	6	5	4	3	2	1	0
Field	ADCTCAPH							
RESET	X							
R/W	R							
Addr	FF–E512h							

Bit	Description
[7:0] ADCTCAPH	**ADC Timer 0 Count High Byte** 00h–FFh = The Timer 0 count is held in the data registers until the next ADC conversion is started.

Table 134. ADC Timer 0 Capture Register, Low Byte (ADCTCAP_L)

Bits	7	6	5	4	3	2	1	0
Field	ADCTCAPL							
RESET	X							
R/W	R							
Addr	FF–E513h							

Bit	Description
[7:0] ADCTCAPL	**ADC Timer 0 Count Low Byte** 00h–FFh = The Timer 0 count is held in the data registers until the next ADC conversion is started.

Comparator and Operational Amplifier Overview

ZNeo devices feature a general-purpose comparator and an operational amplifier. The comparator is a moderate speed (200 ns propagation delay) device which is designed for a maximum input offset of 5 mV. The comparator is used to compare two analog input signals. General-purpose input pins (CINP and CINN) provides the comparator inputs. The output is available as an interrupt source.

Option bits allow user configuration of certain aspects of the ZNEO® Z16F Series operation. The feature configuration data is stored in the Program memory and read during Reset. The features available for control using the option bits are:

- WDT time-out response selection–interrupt or Reset
- WDT enabled at Reset
- The ability to prevent unwanted read access to user code in Program memory
- The ability to prevent accidental programming and erasure of the user code in Program memory
- Voltage Brown-Out (VBO) configuration—always enabled or disabled during Stop Mode to reduce Stop Mode power consumption
- Oscillator mode selection for high, medium and low power crystal oscillators, or external RC oscillator
- PWM pin setup for motor control application

Operation

Each time the option bits are programmed or erased, the device must be Reset for the change to take place. During any reset operation (System Reset, Short Reset, or Stop Mode Recovery), the option bits are automatically read from the Program memory and written to Option Configuration registers. The Option Configuration registers control operation of the device. Option Bit Control Register are loaded before the device exits Reset and the ZNEO CPU begins code execution. The Option Configuration registers are not part of the Register file and are not accessible for read or write access.

Option Bit Address Space

The first four bytes of Program Memory at addresses 0000h through 0003h, shown in Tables 161 and 162, respectively, are reserved for the user option bits. These bytes are used to configure user specific options. You can change the option bits to meet application requirements.

Program Memory Address 0000h

Option bits in this space are altered to change the chip configuration at reset.

DBG <<- regdata[23:16]
DBG <<- regdata[15:8]
DBG <<- regdata[7:0]
DBG --> CRC[0:7]

Read PC. 7 K H 5 H D G 3 U R J U D P &R X Q W H U F R P P D Q G U H W X U Q V W K

DBG <-- 0000_0110
DBG --> 00h
DBG --> PC[23:16]
DBG --> PC[15:8]
DBG --> PC[7:0]
DBG --> CRC[0:7]

Write PC. 7 K H : U L W H 3 U R J U D P &R X Q W H U F R P P D Q G Z U L W H V W K H

DBG <-- 0000_0111
DBG <-- 00h
DBG <-- PC[23:16]
DBG <-- PC[15:8]
DBG <-- PC[7:0]
DBG --> CRC[0:7]

Read Flags. 7 K H 5 H D G) O D J V F R P P D Q G U H W X U Q V W K H F R Q W H

DBG <-- 0000_1000
DBG --> 00h
DBG --> flags[7:0]
DBG --> CRC[0:7]

Write Instruction. 7 K H : U L W H , Q V W U X F W L R Q F R P P D Q G Z U L W H V R Q

DBG <-- 0000_1001
DBG <-- opcode[15:8]
DBG <-- opcode[7:0]
DBG --> CRC[0:7]

Read Register. 7 K H 5 H D G 5 H J L V W H U F R P P D Q G U H W X U Q V W K H F R

DBG <-- {0100,regno[3:0]}
DBG --> regdata[31:24]
DBG --> regdata[23:16]
DBG --> regdata[15:8]
DBG --> regdata[7:0]
DBG --> CRC[0:7]

Write Register. 7 K H : U L W H 5 H J L V W H U F R P P D Q G Z U L W H V G D W D

DBG <-- {0101,regno[3:0]}
DBG <-- regdata[31:24]
DBG <-- regdata[23:16]
DBG <-- regdata[15:8]
DBG <-- regdata[7:0]
DBG --> CRC[0:7]

currently in progress, transmits a Serial Break condition for 4096 system clocks and sets the ABSRCH bit in the DBGCTL Register. This break is sent to ensure the host also detects the error.

A clock change invalidates the baud reload value. Communication cannot continue until a new autobaud reload value is set. As a result, the device automatically sends a serial break to reset the communication link whenever a clock change occurs.

DEBUG Halt Mode

During debugging, it is appropriate to stop the CPU from executing instructions by placing the device in DEBUG Halt Mode. The operating characteristics of the ZNEO Z16F Series devices in DEBUG Halt Mode are:

- The ZNEO CPU fetch unit stops, idling the ZNEO CPU
- All enabled on-chip peripherals operate unless in Stop Mode
- Constantly refreshes the WDT, if enabled

Entering DEBUG Halt Mode

The device enters DEBUG Halt Mode by any of the following operations:

- Write the DBGHALT bit in the DBGCTL Register to 1 using the OCD interface
- ZNEO CPU execution of BRK instruction (when enabled)
- Hardware breakpoint match.

Exiting DEBUG Halt Mode

The device exits DEBUG Halt Mode by any of the following operations:

- Clearing the DBGHALT bit in the DBGCTL Register to 0
- Power-On Reset
- Voltage Brown-Out reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a Reset

Reading and Writing Memory

Most debugging functions are accomplished by reading and writing control registers. The OCD hardware has the capability of reading and writing memory when the CPU is running.

When a read or write request from the OCD hardware occurs, the OCD steals the bus for the number of cycles required to complete the read or write operation. This bus stealing

Bit	Description (Continued)
[6] TDH	**Transmit Drive High** This control bit causes the interface to drive the line high when a logic 1 is being transmitted. If OE is zero, the line stops being driven when the input is high or at the center of the bit, whichever is first. If OE is one, the line is driven high for one clock cycle. This bit is ignored if Debug Mode is zero and the UART is disabled. 0 = Transmit Drive High disabled. 1 = Transmit Drive High enabled.
[5] HDS	**High Drive Strength** This control bit enabled high drive strength for the output driver. 0 = Low Drive Strength 1 = High Drive Strength
[4] TXFC	**Transmitter Start Bit Flow Control** This control bit enables start bit flow control on the transmitter. The transmitter waits until a remote device sends a start bit before transmitting its data. 0 = Transmitter start bit flow control disabled. 1 = Transmitter start bit flow control enabled.
[3] NBEN	**9-Bit Mode Enable** This control bit enables transmission and reception of a ninth data bit. 0 = Nine bit mode disabled. 1 = Nine bit mode enabled.
[2] NB	**Value Of Ninth Bit** This bit is the value of the ninth data bit. When written, this reflects the ninth data bit that will be transmitted if nine bit mode is enabled. When read, this bit reflects the value of the ninth bit of the last nine bit character received. 0 = Ninth bit is zero. 1 = Ninth bit is one.
[1] OUT	**Output State** This control bit sets the state of the output transceiver. If the UART is enabled, this bit must be set to 1 to idle high. Clearing this bit to 0 when the UART is enabled will transmit a break condition. If the UART is disabled, this logic value will be driven onto the pin if OE is set. This bit is ignored in Debug Mode. 0 = Transmit Break if UART enabled. Drive Low if UART disabled and output enabled. 1 = Idle High if UART enabled. Drive high if UART disabled and output enabled.
[0] PIN	**Debug Pin** This bit reflects the state of the DBG pin. 0 = DBG pin is Low. 1 = DBG pin is High.

Oscillator Operation with an External RC Network

Figure 71 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.

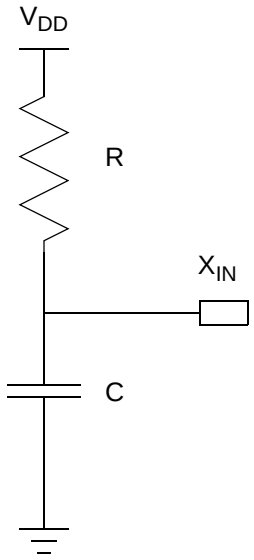

Figure 71. Connecting the On-Chip Oscillator to an External RC Network

An external resistance value of 15 kΩ is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 10 kΩ. The typical oscillator frequency is estimated from the values of the resistor (*R* in kΩ) and capacitor (*C* in pF) elements using the following equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1\times10^{6}}{(1.5 \times R \times C)}$$

Figure 3 displays the typical (3.3 V and 25°C) oscillator frequency as a function of the capacitor (*C* in pF) employed in the RC network assuming a 15kΩ external resistor. For very small values of C, the parasitic capacitance of the oscillator X_{IN} pin and the printed circuit board must be included in the estimation of the oscillator frequency.

Oscillator Divide Register

The Oscillator Divide Register (OSCDIV), shown in Table 184, provides the value to divide the system clock by. The Oscillator Divide Register must be unlocked before writing. Writing the two-step sequence E7h followed by 18h to the Oscillator Control Register address unlocks it. The register locks after completion of a register write to the OSCDIV.

Table 184. Oscillator Divide Register (OSCDIV)

Bits	7	6	5	4	3	2	1	0
Field	DIV							
RESET	00h*							
R/W	R/W							
Addr	FF_E0A1h							

Note: *The reset value is 08h if the option bit LPOPT is 0.

Bit	Value (H)	Description
[7:0] DIV	00h–FFh	**Oscillator Divide** 00h–divider is disabled; all other entries are the divide value for scaling the system clock.

Figure 73 displays the typical current consumption while operating at 3.3 V at 30 ºC versus the system clock frequency.

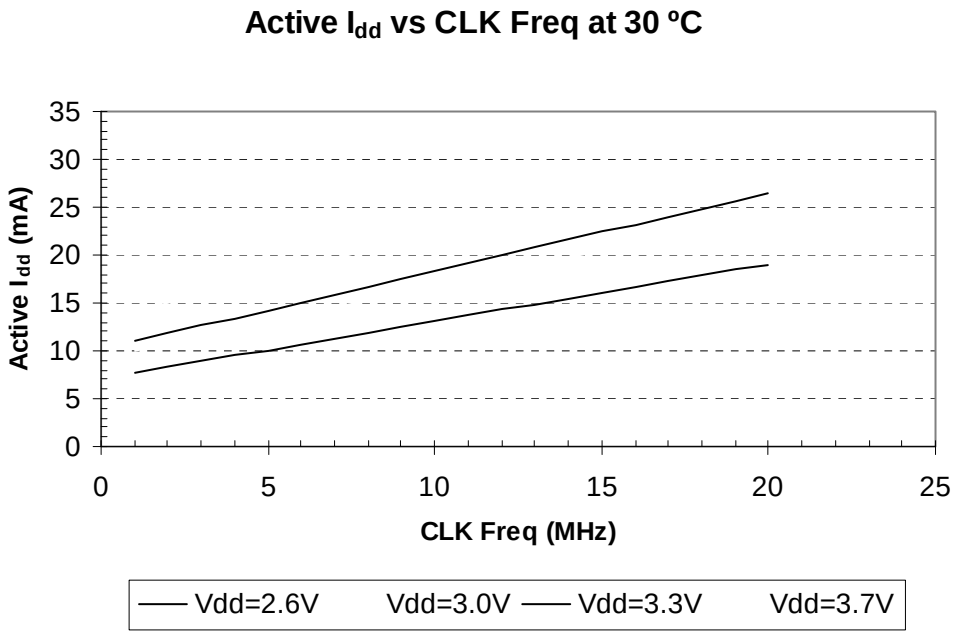

Figure 73. Typical I_{DD} Versus System Clock Frequency