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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f2811fi20sg

List of Tables

10-Bit Analog-to-Digital Converter with Programmable Gain Amplifier

The ADC converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from 12 different analog input sources.

Analog Comparator

It features an on-chip analog comparator with external input pins.

Operational Amplifier

It features a two-input, one-output operational amplifier.

General-Purpose Input/Output

The Motor Control MCUs features 76 GPIO pins. Each pin is individually programmable.

Universal Asynchronous Receiver/Transmitter

It contains two fully-featured UARTs with LIN protocol support. The UART communication is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8-bit and 9-bit data modes, selectable parity and an efficient bus transceiver driver enable signal for controlling a multi-transceiver bus, such as RS-485.

Infrared Encoder/Decoders

The ZNEO Z16F Series products contain two fully-functional, high-performance UART to Infrared Encoder/Decoders (Endecs). Each infrared endec is integrated with an on-chip UART to allow easy communication between the ZNEO Z16F Series device and IrDA physical layer specification Version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost and point-to-point communication between PCs, PDAs, cell phones, printers and other infrared enabled devices.

Inter-Integrated Circuit Master/Slave Controller

The I^2C controller makes Z16F2811 compatible with the I^2C protocol. It consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line. The I^2C operates as a Master and/or Slave and supports multi-master bus arbitration.

Enhanced Serial Peripheral Interface

The ESPI allows the data exchange between ZNEO Z16F Series and other peripheral devices such as electrically erasable programmable read-only memory (EEPROMs),

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E399	PWM 2 High Side Duty Cycle Low Byte	PWMH2DL	00	125
FF_E39A	PWM 2 Low Side Duty Cycle High Byte	PWML2DH	00	124
FF_E39B	PWM 2 Low Side Duty Cycle Low Byte	PWML2DL	00	125
FF_E39C-FF_E3BF	Reserved for PWM	—	—	—
DMA Block Base Address = FF_E400				
DMA Request Selection Control				
FF_E400	DMA0 Request Select	DMA0REQSEL	00	282
FF_E401	DMA1 Request Select	DMA1REQSEL	00	282
FF_E402	DMA2 Request Select	DMA2REQSEL	00	282
FF_E403	DMA3 Request Select	DMA3REQSEL	00	282
FF_E404-F	Reserved	—	—	—
DMA Channel 0 Base Address = FF_E410				
FF_E410	DMA0 Control 0	DMA0CTL0	00	285
FF_E411	DMA0 Control 1	DMA0CTL1	00	285
FF_E412	DMA0 Transfer Length High	DMA0TXLNH	00	286
FF_E413	DMA0 Transfer Length Low	DMA0TXLNL	00	287
FF_E414	Reserved	—	—	—
FF_E415	DMA0 Destination Address Upper	DMA0DARU	00	287
FF_E416	DMA0 Destination Address High	DMA0DARH	00	287
FF_E417	DMA0 Destination Address Low	DMA0DARL	00	287
FF_E418	Reserved	—	—	—
FF_E419	DMA0 Source Address Upper	DMA0SARU	00	288
FF_E41A	DMA0 Source Address High	DMA0SARH	00	288
FF_E41B	DMA0 Source Address Low	DMA0SARL	00	288
FF_E41C	Reserved	—	—	—
FF_E41D	DMA0 List Address Upper	DMA0LARU	00	289
FF_E41E	DMA0 List Address High	DMA0LARH	00	289
FF_E41F	DMA0 List Address Low	DMA0LARL	00	289

XX = Undefined.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E43A	DMA2 Source Address High	DMA2SARH	00	288
FF_E43B	DMA2 Source Address Low	DMA2SARL	00	288
FF_E43C	Reserved			
FF_E43D	DMA2 List Address Upper	DMA2LARU	00	289
FF_E43E	DMA2 List Address High	DMA2LARH	00	289
FF_E43F	DMA2 List Address Low	DMA2LARL	00	289
DMA Channel 3 Base Address = FF_E440				
FF_E440	DMA3 Control 0	DMA3CTL0	00	285
FF_E441	DMA3 Control 1	DMA3CTL1	00	285
FF_E442	DMA3 Transfer Length High	DMA3TXLNH	00	286
FF_E443	DMA3 Transfer Length Low	DMA3TXLNL	00	287
FF_E444	Reserved	—	—	—
FF_E445	DMA3 Destination Address Upper	DMA3DARU	00	287
FF_E446	DMA3 Destination Address High	DMA3DARH	00	287
FF_E447	DMA3 Destination Address Low	DMA3DARL	00	287
FF_E448	Reserved	—	—	—
FF_E449	DMA3 Source Address Upper	DMA3SARU	00	288
FF_E44A	DMA3 Source Address High	DMA3SARH	00	288
FF_E44B	DMA3 Source Address Low	DMA3SARL	00	288
FF_E44C	Reserved	—	—	—
FF_E44D	DMA3 List Address Upper	DMA3LARU	00	289
FF_E44E	DMA3 List Address High	DMA3LARH	00	289
FF_E44F	DMA3 List Address Low	DMA3LARL	00	289
Analog Block Base Address = FF_E500				
ADC Base Address = FF_E500				
FF_E500	ADC0 Control Register	ADC0CTL	00	246
FF_E501	Reserved	—	—	—
FF_E502	ADC0 Data High Byte Register	ADC0D_H	XX	247
FF_E503	ADC0 Data Low Bits Register	ADC0D_L	XX	248

XX = Undefined.

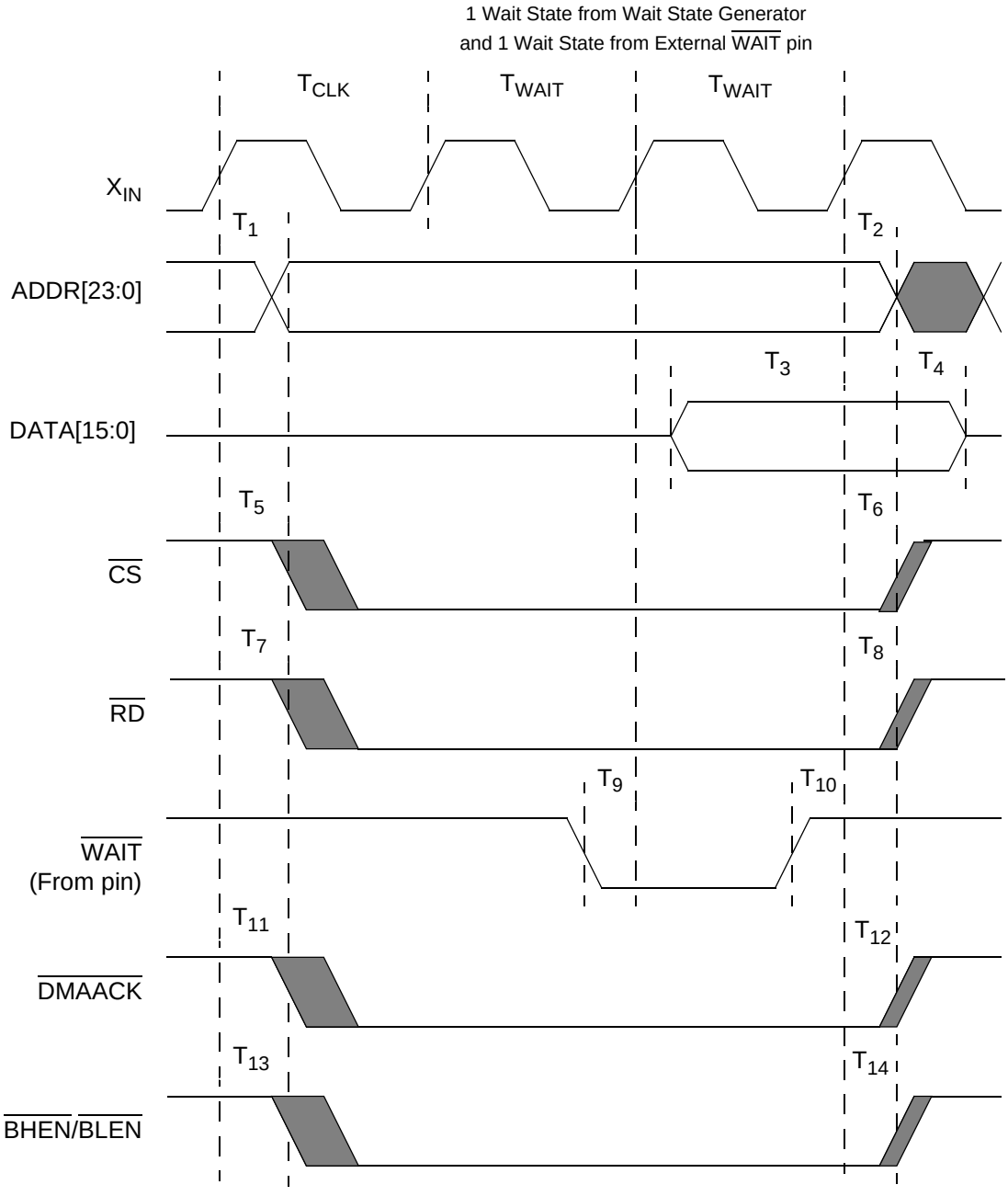

Figure 13. External Interface Timing for a Read Operation, Normal Mode

Table 45. Interrupt Request1 Register (IRQ1) and Interrupt Request1 Set Register (IRQ1SET)

Bits	7	6	5	4	3	2	1	0
Field	PAD7I	PAD6I	PAD5I	PAD4I	PAD3I	PAD2I	PAD1I	PAD0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Addr	FF_E034h							
Field	PAD7I	PAD6I	PAD5I	PAD4I	PAD3I	PAD2I	PAD1I	PAD0I
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Addr	FF_E035h							

Note: IRQ1SET at address FF_E035h is write only and used to set the interrupts identified.

Bit	Description
[7:0] PADxI	**Port A/D Pin *x* Interrupt Request** 0 = No interrupt request is pending for GPIO Port A/D pin *x*. 1 = An interrupt request from GPIO Port A/D pin *x* is awaiting service. Writing 1 to these bits resets it to 0. Here, *x* indicates the specific GPIO port pin number (0 through 7). PAD7I and PAD0I have interrupt sources other than Port A and Port D as selected by the Port A IRQ MUX registers. PAD7I is configured to provide the comparator interrupt. PAD0I is configured to provide the OCD interrupt.

Note: The above IRQ1 bits are set any time the selected port is toggled. The setting of these bits are not affected by the associated interrupt enable bits.

Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 46, stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the ZNEO CPU. If interrupts are globally disabled (polled interrupts), the ZNEO CPU reads the Interrupt Request 1 Register to determine, if any interrupt requests are pending. Writing 1 to the bits in this register clears the interrupt. The bits of this register are set bywriting 1 to the Interrupt Request 2 Set Register (IRQ2SET) at address FF_E039h.

PWM Output Polarity and Off-State

The default off-state and polarity of the PWM outputs are controlled by the option bits PWMHI and PWMLO. The PWMHI option controls the off-state and polarity for PWM high-side outputs PWMH0, PWMH1 and PWMH2. The PWMLO option controls the off-state and polarity for low-side outputs PWML0, PWML1 and PWML2.

The off-state is the value programmed in the option bit. For example, programming PWMHI to 1 makes the off-state of PWMH0, PWMH1 and PWMH2 a High logic value and the active state a Low logic value. Conversely, programming PWMHI to 0 causes the off-state to be a Low logic value. PWMLO is programmed in a similar manner.

PWM Enable

The MCEN option bit enables output pairs PWM0, PWM1 and PWM2. If the Motor Control option is not enabled, the PWM outputs remain in a high-impedance state after reset and is used as alternate functions like general purpose input. If the Motor Control option is enabled, following a Power-On Reset (POR) the PWM pins enter a high impedance state. As the internal reset proceeds, the PWM outputs are forced to the off-state as determined by the PWMHI and PWMLO off-state option bits.

PWM Reload Event

To prevent erroneous PWM pulse-widths and periods, registers that control the timing of the output are buffered. Buffering causes all of the PWM compare values to update. In other words, the registers controlling the duty cycle and clock source prescaler only take effect on a PWM reload event. A PWM reload event is configured to occur at the end of each PWM period or only every 2, 4, or 8 PWM periods by setting the RELFREQ bits in the PWM Control 1 Register (PWMCTL1). Software indicates that all new values are ready by setting the READY bit in the PWM Control 0 Register (PWMCTL0) to 1. When the READY bit is set to 1, the buffered values take effect at the next reload event.

PWM Prescaler

The prescaler decreases the PWM clock signal by factors of 1, 2, 4, or 8 with respect to the system clock. The PRES[1:0] bit field in the PWM Control 1 Register (PWMCTL1) controls prescaler operation. This 2-bit PRES field is buffered so that the prescale value only changes on a PWM Reload event.

PWM Period and Count Resolution

The PWM counter operates in two modes to allow edge-aligned and center-aligned outputs. Figures 22 and 23 illustrate edge and center-aligned PWM outputs. The mode in which the PWM operates determine the period of the PWM outputs (PERIOD). The programmed duty-cycle (PWMDC) and the programmed deadband time (PWMDB) deter-

$$\text{roundup}(\text{PWMMPF}) = T_{\text{minPulseOut}} / (T_{\text{systemClock}} \cdot \text{PWMprescaler})$$

where *minPulseOut* is the shortest allowed pulse width on the PWM outputs (in seconds).

Synchronization of PWM and ADC

The ADC on the ZNeo is synchronized with the PWM period. Enabling the PWM ADC trigger causes the PWM to generate an ADC conversion signal at the end of each PWM period. Additionally, in CENTER-ALIGNED Mode, the PWM generates a trigger at the center of the period. Setting the ADCTRIG bit in the PWM Control 0 Register (PWMCTL0) enables the ADC synchronization.

Synchronized Current-Sense Sample and Hold

The PWM controls the current-sense input sample and hold amplifier. The signal controlling the sample/hold is configured to always sample or automatically hold when any or all of the PWM High or Low outputs are in the on state. The current-sense sample and hold is controlled by the Current-Sense Sample and Hold Control Register (CSSHR0 and CSSHR1).

PWM Timer and Fault Interrupts

The PWM generates interrupts to the ZNEO CPU during any of the following events:

- PWM Reload, in which the interrupt is generated at the end of a PWM period when a PWM register reload occurs
- PWM Fault, in which a fault condition is indicated by asserting any FAULT pins or by the assertion of the comparator

Fault Detection and Protection

The ZNEO contains hardware and software fault controls, which allow rapid deassertion of all enabled PWM output signals. A logic Low on an external fault pin ($\overline{\text{FAULT0}}$ or FAULT1) or the assertion of the over current comparator forces the PWM outputs to the predefined off-state.

Similar deassertion of the PWM outputs is accomplished in software by writing to the PWMOFF bit in the PWM Control 0 Register. The PWM counter continues to operate while the outputs are deasserted (inactive) due to one of these fault conditions.

The fault inputs are individually enabled through the PWM Fault Control Register. If a fault condition is detected and the source is enabled, the fault interrupt is generated. The

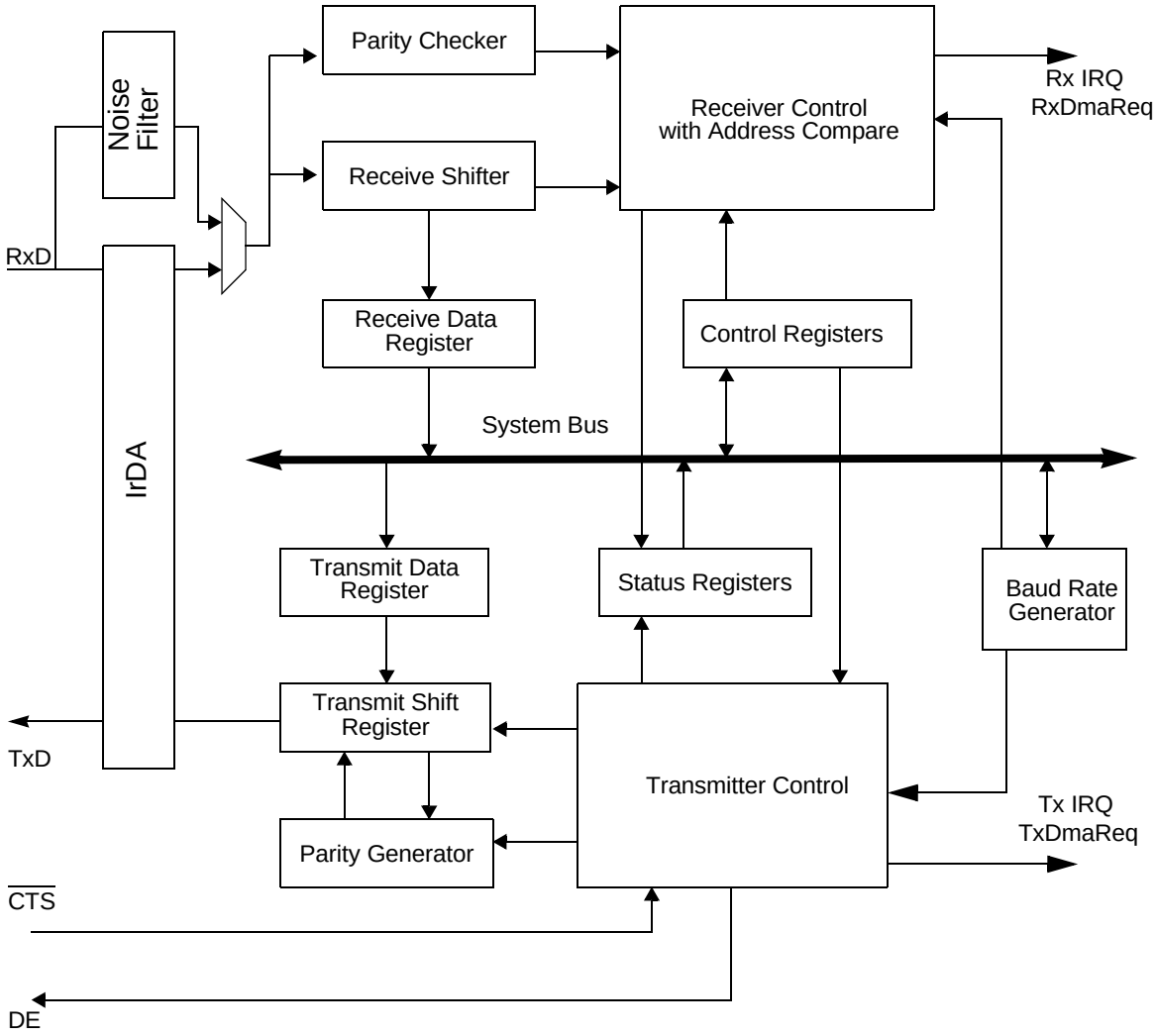

Figure 24. LIN-UART Block Diagram

Operation

Data Format for Standard UART Modes

The LIN-UART always transmits and receives data in an 8-bit data format, with the first bit being the least-significant bit. An even- or odd-parity bit or multiprocessor address/ data bit is optionally added to the data stream. Each character begins with an active Low start bit and ends with either 1 or 2 active High stop bits. Figures 25 and 26 display the

LIN-UART Control 0 Register

The LIN-UART Control 0 Register, shown in Table 89, configures the basic properties of the LIN-UART's transmit and receive operations.

Table 89. LIN-UART Control 0 Register (UxCTL0)

Bits	7	6	5	4	3	2	1	0
Field	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF–E202h, FF–E212h							

Bit	Description
[7] TEN	**Transmit Enable** This bit enables or disables the transmitter. The enable is also controlled by the $\overline{CTS}$ signal and the CTSE bit. If the $\overline{CTS}$ signal is Low and the CTSE bit is 1, the transmitter is enabled. 0 = Transmitter disabled. 1 = Transmitter enabled.
[6] REN	**Receive Enable** This bit enables or disables the receiver. 0 = Receiver disabled. 1 = Receiver enabled.
[5] CTSE	**CTS Enable** 0 = The $\overline{CTS}$ signal has no effect on the transmitter. 1 = The LIN-UART recognizes the $\overline{CTS}$ signal as an enable control for the transmitter.
[4] PEN	**Parity Enable** This bit enables or disables parity. Even or odd is determined by the PSEL bit. 0 = Parity is disabled. This bit is overridden by the MPEN bit. 1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit.
[3] PSEL	**Parity Select** 0 = Even parity is transmitted and expected on all received data. 1 = Odd parity is transmitted and expected on all received data.

Bit	Description (Continued)
[2] WOR	**Wire-OR (Open-Drain) Mode Enabled** 0 = ESPI signal pins not configured for open-drain. 1 = All four ESPI signal pins (SCK, $\overline{SS}$, MISO, MOSI) configured for open-drain function. This setting is used for Multi-Master and/or Multi-Slave configurations.
[1] MMEN	**ESPI Master Mode Enable** This bit controls the data I/O pin selection and SCK direction. 0 = Data-out on MISO, data-in on MOSI (used in SPI Slave Mode), SCK is an input. 1 = Data-out on MOSI, data-in on MISO (used in SPI Master Mode), SCK is an output.

Caution: If reading the counter one byte at a time while the BRG is counting keep in mind that the values will not be in sync. It is recommended to read the counter using word (2-byte) reads.

I²C Master/Slave Controller Registers

Table 111 summarizes the I²C Master/Slave Controller software-accessible registers.

Table 111. I²C Master/Slave Controller Registers

Name	Abbreviation	Description
I²C Data	I2CDATA	Transmit/Receive Data Register.
I²C Interrupt Status	I2CISTAT	Interrupt Status Register.
I²C Control	I2CCTL	Control Register–basic control functions.
I²C Baud Rate High	I2CBRH	High byte of baud rate generator initialization value.
I²C Baud Rate Low	I2CBRL	Low byte of baud rate generator initialization value.
I²C State	I2CSTATE	State Register.
I²C Mode	I2CMODE	Selects MASTER or SLAVE modes, 7-bit or 10-Bit Address. Configure address recognition, Defines Slave Address bits [9:8].
I²C Slave Address	I2CSLVAD	Defines Slave Address bits [7:0]

Comparison with Master Mode only I²C Controller

Porting code written for the Master-only I²C Controller found on other Z8 Encore!® parts to the I²C Master/Slave Controller is straightforward. The I2CDATA, I2CCTL, I2CBRH and I2CBRL Register definitions are not changed.

The differences between the Master-only I²C Controller and I²C Master/Slave Controller designs are:

- The Status Register (I2CSTATE) from the Master-only I²C Controller is split into the Interrupt Status (I2CISTAT) Register and the State (I2CSTATE) Register because there are more interrupt sources. The ACK, 10b, TAS (now called AS) and DSS (now called DS) bits formerly in the status register are moved to the state register.
- The I2CSTATE Register is called as I2CDST (Diagnostic State) Register in the Master Only Mode version. The I2CDST Register provided diagnostic information. The I2CSTATE Register contains status and state information that are useful to software in operational mode.
- The I2CMODE Register is called as I2CDIAG (Diagnostic Control) Register in the Master Only Mode version. The I2CMODE Register provides control for Slave modes of operation as well as the most significant two bits of the 10-bit Slave address.
- The I2CSLVAD Register is added for programming the Slave address.
- The ACKV bit in the I2CSTATE Register enables the Master to verify the acknowledge from the Slave before sending the next byte.

14. The Slave I2C Controller asserts the Stop/Restart interrupt (set the SPRS bit in the I2CISTAT Register).
15. Software responds to the Stop interrupt by reading the I2CISTAT Register, clearing the SPRS bit.

DMA Control of I2C Transactions

The DMA engine is configured to support transmit and receive DMA requests from the I2C Controller. The I2C data interrupt requests must be disabled by setting the DMAIF bit in the I2C Mode Register and clearing the TXI bit in the I2C Control Register. This allows error condition interrupts to be handled by software while data movement is handled by the DMA engine.

The DMA interface on the I2C Controller is intended to support data transfer but not Master Mode address byte transfer. The Start, Stop and NAK bits must be controlled by software.

A summary of the sequence of I2C data transfer using the DMA follows.

Master Write Transaction with Data DMA

1. Configure the selected DMA Channel for I2C transmit. The IEOB bit must be set in the DMACTL Register for the last buffer to be transferred.
2. The I2C interrupt must be enabled in the interrupt controller to alert software of any I2C error conditions. A Not Acknowledge interrupt occurs on the last byte transferred.
3. The I2C Master/Slave must be configured as defined in the sections above describing Master Mode transactions. The TXI bit in the I2CCTL Register must be cleared.
4. Initiate the I2C transaction as described in the Master Address Only Transactions section on page 210, using the ACKV and ACK bits in the I2CSTATE Register to determine if the slave acknowledges.
5. Set the DMAIF bit in the I2CMODE Register.
6. The DMA transfers the data, which is to be transmitted to the slave.
7. When the DMA interrupt occurs, poll the I2CSTAT Register until the TDRE bit = 1 to ensure that the I2C Master/Slave hardware has commenced transmitting the most recent byte written by the DMA.
8. Set the Stop bit in the I2CCTL Register. The Stop bit is polled by software to determine when the transaction is actually completed.
9. Clear the DMAIF bit in the I2CMODE Register.

The following section describes the I2C Master/Slave Controller operating as a Slave in 10-Bit Addressing Mode, transmitting data to the bus master.

Note: If BRG = 0000h, use 10000h in the equation.

Table 115. I²C Baud Rate High Byte Register (I2CBRH)

Bits	7	6	5	4	3	2	1	0
Field	BRH							
RESET	FFh							
R/W	R/W							
Addr	FF–E243h							

Bit	Description
[7:0] BRH	**I²C Baud Rate High Byte** Most significant byte, BRG[15:8], of the I²C Baud Rate Generator's reload value.

Note: If the DIAG bit in the I²C Mode Register is set to 1, a read of the I2CBRH Register returns the current value of the I²C Baud Rate Counter[15:8].

Table 116. I²C Baud Rate Low Byte Register (I2CBRL)

Bits	7	6	5	4	3	2	1	0
Field	BRL							
RESET	FFh							
R/W	R/W							
Addr	FF–E244h							

Bit	Description
[7:0] BRL	**I²C Baud Rate Low Byte** Least significant byte, BRG[7:0], of the I²C Baud Rate Generator's reload value.

Note: If the DIAG bit in the I²C Mode Register is set to 1, aread of the I2CBRL Register returns the current value of the I²C Baud Rate Counter[7:0].

Reference Buffer, RBUF

The reference buffer, RBUF, supplies the reference voltage for the ADC. When enabled, the internal voltage reference generator supplies the ADC and the voltage is available on the VREF pin. When RBUF is disabled, the reference voltage must be supplied externally through the VREF pin. RBUF is controlled by the REFEN bit in the ADC0 Control Register.

Internal Voltage Reference Generator

The internal voltage reference generator provides the voltage to RBUF. The internal reference voltage is 2 V.

ADC Control Register Definitions

The following sections describe the control registers for the ADC.

ADC0 Control Register 0

The ADC0 Control Register initiates the A/D conversion and provides ADC0 status information.

Table 126. ADC0 Control Register 0 (ADC0CTL)

Bits	7	6	5	4	3	2	1	0
Field	START0	CVTRD0	REFEN	ADC0EN	ANAIN0[3:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF–E500h							

Bit	Description
[7] START0	**ADC0 Start/Busy** 0 = Writing to 0 has no effect. Reading a 0 indicates the ADC0 is available to begin a conversion. 1 = Writing to 1 starts a conversion on ADC0. Reading a 1 indicates a conversion is currently in progress.
[6] CVTRD0	**Convert On Read** 0 = The ADC0 operates normally. 1 = If this bit is set to 1, whenever the ADC0D Register is read it increments the ANAIN field by one and start a new conversion. The ANAIN field increments until it reaches the value set in the ADC0MAX Register. After doing the conversion on the channel specified by the ADC0MAX Register, the next read resets the ANAIN field to 0. This function is used with the DMA to perform continuous conversions.

Programming

When the Flash Controller is unlocked, word writes to Program memory from user code programs a word into the Flash if the address is located in the unlocked page. An erased Flash word contains all ones (FFFFh). The programming operation is used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires a Page Erase or Mass Erase operation.

The Flash must be programmed one word (16-bits) at a time. If a byte (8-bit) write to Flash memory occurs, the Flash controller waits until the other byte within the word is written before beginning the programming operation.

While the Flash Controller programs the Flash memory, Flash reads are held in wait. If the CPU is fetching instruction from Flash, the CPU idles until the programming operation is complete. Interrupts that occur when a programming operation is in progress are serviced after the programming operation is complete. To exit Programming Mode and lock the Flash Controller, write 00h to the Flash Command Register.

User code cannot program Flash Memory on a page that lies in a protected sector. When user code writes memory locations, only addresses located in the unlocked page are programmed. Memory writes outside of the unlocked page are ignored.

Caution: Each memory location must not be programmed more than twice before an erase occurs.

Observe the following steps to program the Flash from user code:

1. Write the page of memory to be programmed to the Flash Page Select Register.
2. Write the first unlock command 73h to the Flash Command Register.
3. Write the second unlock command 8Ch to the Flash Command Register.
4. Write a word to Program memory.
5. Repeat step 4 to program additional memory locations on the same page.
6. Write 00h to the Flash Command Register to lock the Flash Controller.

Page Erase

The Flash memory is erased one page (2 KB) at a time. Page Erasing the Flash memory sets all words in that page to the value FFFFh. The Flash Page Select Register identifies the page to be erased. While the Flash Controller executes the Page Erase operation, Flash reads are held in wait. Interrupts that occur when the Page Erase operation is in progress will be serviced after the Page Erase operation is complete. When the Page Erase opera-

On-Chip Peripheral AC and DC Electrical Characteristics

Table 187 lists the POR and VBO electrical characteristics and timing. Table 188 lists the Reset and Stop Mode Recovery pin timing.

Table 187. POR and VBO Electrical Characteristics and Timing

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
V_{POR}	Power-On Reset voltage threshold	2.20	2.45	2.70	V	$V_{DD} = V_{POR}$
V_{VBO}	Voltage Brown-Out reset voltage threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$
	V_{POR}–V_{VBO}		50	100	mV	
	Starting V_{DD} voltage to ensure valid POR	—	V_{SS}	—	V	
T_{ANA}	Power-On Reset analog delay	—	50	—	ms	$V_{DD} > V_{POR}$; T_{POR} Digital Reset delay follows T_{ANA}
T_{POR}	Power-On Reset digital delay	—	12	—	µs	66 IPO cycles
T_{VBO}	Voltage Brown-Out pulse rejection period	—	10	—	ms	$V_{DD} < V_{VBO}$ to generate a Reset
T_{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset	0.10	—	100	ms	
I_{CC}	Supply current		500		µA	V_{DD} = 3.3 V.

Note:
1. Data in the typical column is from characterization at 3.3 V and 0°C. These values are provided for design guidance only and are not tested in production.

Table 188. Reset and Stop Mode Recovery Pin Timing

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
T_{RESET}	$\overline{\text{RESET}}$ pin assertion to initiate a System Reset	4	—	—	T_{CLK}	Not in Stop Mode. T_{CLK} = System Clock period.
T_{SMR}	Stop Mode Recovery pin Pulse Rejection Period	10	20	40	ns	RESET, DBG and GPIO pins configured as SMR sources.

Table 193. Operational Amplifier Electrical Characteristics (Continued)

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
PSRR	Power Supply Rejection Ratio		80		dB	V_{DD} = 2.7 V – 3.6 V; T_A = 25 ºC
A_{VOL}	Voltage Gain		80		dB	
SR+	Slew Rate while rising		12		V/µs	R_{LOAD} = 33 K; C_{LOAD} = 50 pF; A_{VCL} = 1, V_{IN} = 0.7 V to 1.7 V
SR-	Slew Rate while falling		16		V/µs	R_{LOAD} = 33 K; C_{LOAD} = 50 pF; A_{VCL} = 1, V_{IN} = 1.7 V to 0.7 V
GBW	Gain-Bandwidth Product	5			MHz	
FM	Phase Margin		50		degree	
I_S	Supply Current			1	mA	V_{DD} = 3.6 V; V_{OUT}= V_{DD} ÷ 2
T_{WUP}	Wake up time from off state			20	µs	

Table 203. ZNEO Z16F Series Part Numbering

Part Number	Flash (Kbytes)	RAM (Kbytes)	External Interface	I/O	Multi-Channel timers with PWM	Standard Timers with PWM	ADC Inputs	I^2C Master/Slave	UART with LIN and IrDA	ESPI	Package
Automotive Temperature: –40°C to +125°C											
Z16F2811AL20AG	128	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F2811FI20AG	128	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F2810FI20AG	128	4	No	60	1	3	12	1	2	1	80-pin QFP
Z16F2810AG20AG	128	4	No	46	1	3	12	1	2	1	64-pin LQFP
Z16F2810VH20AG	128	4	No	46	1	3	12	1	2	1	68-pin PLCC
Z16F6411AL20AG	64	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F6411FI20AG	64	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F3211AL20AG	32	2	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F3211FI20AG	32	2	Yes	60	1	3	12	1	2	1	80-pin QFP

ZNEO Z16F Series Development Tools	
Z16F2800100ZCOG	ZNEO® Z16F Series Development Kit
ZUSBSC00100ZACG	USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG	Opto-Isolated USB Smart Cable Accessory Kit
ZENETSC0100ZACG	Ethernet Smart Cable Accessory Kit