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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f3211al20eg

List of Tables

Use of the Terms LSB, MSB, lsb, and msb

In this document, the terms LSB and MSB, when appearing in upper case, mean least significant byte and most significant byte, respectively. The lowercase forms, lsb and msb, mean least significant bit and most significant bit, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings and modes in general text.

Example 1. The receiver forces the SCL line to Low.

Example 2. Stop Mode.

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states and commands.

Example 1. The bus is considered BUSY after the Start condition.

Example 2. A Start command triggers the processing of the initialization sequence.

Bit Numbering

Bits are numbered from 0 to *n*–1, in which *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that all users understand the following safety terms, which are defined here.

Caution: Indicates that a procedure or file may become corrupted if you do not follow instructions.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E03B	IRQ2 Enable Low Bit	IRQ2ENL	00	92
FF_E03C-FF_E03F	Reserved	—	XX	—
Watchdog Timer Base Address = FF_E040				
FF_E040-FF_E041	Reserved	—	—	—
FF_E042	Watchdog Timer Reload High Byte	WDTH	04	241
FF_E043	Watchdog Timer Reload Low Byte	WDTL	00	241
FF_E044-FF_E04F	Reserved	—	—	—
Reset Base Address = FF_E050				
FF_E050	Reset Status and Control Register	RSTSCR	XX	62
FF_E051-FF_E06F	Reserved	—	XX	—
Flash Controller Base Address = FF_E060				
FF_E060	Flash Command Register	FCMD	XX	261
FF_E060	Flash Status Register	FSTAT	00	262
FF_E061	Flash Control Register	FCTL	00	263
FF_E062	Flash Sector Protect Register	FSECT	00	264
FF_E063	Reserved	—	XX	—
FF_E064-FF_E065	Flash Page Select Register	FPAGE	0000	265
FF_E066-FF_E067	Flash Frequency Register	FFREQ	0000	266
External Interface Base Address = FF_E070				
FF_E070	External Interface Control	EXTCT		42
FF_E071	Reserved	—	—	—
FF_E072	Chip Select 0 Control High	EXTCS0H		43
FF_E073	Chip Select 0 Control Low	EXTCS0L		44
FF_E074	Chip Select 1 Control High	EXTCS1H		43
FF_E075	Chip Select 1 Control Low	EXTCS1L		45
FF_E076	Chip Select 2 Control High	EXTCS2H		43
FF_E077	Chip Select 2 Control Low	EXTCS2L		46
FF_E078	Chip Select 3 Control High	EXTCS3H		43
FF_E079	Chip Select 3 Control Low	EXTCS3L		46
FF_E07A	Chip Select 4 Control High	EXTCS4H		43

XX = Undefined.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E132	Port D Data Direction	PDDD	00	73
FF_E133	Port D High Drive Enable	PDHDE	00	74
FF_E134	Port D Alternate Function High	PDAFH	00	75
FF_E135	Port D Alternate Function Low	PDAFL	00	76
FF_E136	Port D Output Control	PDOC	00	76
FF_E137	Port D Pull-Up Enable	PDPUE	00	76
FF_E138	Port D Stop Mode Recovery Enable	PDSMRE	00	77
FF_E139-FF_E13F	Port D Reserved	—	—	—
GPIO Port E Base Address = FF_E140				
FF_E140	Port E Input Data	PEIN	XX	71
FF_E141	Port E Output Data	PEOUT	00	72
FF_E142	Port E Data Direction	PEDD	00	73
FF_E143	Port E High Drive Enable	PEHDE	00	74
FF_E144	Reserved	—	—	—
FF_E145	Reserved	—	—	—
FF_E146	Port E Output Control	PEOC	00	76
FF_E147	Port E Pull-Up Enable	PEPUE	00	76
FF_E148	Port E Stop Mode Recovery Enable	PESMRE	00	77
FF_E149-FF_E14F	Port E Reserved	—	—	—
GPIO Port F Base Address = FF_E150				
FF_E150	Port F Input Data	PFIN	XX	71
FF_E151	Port F Output Data	PFOUT	00	72
FF_E152	Port F Data Direction	PFDD	00	73
FF_E153	Port F High Drive Enable	PFHDE	00	74
FF_E154	Reserved	—	—	—
FF_E155	Port F Alternate Function Low	PFAFL	00	76
FF_E156	Port F Output Control	PFOC	00	76
FF_E157	Port F Pull-Up Enable	PFPUE	00	76
FF_E158	Port F Stop Mode Recovery Enable	PFSMRE	00	77
FF_E159-FF_E15F	Port F Reserved	—	—	—

XX = Undefined.

Bit	Description
[4] PWMFENL	PWM Fault Interrupt Request Enable Low Bit.
[3:0] CxENL/ DMAxENL	Port C*x* or *DMAx* Interrupt Request Enable Low Bit.

PWM Reload High and Low Byte Registers

The PWM Reload High and Low Byte (PWMRH and PWMRL) registers, shown in Tables 66 and 67, store a 12-bit reload value, {PWMRH[3:0], PWMRL[7:0]}. The PWM reload value is held in buffer registers. The PWM reload value written to the buffer registers are not used by the PWM generator until the next PWM reload event occurs. Reads from these registers always return the values from the buffer registers.

$$\text{Edge-Aligned PWM Mode Period} = \frac{\text{Prescaler} \times \text{Reload Value}}{f_{PWMclk}}$$

$$\text{Center-Aligned PWM Mode Period} = \frac{2 \times \text{Prescaler} \times \text{Reload Value}}{f_{PWMclk}}$$

Table 66. PWM Reload High Byte Register (PWMRH)

Bits	7	6	5	4	3	2	1	0
Field	Reserved				PWMRH			
RESET	0h				Fh			
R/W	R/W				R/W			
Addr	FF_E38EH							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] PWMRH	**PWM Reload Register High and Low** These two bytes form the 12-bit reload value, {PWMRH[3:0], PWMRL[7:0]}. This value sets the PWM period.

Table 67. PWM Reload Low Byte Register (PWMRL)

Bits	7	6	5	4	3	2	1	0
Field	PWMRL							
RESET	FF							
R/W	R/W							
Addr	FF_E38Fh							

Bit	Description
[7:0] PWMRL	**PWM Reload Register High and Low** These two bytes form the 12-bit reload value, {PWMRH[3:0], PWMRL[7:0]}. This value sets the PWM period.

Bit	Description (Continued)
[3] ADCTRIG	**ADC Trigger Enable** 0 = No ADC trigger pulses. 1 = ADC trigger enabled.
[2]	**Reserved** This bit is reserved and must be programmed to 0.
[1] READY	**Values Ready for Next Reload Event** 0 = PWM values (prescale, period and duty cycle) are not ready. Do not use values in holding registers at next PWM reload event. 1 = PWM values (prescale, period and duty cycle) are ready. Transfer all values from temporary holding registers to working registers at next PWM reload event.
[0] PWMEN	**PWM Enable** 0 = PWM is disabled and enabled PWM output pins are forced to default off-state. PWM master counter is stopped. Certain control registers may only be written in this state. 1 = PWM is enabled and PWM output pins are enabled as outputs.

PWM Control 1 Register

The PWM Control 1 (PWMCTL1) Register controls portions of PWM operation.

Table 71. PWM Control 1 Register (PWMCTL1)

Bits	7	6	5	4	3	2	1	0
Field	RLFREQ[1:0]		INDEN	POL45	POL23	POL10	PRES[1:0]	
RESET	00		0	0	0	0	00	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Addr	FF_E381h							

Bit	Description
[7:6] RLFREQ[1:0]	**Reload Event Frequency** This bit field is buffered. Changes to the reload event frequency takes effect at the end of the current PWM period. Reads always return the bit values from the temporary holding register. 00 = PWM reload event occurs at the end of every PWM period. 01 = PWM reload event occurs once every two PWM periods. 10 = PWM reload event occurs once every four PWM periods. 11 = PWM reload event occurs once every eight PWM periods.
[5] INDEN	**Independent PWM Mode Enable** 0 = PWM outputs operate as three complementary pairs. 1 = PWM outputs operate as six independent channels.

Baud Rate Generator Interrupts

If the BRGCTL bit of the Multiprocessor Contrd Register (LIN-UART Control 1 Register with MSEL = 000b) register is set and the REN bit of the Control 0 Register is 0, the LIN-UART receiver interrupt asserts when the LIN-UART baud rate generator reloads. This action allows the BRG to function as an additional counter if the LIN-UART receiver functionality is not employed. The transmitter is enabled in this mode.

LIN-UART DMA Interface

The DMA engine is configured to move UART transmit and/or receive data. This reduces processor overhead, especially when moving blocks of data. The DMA interface on the LIN-UART consists of the TxDmaReq and RxDmaReq outputs and the TxDmaAck and RxDmaAck inputs. Any of the DMA channels are configured to process the UART DMA requests.

If transmit data is to be moved by the DMA, the transmit interrupt must be disabled in the interrupt controller. If receive data is to be moved by the DMA, the RDAIRQ bit in the LIN-UART Control 1 Register must be set. This disables receive data interrupts when still enabling error interrupts. The receive interrupt must be enabled in the interrupt controller to process error condition interrupts.

LIN-UART Baud Rate Generator

The LIN-UART baud rate generator creates a lower frequency baud rate clock for data transmission. The input to the BRG is the system clock. The LIN-UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) which sets the data transmission rate (baud rate) of the LIN-UART. The LIN-UART data rate is calculated using the following equation for normal UART operation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

The LIN-UART data rate is calculated using the following equation for LIN Mode UART operation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{\text{UART Baud Rate Divisor Value}}$$

When the LIN-UART is disabled, the BRG functions as a basic 16-bit timer with interrupt on time-out. Observe the following steps to configure BRG as a timer with interrupt on time-out:

1. Disable the LIN-UART receiver by clearing the REN bit in the LIN-UART Control 0 Register to 0 (TEN bit is asserted, transmit activity may occur).

Table 85. Multiprocessor Mode Status Field (MSEL = 000b)

NE	**Noise Event** This bit is asserted if digital noise is detected on the receive data line when the data is sampled (center of bit time). If this bit is set, it does not mean that the receive data is corrupted (in extreme cases), just that one or more of the noise filter data samples near the center of the bit time did not match the average data value.
NEWFRM	**New Frame** Status bit denoting the start of a new frame. Reading the LIN-UART Receive Data Register Resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame.
MPRX	**Multiprocessor Receive** Returns the value of the last multiprocessor bit received. Reading from the LIN-UART Receive Data Register Resets this bit to 0.

Table 86. Digital Noise Filter Mode Status Field (MSEL = 001b)

NE	**Noise Event** This bit is asserted if digital noise is detected on the receive data line while the data is sampled (center of bit time). If this bit is set, it does not mean that the receive data is corrupted (in extreme cases), just that one or more of the noise filter data samples near the center of the bit time did not match the average data value.

Table 87. LIN Mode Status Field (MSEL = 010b)

NE	**Noise Event** This bit is asserted if some noise level is detected on the receive data line when the data is sampled (center of bit time). If this bit is set, it does not indicate that the receive data is corrupt (in extreme cases), just that one or more of the 16x data samples near the center of the bit time did not match the average data value.
RxBreak-Length	**LIN Mode Received Break Length** This field is read following a break (LIN WAKE-UP or BREAK) so software determines the measured duration of the break. If the break exceeds 15 bit times the value saturates at 1111b.

Table 88. Hardware Revision Mode Status Field (MSEL = 111b)

LIN-UART Hardware Revision	This field indicates the hardware revision of the LIN-UART block. 00_xxx LIN UART hardware rev 01_xxx Reserved 10_xxx Reserved 11_xxx Reserved

words, 24 baud clock periods since the previous pulse was detected). This open window allows the endec a sampling of minus 4 baudrate clocks to plus 8 baudrate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window, this process is repeated. If the incoming data is a logical 1 (no pulse), the endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the endec clock counter is reset, resynchronizing the endec to the incoming signal. This allows the endec to tolerate jitter and baud rate errors in the incoming data stream. Resynchronizing the endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

Infrared Encoder/Decoder Control Register Definitions

Caution: All infrared endec configuration and status information is set by the UART control registers as defined in the beginning of the LIN-UART Control Register Definitions section on page 153.

To prevent spurious signals during IrDA data transmission, set the IREN bit in the UARTx Control 1 Register to 1 to enable the infrared encoder/decoder before enabling the GPIO port alternate function for the corresponding pin.

0 for General Call Address). For a General Call Address, the I2C Controller automatically responds during the address acknowledge phase with the value in the NAK bit of the I2CCTL Register. If software processes the data bytes associated with the GCA bit, the IRM bit is optionally set following the SAM interrupt to allow software to examine each received data byte before deciding to set or clear the NAK bit. A Start byte will not be acknowledged (requirement the I2C specification).

Software Address Recognition Mode. To disable the hardware address recognition, the IRM bit must be set = 1 prior to the reception of the address byte(s). When IRM = 1 each received byte generates a receive interrupt (RDRF = 1 in the I2CISTAT Register). Software must examine each byte and determine whether to set or clear the NAK bit. The Slave holds SCL Low during the acknowledge phase until software responds by writing to the I2CCTL Register. The value written to the NAK bit is used by the controller to drive the I2C Bus, then releasing the SCL. The SAM and GCA bits are not set when IRM = 1 during the address phase, but the RD bit is updated based on the first address byte.

Slave Transaction Diagrams

In the following transaction diagrams, shaded regions indicate data transferred from the Master to the Slave and unshaded regions indicate data transferred from the Slave to the Master. The transaction field labels are defined as follows:

S: Start

W: Write

A: Acknowledge

$\overline{A}$: Not Acknowledge

P: Stop

Slave Receive Transaction with 7-Bit Address

The data transfer format for writing data from Master to Slave in 7-bit address Mode is shown in Figure 47. The following procedure describes the I2C Master/Slave Controller operating as a Slave in 7-bit address Mode, receiving data from the bus Master.

S	Slave Address	W=0	A	Data	A	Data	A	Data	A/$\overline{A}$	P/S

Figure 48. Data Transfer Format, Slave Receive Transaction with 7-Bit Addressing

1. Software configures the controller for operation as a Slave in 7-Bit Address Mode as follows.
   a. Initialize the MODE field in the I2C Mode Register for either Slave Only Mode or Master/Slave Mode with 7-Bit Addressing.

Watchdog Timer Register Definitions

Watchdog Timer Reload High and Low Byte Registers

The Watchdog Timer Reload High and Low Byte (WDTH, WDTL) registers, shown in Table 124 through Table 125) form the 16-bit reload value that is loaded into the WDT when a WDT instruction executes. The 16-bit reload value is {WDTH[7:0], WDTL[7:0]}. Writing to these registers following the unlock sequence sets the appropriate reload value. Reading from these registers returns the current WDT count value.

Caution: The 16-bit WDT Reload Value must not be set to a value less than 0004h.

Table 124. Watchdog Timer Reload High Byte Register (WDTH)

Bits	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	0	0	0	0	0	1	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Addr	FF_E042h							

Note: R/W* = Read returns the current WDT count value. Write sets the appropriate Reload Value.

Bit	Description
[7:0] WDTH	**WDT Reload High Byte** Most significant byte (MSB), Bits[15:8], of the 16-bit WDT reload value.

Table 125. Watchdog Timer Reload Low Byte Register (WDTL)

Bits	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Addr	FF_E043h							

Note: R/W* = Read returns the current WDT count value. Write sets the appropriate Reload Value.

Bit	Description
[7:0] WDTL	**WDT Reload Low Byte** Least significant byte (LSB), Bits[7:0], of the 16-bit WDT reload value.

ADC0 Data Low Bits Register

The ADC0 Data Low Bits Register contains the lower bits of the ADC0 output. Access to the ADC0 Data Low Bits Register is Read-Only.

Table 128. ADC0 Data Low Bits Register (ADC0D_L)

Bits	7	6	5	4	3	2	1	0
Field	ADC0D_L		Reserved					
RESET	X		X					
R/W	R		R					
Addr	FF–E503h							

Bit	Description
[7:6] ADC0D_L	**ADC0 Low Bits** 00–11b = These bits are the 2 least significant bits of the 10-bit ADC0 output. These bits are undefined after a Reset.
[5:0]	**Reserved** These bits are reserved and must be programmed to 0.

Sample Settling Time Register

The Sample Settling Time Register is used to program the length of time from the SAMPLE/$\overline{\text{HOLD}}$ signal to the Start signal, when the conversion begins. The number of clock cycles required for settling varies from system to system depending on the system clock period used. This register must be programmed to contain the number of clocks required to meet a 0.5µs minimum settling time.

Table 129. Sample and Settling Time (ADCSST)

Bits	7	6	5	4	3	2	1	0
Field	Reserved			SST				
RESET	0	0	0	1	1	1	1	1
R/W	R			R/W				
Addr	FF–E504h							

Bit	Description
[7:5]	**Reserved** These bits are reserved and must be programmed to 0.
[4:0] SST	**Sample Settling Time** 00h–1Fh = Sample settling time in number of system clock periods to meet 0.5µs minimum.

Flash Control Register

The Flash Control Register, shown in Table 141, selects how the Flash memory is accessed.

Table 141. Flash Control Register (FCTL)

Bits	7	6	5	4	3	2	1	0
Field	INFO	Reserved						
RESET	0	00h						
R/W	R/W	R						
Addr	FF_E061h							

Bit	Description
[7] INFO	**Information Area Access** This bit selects access to the information area. 0 = Information Area is not selected. 1 = Information Area is selected. The Information area is mapped into the Program memory address space at addresses 000000h through 00007Fh.
[6:0]	**Reserved** These bits are reserved and must be programmed to 0000000.

Bit	Description (Continued)
[6] LPOPT	**Low Power Option** 0 = The part will come up in low power mode. The Clock is divided by 8 and Flash memory will only be accessed the last half of the last cycle of the divide. This reduces Flash power consumption. 1 = The part will come up normally.
[5:0]	**Reserved** These option bits are reserved for future use and must always be 1. This setting is the default for unprogrammed (erased) Flash.

Information Area

Data in the information area of memory cannot be altered directly. If you wish to alter the factory settings, it must be done by writing to the Register Address identified. The part defaults to the factory settings after reset and the registers must be rewritten to have the user settings in effect. Read the information area address to determine the factory settings.

IPO Trim Registers (Information Area Address 0021h and 0022h)

Tables 165 and 166 define the IPO Trim settings, which are altered after reset by accessing the IPOTRIM1 and IPOTRIM2 registers.

Table 165. IPO Trim 1 (IPOTRIM1)

Bits	7	6	5	4	3	2	1	0
Field	IPO TEMP TRIM						IPO TRIM	
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF25h							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

Table 166. IPO Trim 2 (IPOTRIM2)

Bits	7	6	5	4	3	2	1	0
Field	IPO TRIM							
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF26							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

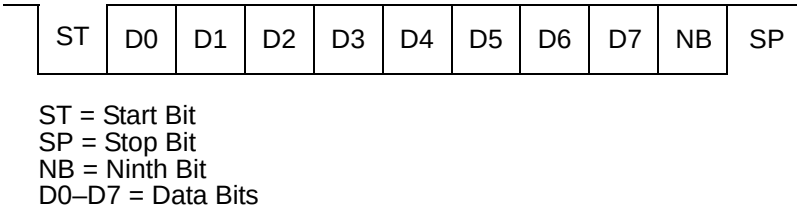

Figure 67. 9-Bit Mode

Start Bit Flow Control

If flow control is required, start bit flow control is used. Start bit flow control requires the receiving device send the start bit. The transmitter waits for the start bit, then transmit its data following the start bit.

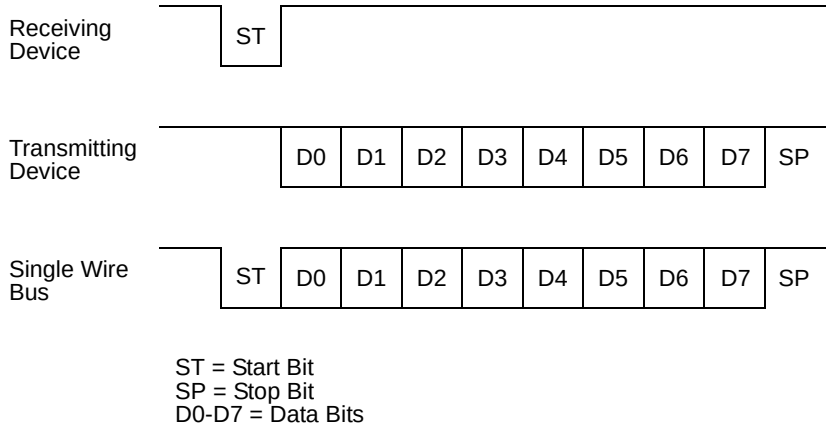

Figure 68. Start Bit Flow Control

If the standard serial port of a PC is used, transmit flow control is enabled on the ZNEO Z16F Series device. The PC sends the start bit when receiving data by transmitting the character FFh. Because the FFh character is also received from a nonresponsive device, space parity (parity bit always zero) must be enabled and used as an acknowledge bit.

Initialization

The OCD ignores any data received until it receives the read revision command 00h. After the read revision command is received, the remaining debug commands are issued. The packet CRC is not sent for the first read revision command issued during initialization.

```
DBG <<- regdata[23:16]
DBG <<- regdata[15:8]
DBG <<- regdata[7:0]
DBG --> CRC[0:7]
```

Read PC. The Read Program Counter command returns the contents of the program counter.

```
DBG <-- 0000_0110
DBG --> 00h
DBG --> PC[23:16]
DBG --> PC[15:8]
DBG --> PC[7:0]
DBG --> CRC[0:7]
```

Write PC. The Write Program Counter command writes data to the program counter.

```
DBG <-- 0000_0111
DBG <-- 00h
DBG <-- PC[23:16]
DBG <-- PC[15:8]
DBG <-- PC[7:0]
DBG --> CRC[0:7]
```

Read Flags. The Read Flags command returns the contents of the CPU flags.

```
DBG <-- 0000_1000
DBG --> 00h
DBG --> flags[7:0]
DBG --> CRC[0:7]
```

Write Instruction. The Write Instruction command writes one word of Op Code to the CPU.

```
DBG <-- 0000_1001
DBG <-- opcode[15:8]
DBG <-- opcode[7:0]
DBG --> CRC[0:7]
```

Read Register. The Read Register command returns the contents of a single CPU register.

```
DBG <-- {0100,regno[3:0]}
DBG --> regdata[31:24]
DBG --> regdata[23:16]
DBG --> regdata[15:8]
DBG --> regdata[7:0]
DBG --> CRC[0:7]
```

Write Register. The Write Register command writes data to a single CPU register.

```
DBG <-- {0101,regno[3:0]}
DBG <-- regdata[31:24]
DBG <-- regdata[23:16]
DBG <-- regdata[15:8]
DBG <-- regdata[7:0]
DBG --> CRC[0:7]
```

Oscillator Operation with an External RC Network

Figure 71 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.

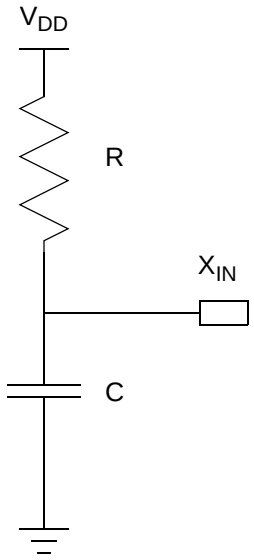

Figure 71. Connecting the On-Chip Oscillator to an External RC Network

An external resistance value of 15 kΩ is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 10 kΩ. The typical oscillator frequency is estimated from the values of the resistor (*R* in kΩ) and capacitor (*C* in pF) elements using the following equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1\times10^{6}}{(1.5 \times R \times C)}$$

Figure 3 displays the typical (3.3 V and 25°C) oscillator frequency as a function of the capacitor (*C* in pF) employed in the RC network assuming a 15kΩ external resistor. For very small values of C, the parasitic capacitance of the oscillator X_{IN} pin and the printed circuit board must be included in the estimation of the oscillator frequency.

Electrical Characteristics

All data in this chapter is prequalification and precharacterization and is subject to change.

Absolute Maximum Ratings

Stress greater than those listed in Table 185 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 185. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	–40	+125	C	
Storage temperature	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V	2
Maximum current on input and/or inactive output pin	–5	+5	µA	
Maximum output current from active output pin	–25	+25	mA	
100-Pin LQFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		1325	mW	
Maximum current into V_{DD} or out of V_{SS}		368	mA	
100-Pin LQFP Maximum Ratings at 70°C to 125°C				
Total power dissipation		482	mW	
Maximum current into V_{DD} or out of V_{SS}		134	mA	
80-Pin QFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		550	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
80-Pin QFP Maximum Ratings at 70°C to 125°C				
Total power dissipation		200	mW	

Notes:
1. This voltage applies to 5 V tolerant pins which are Port A, C, D, E, F and G pins (except pins PC0 and PC1).
2. This voltage applies to V_{DD}, AV_{DD}, pins supporting analog input (Ports B and H), Pins PC0 and PC1, RESET, DBG and X_{IN} pins which are non 5 V tolerant pins.

On-Chip Peripheral AC and DC Electrical Characteristics

Table 187 lists the POR and VBO electrical characteristics and timing. Table 188 lists the Reset and Stop Mode Recovery pin timing.

Table 187. POR and VBO Electrical Characteristics and Timing

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
V_{POR}	Power-On Reset voltage threshold	2.20	2.45	2.70	V	$V_{DD} = V_{POR}$
V_{VBO}	Voltage Brown-Out reset voltage threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$
	V_{POR}–V_{VBO}		50	100	mV	
	Starting V_{DD} voltage to ensure valid POR	—	V_{SS}	—	V	
T_{ANA}	Power-On Reset analog delay	—	50	—	ms	$V_{DD} > V_{POR}$; T_{POR} Digital Reset delay follows T_{ANA}
T_{POR}	Power-On Reset digital delay	—	12	—	µs	66 IPO cycles
T_{VBO}	Voltage Brown-Out pulse rejection period	—	10	—	ms	$V_{DD} < V_{VBO}$ to generate a Reset
T_{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset	0.10	—	100	ms	
I_{CC}	Supply current		500		µA	V_{DD} = 3.3 V.

Note:
1. Data in the typical column is from characterization at 3.3 V and 0°C. These values are provided for design guidance only and are not tested in production.

Table 188. Reset and Stop Mode Recovery Pin Timing

		T_A = –40°C to 125°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
T_{RESET}	$\overline{\text{RESET}}$ pin assertion to initiate a System Reset	4	—	—	T_{CLK}	Not in Stop Mode. T_{CLK} = System Clock period.
T_{SMR}	Stop Mode Recovery pin Pulse Rejection Period	10	20	40	ns	RESET, DBG and GPIO pins configured as SMR sources.