Zilog - Z16F3211FI20AG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f3211fi20ag

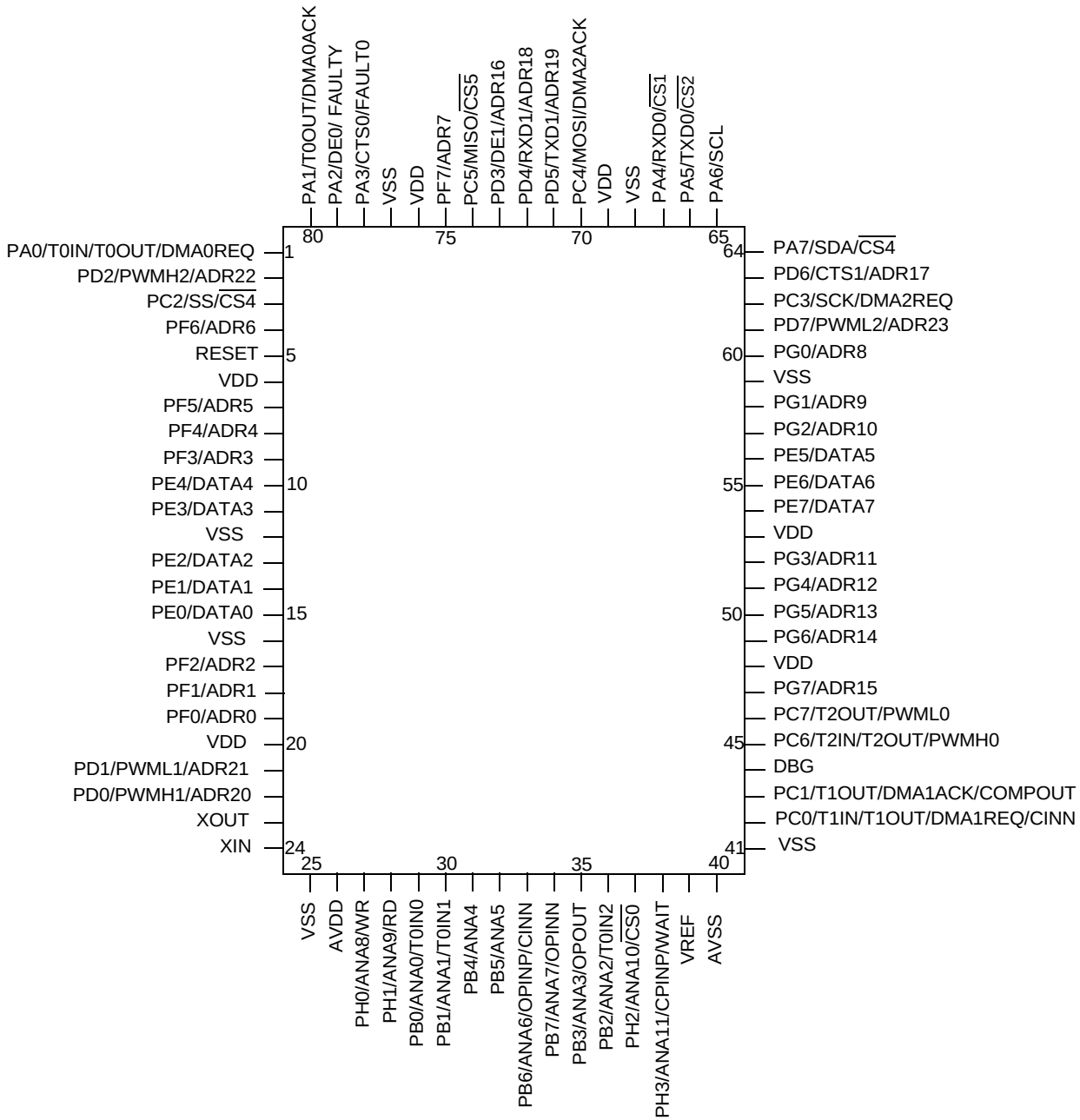

Figure 4. ZNEO Z16F Series, 80-Pin Quad Flat Package (QFP)

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
GPIO Port G Base Address = FF_E160				
FF_E160	Port G Input Data	PGIN	XX	71
FF_E161	Port G Output Data	PGOUT	00	72
FF_E162	Port G Data Direction	PGDD	00	73
FF_E163	Port G High Drive Enable	PGHDE	00	74
FF_E164	Reserved	—	—	—
FF_E165	Port G Alternate Function Low	PGAFL	00	76
FF_E166	Port G Output Control	PGOC	00	76
FF_E167	Port G Pull-Up Enable	PGPUE	00	76
FF_E168	Port G Stop Mode Recovery Enable	PGSMRE	00	77
FF_E169-FF_E16F	Port G Reserved	—	—	—
GPIO Port H Base Address = FF_E170				
FF_E170	Port H Input Data	PHIN	XX	71
FF_E171	Port H Output Data	PHOUT	00	72
FF_E172	Port H Data Direction	PHDD	00	73
FF_E173	Port H High Drive Enable	PHHDE	00	74
FF_E174	Port H Alternate Function High	PHAFH	00	75
FF_E175	Port H Alternate Function Low	PHAFL	00	76
FF_E176	Port H Output Control	PHOC	00	76
FF_E177	Port H Pull-Up Enable	PHPUE	00	76
FF_E178	Port H Stop Mode Recovery Enable	PHSMRE	00	77
FF_E179-FF_E17F	Port H Reserved	—	—	—
GPIO Port J Base Address = FF_E180				
FF_E180	Port J Input Data	PJIN	XX	71
FF_E181	Port J Output Data	PJOUT	00	72
FF_E182	Port J Data Direction	PJDD	00	73
FF_E183	Port J High Drive Enable	PJHDE	00	74
FF_E184	Reserved	—	—	—
FF_E185	Reserved	—	—	—
FF_E186	Port J Output Control	PJOC	00	76
FF_E187	Port J Pull-Up Enable	PJPUE	00	76

XX = Undefined.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E188	Port J Stop Mode Recovery Enable	PJSMRE	00	77
FF_E189-FF_E18F	Port J Reserved	—	—	—
GPIO Port K Base Address = FF_E190				
FF_E190	Port K Input Data	PKIN	XX	71
FF_E191	Port K Output Data	PKOUT	00	72
FF_E192	Port K Data Direction	PKDD	00	73
FF_E193	Port K High Drive Enable	PKHDE	00	74
FF_E194	Reserved	—	—	—
FF_E195	Port K Alternate Function Low	PKAFL	00	76
FF_E196	Port K Output Control	PKOC	00	76
FF_E197	Port K Pull-Up Enable	PKPUE	00	76
FF_E198	Port K Stop Mode Recovery Enable	PKSMRE	00	77
FF_E199-FF_E19F	Port K Reserved	—	—	—
Serial Channels Base Address = FF_E200				
LIN-UART 0 Base Address = FF_E200				
FF_E200	LIN-UART0 Transmit Data	U0TXD	XX	154
	LIN-UART0 Receive Data	U0RXD	XX	154
FF_E201	LIN-UART0 Status 0	U0STAT0	0000011Xb	155
FF_E202	LIN-UART0 Control 0	U0CTL0	00	160
FF_E203	LIN-UART0 Control 1	U0CTL1	00	164
FF_E204	LIN-UART0 Mode Select and Status	U0MDSTAT	00	162
FF_E205	LIN-UART0 Address Compare Register	U0ADDR	00	166
FF_E206	LIN-UART0 Baud Rate High Byte	U0BRH	FF	166
FF_E207	LIN-UART0 Baud Rate Low Byte	U0BRL	FF	167
FF_E208-FF_E20F	Reserved	—	XX	—
LIN-UART 1 Base Address = FF_E210				

XX = Undefined.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E43A	DMA2 Source Address High	DMA2SARH	00	288
FF_E43B	DMA2 Source Address Low	DMA2SARL	00	288
FF_E43C	Reserved			
FF_E43D	DMA2 List Address Upper	DMA2LARU	00	289
FF_E43E	DMA2 List Address High	DMA2LARH	00	289
FF_E43F	DMA2 List Address Low	DMA2LARL	00	289
DMA Channel 3 Base Address = FF_E440				
FF_E440	DMA3 Control 0	DMA3CTL0	00	285
FF_E441	DMA3 Control 1	DMA3CTL1	00	285
FF_E442	DMA3 Transfer Length High	DMA3TXLNH	00	286
FF_E443	DMA3 Transfer Length Low	DMA3TXLNL	00	287
FF_E444	Reserved	—	—	—
FF_E445	DMA3 Destination Address Upper	DMA3DARU	00	287
FF_E446	DMA3 Destination Address High	DMA3DARH	00	287
FF_E447	DMA3 Destination Address Low	DMA3DARL	00	287
FF_E448	Reserved	—	—	—
FF_E449	DMA3 Source Address Upper	DMA3SARU	00	288
FF_E44A	DMA3 Source Address High	DMA3SARH	00	288
FF_E44B	DMA3 Source Address Low	DMA3SARL	00	288
FF_E44C	Reserved	—	—	—
FF_E44D	DMA3 List Address Upper	DMA3LARU	00	289
FF_E44E	DMA3 List Address High	DMA3LARH	00	289
FF_E44F	DMA3 List Address Low	DMA3LARL	00	289
Analog Block Base Address = FF_E500				
ADC Base Address = FF_E500				
FF_E500	ADC0 Control Register	ADC0CTL	00	246
FF_E501	Reserved	—	—	—
FF_E502	ADC0 Data High Byte Register	ADC0D_H	XX	247
FF_E503	ADC0 Data Low Bits Register	ADC0D_L	XX	248

XX = Undefined.

Timer 0–2 PWM High and Low Byte Registers

The Timer 0–2 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 60 and 61, define PWM operations and store the timer counter values for the Capture modes. These TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in Capture or Capture/Compare modes.

Table 60. Timer 0–2 PWM High Byte Register (TxPWMH)

Bits	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	00h							
R/W	R/W							
Addr	FF–E304h, FF–E314h, FF–E324h							

Bit	Description
[7:0] PWMH	**Pulse-Width Modulator High and Low Bytes** These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value which is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control 1 Register (TxCTL1).

Table 61. Timer 0–2 PWM Low Byte Register (TxPWML)

Bits	7	6	5	4	3	2	1	0
Field	PWML							
RESET	00h							
R/W	R/W							
Addr	FF–E305h, FF–E315h, FF–E315h							

Bit	Description
[7:0] PWML	**Pulse-Width Modulator High and Low Bytes** These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value which is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control 1 Register (TxCTL1).

Timer 0–2 Control Registers

Timer 0–2 Control 0 Register

The Timer 0–2 Control 0 Register (TxCTL0), together with the Timer 0–2 Control 1 (TxCTL1) Register, determines timer configuration and operation.

Bit	Description (Continued)
[3:1] PWMD	**PWM Delay Value** This field is a programmable delay to control the number of additional system clock cycles following a PWM or Reload compare before the timer output or the timer output complement is switched to the active state. This field ensures a time gap between deassertion of one PWM output to the assertion of its complement. No delay. 2 cycles delay. 4 cycles delay. 8 cycles delay. 16 cycles delay. 32 cycles delay. 64 cycles delay. 128 cycles delay.
[0] INCAP	**Input Capture Event** 0 = Previous timer interrupt is not a result of a timer input capture event. 1 = Previous timer interrupt is a result of a timer input capture event.

Timer 0–2 Control 1 Register

The Timer 0–2 Control 1 (TxCTL1) Register enables/disables the timer, sets the prescaler value and determines the timer operating mode.

Table 63. Timer 0–2 Control 1 Register (TxCTL1)

Bits	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	000			000		
R/W	R/W	R/W	R/W			R/W		
Addr	FF–E307h, FF–E317h, FF–E327h							

Bit	Description
[7] TEN	0 = Timer is disabled. 1 = Timer is enabled. **Note:** the TEN bit is cleared automatically when the timer stops.

Multi-Channel PWM Timer

The ZNEO® Z16F Series includes a Multi-Channel PWM optimized for motor control applications. The PWM includes the following features:

- Six independent PWM outputs or three complementary PWM output pairs
- Programmable deadband insertion for complementary output pairs
- Edge-aligned or center-aligned PWM signal generation
- PWM off-state is an option bit programmable
- PWM outputs driven to off-state on System Reset
- Asynchronous disabling of PWM outputs on system fault; outputs are forced to off-state
- Fault inputs generate pulse-by-pulse or hard shutdown
- 12-bit reload counter with 1, 2, 4 or 8 programmable clock prescaler
- High current source and sink on all PWM outputs
- PWM pairs used as general purpose inputs when outputs are disabled
- ADC synchronized with PWM period
- Synchronization for current-sense sample and hold
- Narrow pulse suppression with programmable threshold

Architecture

The PWM unit consists of a master timer to generate the modulator time base and six independent compare registers to set the PWM for each output. The six outputs are designed to provide control signals for inverter drive circuits. The outputs are grouped into pairs consisting of a high-side driver and a low-side driver output. The output pairs are programmable to operate independently or as complementary signals.

In complementary output mode, a programmable dead-time is inserted to ensure nonoverlapping signal transitions. The master count and compare values feed into modulator logic which generates the proper transitions in the output states. Output polarity and fault/off-state control logic allows programming of the default off-states which forces the outputs to a safe state in the event a fault in the motor drive is detected. Figure 21 displays the architecture of the PWM modulator.

PWM Fault Status Register (PWMFSTAT) is read to determine which fault source caused the interrupt.

When a fault is detected and the PWM outputs are disabled, modulator control of the PWM outputs are reenabled either by the software or by the fault input signal deasserting. Selection of the reenable method is made using the PWM Fault Control Register (PWMFCTL). Configuration of the fault modes and reenable methods allow pulse-by-pulse limiting and hard shutdown. When configured in Automatic Restart Mode, the PWM outputs are reengaged at beginning of the next PWM cycle (master timer value is equal to 0) if all fault signals are deasserted. In software controlled restart, all fault inputs must be deasserted and the fault flags must be cleared.

The fault input pin is Schmitt-triggered. The input signal from the pin as well as the comparators pass though an analog filter to reject high-frequency noise.

The logic path from the fault sources to the PWM output is asynchronous ensuring that the fault inputs forces the PWM outputs to their off-state even if the system clock is stopped.

PWM Operation in CPU Halt Mode

When the ZNEO CPU is operating in Halt Mode, the PWM continues to operate if it is enabled. To minimize current in Halt Mode, the PWM must be disabled by clearing the PWMEN bit to 0.

PWM Operation in CPU Stop Mode

When the ZNEO CPU is operating in Stop Mode, the PWM is disabled as the system clock ceases to operate in Stop Mode. The PWM output remains in the same state as they were prior to entering the Stop Mode. In normal operation, the PWM outputs must be disabled by software prior to the CPU entering the Stop Mode. A fault condition detected in Stop Mode forces the PWM outputs to the predefined off-state.

Observing the State of PWM Output Channels

The logic value of the PWM outputs is sampled by reading the PWMIN Register. If a PWM channel pair is disabled (option bit is not set), the associated PWM outputs are forced to high impedance and are used as general purpose inputs.

PWM Control Register Definitions

The following sections describe the various PWM control registers.

Bit	Description (Continued)
[1] Fault0INT	**Fault 0 Interrupt** 0 = Interrupt on fault 0 pin assertion disabled. 1 = Interrupt on Fault0 pin assertion enabled.
[0] Fault0RST	**Fault 0 Restart** 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. **Software Controlled Recovery** 1 = PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.

Note: This register can only be written when PWMEN is cleared.

PWM Input Sample Register

The PWM pin value is sampled by reading the PWM Input Sample Register, shown in Table 77.

Table 77. PWM Input Sample Register (PWMIN)

Bits	7	6	5	4	3	2	1	0
Field	Reserved	FAULT	IN2L	IN2H	IN1L	IN1H	IN0L	IN0H
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E386h							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] FAULT	**Sample Fault0 pin** 0 = A Low-level signal was read on the fault pin. 1 = A High-level signal was read on the fault pin.
[5:0] IN2L/IN2H/ IN1L/IN1H/ IN0L/IN0H	**Sample PWM Pins** 0 = A Low-level signal was read on the pins. 1 = A High-level signal was read on the pins.

Baud Rate Generator Interrupts

If the BRGCTL bit of the Multiprocessor Contrd Register (LIN-UART Control 1 Register with MSEL = 000b) register is set and the REN bit of the Control 0 Register is 0, the LIN-UART receiver interrupt asserts when the LIN-UART baud rate generator reloads. This action allows the BRG to function as an additional counter if the LIN-UART receiver functionality is not employed. The transmitter is enabled in this mode.

LIN-UART DMA Interface

The DMA engine is configured to move UART transmit and/or receive data. This reduces processor overhead, especially when moving blocks of data. The DMA interface on the LIN-UART consists of the TxDmaReq and RxDmaReq outputs and the TxDmaAck and RxDmaAck inputs. Any of the DMA channels are configured to process the UART DMA requests.

If transmit data is to be moved by the DMA, the transmit interrupt must be disabled in the interrupt controller. If receive data is to be moved by the DMA, the RDAIRQ bit in the LIN-UART Control 1 Register must be set. This disables receive data interrupts when still enabling error interrupts. The receive interrupt must be enabled in the interrupt controller to process error condition interrupts.

LIN-UART Baud Rate Generator

The LIN-UART baud rate generator creates a lower frequency baud rate clock for data transmission. The input to the BRG is the system clock. The LIN-UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) which sets the data transmission rate (baud rate) of the LIN-UART. The LIN-UART data rate is calculated using the following equation for normal UART operation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

The LIN-UART data rate is calculated using the following equation for LIN Mode UART operation:

$$\text{UART Data Rate (bps)} = \frac{\text{System Clock Frequency (Hz)}}{\text{UART Baud Rate Divisor Value}}$$

When the LIN-UART is disabled, the BRG functions as a basic 16-bit timer with interrupt on time-out. Observe the following steps to configure BRG as a timer with interrupt on time-out:

1. Disable the LIN-UART receiver by clearing the REN bit in the LIN-UART Control 0 Register to 0 (TEN bit is asserted, transmit activity may occur).

Table 80. LIN-UART Transmit Data Register (UxTXD)

Bits	7	6	5	4	3	2	1	0
Field	TXD							
RESET	X							
R/W	W							
Addr	FF–E200h, FF–E210h							

Bit	Description
[7:0] TXD	**Transmit Data** LIN-UART transmitter data byte to be shifted out through the TXD pin.

LIN-UART Receive Data Register

Data bytes received through the RXD pin are stored in the LIN-UART Receive Data Register, shown in Table 81. The Read-only LIN-UART Receive Data Register shares a register file address with the Write-only LIN-UART Transmit Data Register.

Table 81. LIN-UART Receive Data Register (UxRXD)

Bits	7	6	5	4	3	2	1	0
Field	RXD							
RESET	X							
R/W	R							
Addr	FF–E200h, FF–E210h							

Bit	Description
[7:0] RXD	**Receive Data** LIN-UART receiver data byte from the RXD pin

Noise Filter Control Register (LIN-UART Control 1 Register with MSEL = 001b)

When MSEL = 001b, this register, shown in Table 91, provides control for the digital noise filter.

Table 91. Noise Filter Control Register (UxCTL1 with MSEL = 001b)

Bits	7	6	5	4	3	2	1	0
Field	NFEN	NFCTL			Reserved			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R
Addr	FF–E203h, FF–E213h with MSEL = 001b							

Bit	Description
[7] NFEN	**Noise Filter Enable** 0 = Noise filter is disabled. 1 = Noise filter is enabled. Receive data is preprocessed by the noise filter.
[6:4] NFCTL	**Noise Filter Control** This field controls the delay and noise rejection characteristics of the noise filter. The wider the counter the more delay that is introduced by the filter and the wider the noise event that is filtered. 000 = 4-bit up/down counter 001 = 5-bit up/down counter 010 = 6-bit up/down counter 011 = 7-bit up/down counter 100 = 8-bit up/down counter 101 = 9-bit up/down counter 110 = 10-bit up/down counter 111 = 11-bit up/down counter
[3:0]	**Reserved** These bits are reserved and must be programmed to 0000.

9. The Master sends the Stop or Restart signal on the bus. Either of these signals cause the I2C Controller to assert the Stop interrupt (Stop bit = 1 in the I2CISTAT Register). When the Slave receive data from the Master, software takes no action in response to the Stop interrupt other than reading the I2CISTAT Register, clearing the Stop bit.

Slave Transmit Transaction with 7-Bit Address

The data transfer format for a Master reading data from a Slave in 7-bit address Mode is shown in Figure 49. The following procedure describes the I2C Master/Slave Controller operating as a Slave in 7-Bit Addressing Mode, transmitting data to the bus Master.

S	Slave Address	R=1	A	Data	A	Data	A	P/S

Figure 50. Data Transfer Format, Slave Transmit Transaction with 7-Bit Addressing

1. Software configures the controller for operation as a Slave in 7-Bit Addressing Mode as follows.
   a. Initialize the MODE field in the I2C Mode Register for either Slave Only Mode or Master/Slave Mode with 7-Bit Addressing.
   b. Optionally set the GCE bit.
   c. Initialize the SLA[6:0] bits in the I2C Slave Address Register.
   d. Set IEN = 1 in the I2C Control Register. Set NAK = 0 in the I2C Control Register.
   e. Program the Baud Rate High and Low Byte registers for the I2C baud rate.

2. The Master initiates a transfer, sending the address byte. The Slave Mode I2C Controller finds an address match and detects the R/$\overline{W}$ bit = 1 (read by Master from Slave). The I2C Controller acknowledges, indicating that it is ready to accept the transaction.The SAM bit in the I2CISTAT Register is set = 1, causing an interrupt. The RD bit is set = 1, indicating a read from the Slave.
3. Software responds to the interrupt by reading the I2CISTAT Register, clearing the SAM bit. When RD = 1, software responds by loading the first data byte into the I2CDATA Register. Software sets the TXI bit in the I2CCTL Register to enable transmit interrupts. When the Master initiates the data transfer, the I2C Controller holds SCL Low until software has written the first data byte to the I2CDATA Register.
4. SCL is released and the first data byte is shifted out.
5. When the first bit of the first data byte is transferred, the I2C controller sets the TDRE bit, which asserts the transmit data interrupt.
6. Software responds to the transmit data interrupt (TDRE = 1) by loading the next data byte into the I2CDATA Register, which clears TDRE.

ADC Overview

The ZNEO Z16F Series devices include a 12-channel ADC. The ADC converts an analog input signal to a 10-bit binary number. The features of the successive approximation ADC include:

- 12 analog input sources multiplexed with GPIO ports
- Fast conversion time (2.5 µs)
- Programmable timing controls
- Interrupt on conversion complete
- Internal voltage reference generator
- Internal reference voltage available externally
- Ability to supply external reference voltage
- Ability to perform simultaneous or independent conversions

Architecture

The architecture as illustrated in Figure 52 consists of a 12-input multiplexer, sample-and-hold amplifier and 10-bit successive approximation ADC. The ADC digitizes the signal on selected channel and stores the digitized data in the ADC data registers. In environment with high electrical noise, an external RC filter must be added at the input pins to reduce high frequency noise.

Operation

The ADC converts the analog input, ANA*x*, to a 10-bit digital representation. The equation for calculating the digital value is:

ADC Output = 1024*(ANAx/VREF)

Assuming zero gain and offset errors, any voltage outside the ADC input limits of AVSS and VREF returns all 0s or 1s, respectively.

A new conversion is initiated by either software write to the ADC Control register's Start bit or by PWM trigger. For detailed information about the PWM trigger, see the Synchronization of PWM and ADC section on page 120. Initiating a new conversion stops any conversion currently in progress and begins a new conversion. To avoid disrupting a con-

Table 145. Linked List Descriptor

Address	Even
LAR	CONTROL
LAR + 02h	TXLN
LAR + 04h	DAR High
LAR + 08h	SAR High
LAR + 0Ch	LAR High

DMA Control Bit Definitions

The following paragraphs explain the control bits of each DMA Channel.

DMAxEN

This bit if set by the CPU enables the DMA Channel for direct operation. Direct operation uses the addresses and transfer length, which has been directly written to the DMA Channel by software.

If this bit is set by a descriptor read then LINKED LIST Mode is enabled. Linked list operation starts when an address is written to the DMAxLAR. This write causes the DMA to read in the descriptor control value and addresses and place them in the DMA Channel.

LOOP

If the DMA is in LINKED LIST Mode and this bit is set to 1, it prevents the DMA from updating the descriptor when the buffer is closed. This bit is set to allow lists to loop on themselves without software intervention.

TXSIZE

The TXSIZE bits set the width of the transfer, as follows:

00 8-bit bytes are transferred on each DMA transfer. The destination and source addresses increment or decrement by 1 for each transfer if the DSTCTL and/or SRCCTL is selected for increment or decrement. The transfer length is decremented by 1 to allow 64Kbytes to be transferred.

01 A 16-bit word is transferred on each DMA transfer. The destination and source addresses increment or decrement by 2 if the DSTCTL and/or SRCCTL is selected for increment or decrement. In Word Mode, the transfer length is still decremented by 1 to allow 64Kwords to be transferred.

10 A 32-bit quad is transferred on each DMA transfer. The destination and source addresses increment or decrement by 4 if the DSTCTL and/or SRCCTL is selected for increment or decrement. In Quad Mode, the transfer length is still decremented by 1 to allow 64Kquads to be transferred.

5. Fetch the TXLN length from the descriptor and place it in the DMAxTXLN Register in the DMA Channel.
6. After the reads have been completed, the DMA starts looking for requests and transfer data until the transfer length reaches zero or the DMA receives a Request EOF signal.
7. When the DMA receives the Request EOF signal, it performs the following operations based upon the LOOP and EOF bit:
   - 00: The DMA writes the descriptor Control/Status word with the DMAxEN bit reset to 0.
   - 01: The DMA requests status from the peripheral. It then writes the descriptor Control/Status word with the DMAxEN bit reset to 0 and the status returned from the peripheral. The DMA then writes the TXLN length to the descriptor.
   - 10, 11: The DMA does not modify the descriptor.
8. If the HALT bit is set the DMA closes the current buffer but does not fetch the next descriptor.
9. After a new DMAxLAR address has been updated, the DMA returns to Step 2 and fetches the control/status byte.

DMA Priority

The DMA priority is based upon the last channel serviced. After a channel is serviced it becomes the lowest priority channel. Table 146 lists the DMA priority; each DMA has equal priority under this scheme.

External DMA Signals

Two external pins are associated with each DMA Channel capable of external transfers (Channel 3 does not have external DMA capability). They are active Low DMAxREQ and DMAxACK signals. DMAxACK signals are outputs and DMAxREQ are inputs. DMAxREQ must be asserted for a minimum of one system clock period to generate one DMA transfer. DMAxREQ is left asserted for multiple transactions and deasserted after DMAxACK asserts for the last appropriate transfer.

DMA Timing

External DMA Transfer

Figure 60 shows the read and write timing of external DMA transfers.

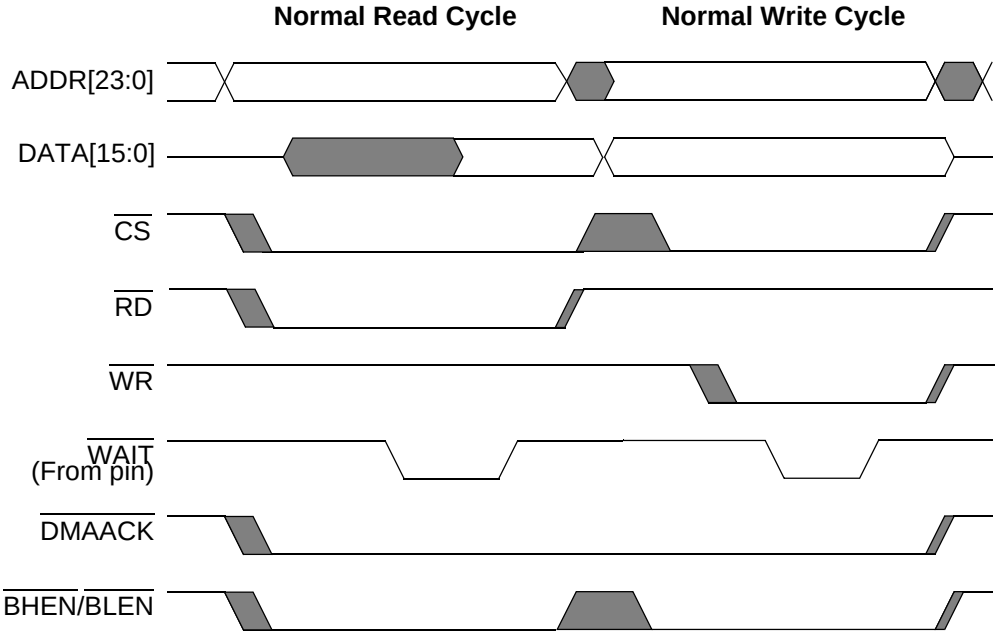

Figure 60. External DMA Transfer

Figure 75 displays the Stop Mode current consumption versus V_{DD} at ambient temperature with VBO and WDT disabled (I_{CCS2}).

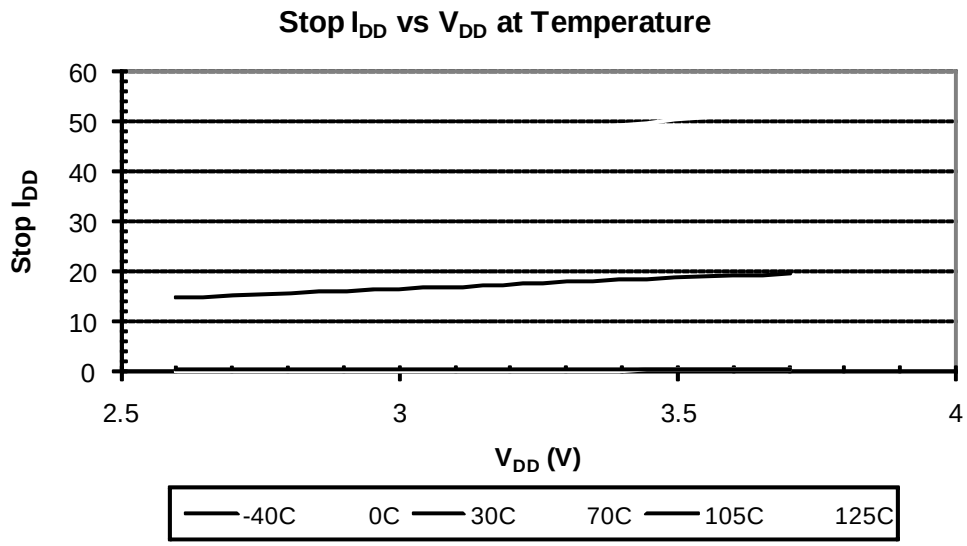

Figure 75. Stop Mode Current Versus V_{DD}

Table 203. ZNEO Z16F Series Part Numbering

Part Number	Flash (Kbytes)	RAM (Kbytes)	External Interface	I/O	Multi-Channel timers with PWM	Standard Timers with PWM	ADC Inputs	I^2C Master/Slave	UART with LIN and IrDA	ESPI	Package
ZNEO Z16F Series											
Standard Temperature: 0°C to +70°C											
Z16F2811AL20SG	128	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F2811FI20SG	128	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F2810FI20SG	128	4	No	60	1	3	12	1	2	1	80-pin QFP
Z16F2810AG20SG	128	4	No	46	1	3	12	1	2	1	64-pin LQFP
Z16F2810VH20SG	128	4	No	46	1	3	12	1	2	1	68-pin PLCC
Z16F6411AL20SG	64	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F6411FI20SG	64	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F3211AL20SG	32	2	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F3211FI20SG	32	2	Yes	60	1	3	12	1	2	1	80-pin QFP
Extended Temperature: –40°C to +105°C											
Z16F2811AL20EG	128	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F2811FI20EG	128	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F2810FI20EG	128	4	No	60	1	3	12	1	2	1	80-pin QFP
Z16F2810AG20EG	128	4	No	46	1	3	12	1	2	1	64-pin LQFP
Z16F2810VH20EG	128	4	No	46	1	3	12	1	2	1	68-pin PLCC
Z16F6411AL20EG	64	4	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F6411FI20EG	64	4	Yes	60	1	3	12	1	2	1	80-pin QFP
Z16F3211AL20EG	32	2	Yes	76	1	3	12	1	2	1	100-pin LQFP
Z16F3211FI20EG	32	2	Yes	60	1	3	12	1	2	1	80-pin QFP